Una Contribución al Diseño de Moduladores Sigma-Delta en Cascada Realizados Mediante Técnicas de Circuito en Tiempo Continuo

Memoria presentada por

RAMÓN TORTOSA NAVAS

para optar al grado de Doctor por la Universidad de Sevilla

Sevilla, abril de 2012
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Índice de Contenidos

Resumen. ................................................................. 1

1. Introducción y Justificación de la Unidad Temática de esta Tesis Doctoral ......................................................... 2
2. Convertidores Analógico-Digitales: Conceptos Básicos y Estado del Arte ................................................................. 3
3. Moduladores $\Sigma$Δ de Tiempo Continuo ............................. 8
4. Objetivos de esta Tesis Doctoral. ........................................ 13
5. Resultados y Discusión ..................................................... 14
6. Conclusiones ................................................................. 18
Referencias ................................................................. 21

Anexo 1: Convertidores Sigma-Delta de Tiempo Continuo – Conceptos, Arquitecturas, Circuitos y Errores. ...................... 23

1.1 Introduction .............................................................. 25
1.2 Fundamentals of A/D Conversion ..................................... 26
1.3 Basics of $\Sigma$Δ ADCs ............................................... 30
1.4 Continuous-Time $\Sigma$Δ Modulators ................................. 38
1.5 DT-to-CT Synthesis Methods and Basic CT-$\Sigma$ΔM Architectures . 50
1.6 Circuits and Errors ...................................................... 62
1.7 CT Integrators ............................................................ 64
1.8 Building-block Errors .................................................. 67
1.9 Excess Loop Delay ..................................................... 79
1.10 Comparator Metastability ............................................. 85
1.11 Clock Jitter Error ....................................................... 86
References ................................................................. 89
Anexo 2: Principales Publicaciones sobre los Trabajos Recogidos en la Tesis Doctoral ........................................... 95

Resumen ................................................................. 95

Publicación 1: “A New High-Level Synthesis Methodology of Cascaded Continuous-Time Σ∆ Modulators” ......................... 97

Publicación 2: “Clock Jitter Error in Multi-bit Continuous-Time Σ∆ Modulators with Non-Return-to-Zero Feedback Waveform” ....... 107

Publicación 3: “Systematic Design of High-Resolution High-Frequency Cascade Continuous-Time Sigma-Delta Modulators” .... 125

Publicación 4: “Design of a 1.2-V Cascade Continuous-Time Σ∆ Modulator for Broadband Telecommunications” .................... 139

Publicación 5: “A 12-bit@40MS/s Gm-C Cascade 3-2 Continuous-Time Sigma-Delta Modulator” ........................................ 145

Anexo 3: Otras Publicaciones sobre los Trabajos Recogidos en la Tesis Doctoral ..................................................... 151

Resumen ................................................................. 151

Publicación 6: “Cascaded Continuous-Time Σ∆ Modulators with Reduced Number of Analog Components - Application to VDSL” ... 153

Publicación 7: “Analysis of Clock Jitter Error in Multibit Continuous-Time Σ∆ Modulators with NRZ Feedback Waveform” ......... 161

Publicación 8: “A Direct Synthesis Method of Cascaded Continuous-Time Sigma-Delta Modulators” .................................. 165

Publicación 9: “Continuous-Time Cascaded Sigma-Delta Modulators for VDSL: A Comparative Study” ................................ 169

Publicación 10: “Design of a 1.2-V 130nm CMOS 13-bit@40MS/s Cascade 2-2-1 Continuous-Time Sigma-Delta Modulator” ....... 181

Publicación 11: “A Design Tool for High-Resolution High-Frequency Cascade Continuous-Time Σ∆ Modulators” ................. 187

Listado Completo de Publicaciones ..................................... 203
RESUMEN

Esta tesis doctoral es el resultado de un conjunto de trabajos de investigación encaminados a sistematizar y optimizar el diseño de convertidores analógico-digitales de tipo Sigma-Delta (ΣΔ), realizados mediante técnicas de circuito en tiempo continuo. Para ello, se ha desarrollado una nueva metodología de diseño de alto nivel que está especialmente orientada a topologías de moduladores ΣΔ en cascada. En esencia, el método propuesto consiste en sintetizar el filtro del modulador complementamente en el dominio del tiempo continuo, en lugar de hacerlo a partir de un equivalente en tiempo discreto, al que luego se le aplica una transformada discreta a continua. La síntesis directa en el dominio del tiempo continuo permite obtener arquitecturas con un menor número de componentes analógicos, lo que las hace más robustas frente a los errores de tolerancia de dichos componentes, principalmente debidos a variaciones aleatorias de los parámetros físicos del proceso tecnológico.

Además de la sensibilidad a los errores de tolerancia de los circuitos analógicos, otra fuente de error que limita en la práctica las prestaciones de los moduladores ΣΔ de tiempo continuo es debida a la incertidumbre en los instantes de conmutación de la señal de reloj, conocida como error de “jitter”. En esta tesis se demuestra que la potencia de ruido generada por dicho error en la banda de la señal presenta dos componentes: una que depende de los parámetros del filtro del lazo del modulador y otra debida a la propia señal de entrada. Del análisis matemático desarrollado se derivan ecuaciones de diseño que permiten optimizar las prestaciones de moduladores de lazo único y en cascada, minimizando el consumo de potencia para unas determinadas especificaciones dadas.

Como aplicación de los estudios realizados, se presentan varios casos de estudio prácticos de distintas topologías de moduladores, considerando diferentes tipos de implementación, tanto Gm-C como RC activa. Los diseños se realizaron en una tecnologías CMOS de 130nm, empleando una única fuente de alimentación de 1.2V, y con aplicación en la digitalización de señales con ancho de banda de 20MHz y resolución efectiva de 12 bits, lo que suponía alcanzar prestaciones en el estado del arte del momento.

La importancia y calidad de todos estos trabajos ha sido reconocida por la comunidad científica internacional, como se demuestra por las publicaciones de los mismos en artículos en revistas internacionales y conferencias internacionales, todos ellos sometidos al proceso de revisión por pares y editados por la mayoría por el IEEE, así como por otras entidades de la máxima relevancia en el área de investigación (Microelectrónica) en la que se enmarca la presente tesis doctoral.

Tras este resumen inicial, y en cumplimiento de la normativa vigente el presente documento incluye un resumen del trabajo correspondiente a esta tesis doctoral, justificándose la unidad temática de la tesis, los objetivos a alcanzar, un resumen global de los resultados obtenidos, la discusión de estos resultados y las conclusiones finales. Finalmente se incluyen las principales publicaciones realizadas, precedidas por un breve resumen de cada una de ellas.

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1 Acuerdo 7.2/CG 17-6-11, BOUS nº4, 13-7-11.
1. Introducción y Justificación de la Unidad Temática de esta Tesis Doctoral

Sería muy complicado, si no imposible, poder explicar la sociedad contemporánea sin hablar de las tecnologías de la información y las comunicaciones (TIC). Tanto es así que posiblemente la primera década del siglo XXI será recordada por el vertiginoso aumento de dispositivos electrónicos portátiles con capacidad multimedia y de conexión a Internet, así como por la proliferación de cada vez más redes de comunicación inalámbricas, que facilitan el acceso ubicuo a la información. Esta tendencia continúa, incrementando en cada generación de nuevos dispositivos tanto el número de aplicaciones que soportan como la tasa de transferencia de datos, con una autonomía cada vez mayor [1].

Uno de los exponentes más evidentes de la popularización de las TIC son los teléfonos celulares o móviles. La mayoría de terminales de última generación, conocidos como “smart phones”, soportan un gran número de estándares de comunicación, entre los que se encuentran GSM, GPRS/EDGE, CDMA, UMTS/WCDMA, HSDPA, Bluetooth y WLAN y más recientemente WiMAX y LTE. De hecho, se estima que hay actualmente coexistiendo en diferentes regiones del mundo más de cien estándares de comunicación diferentes [2].

Sin embargo, la forma actual en la que se incluyen nuevos modos de operación en un terminal implica la incorporación de nuevos “chipsets” específicos de Radio Frequencia (RF) y de su correspondiente circuitería de banda base. De este modo, no resulta difícil encontrar varios chips de radio, típicamente del orden de cinco, en un terminal de última generación que podamos adquirir hoy día en el mercado. Estos chips se interconectan normalmente en tarjetas de circuito impreso ultracompactas, o bien mediante el empleo de tecnologías avanzadas de conexionado y encapsulado como por ejemplo la tecnología LTCC (de “Low Temperature Co-fired Ceramic “) o SiP (de “System-in-Package”), que hace de los teléfonos móviles más actuales unas auténticas maravillas de la miniaturización [3].

A pesar de ello, el ritmo creciente de incorporación de nuevos estándares de comunicación y funcionalidades de los sistemas electrónicos, hace que el modelo de incorporación de las mismas – basados en actualización del hardware – esté llegando a sus límites, lo que está planteando la necesidad de buscar soluciones que combinen un uso más eficiente de hardware y software, que permitan programar o actualizar los sistemas electrónicos vía software o “firmware”. Todo ello
está siendo impulsado por el escalado de las tecnologías micro-nanoelectrónicas, las cuales están posibilitando una mayor integración monolítica en un único chip de sistemas electrónicos completos, denominados “Systems on Chip” o SoC [3]-[5].

La miniaturización de sistemas electrónicos completos a escala nanométrica permite, por una parte, alcanzar una mayor velocidad de los dispositivos (lo que se traduce en una mayor tasa de transferencia de datos) y ahorro en términos de tamaño (lo que supone una disminución del coste) y del consumo de potencia (lo que permite una mayor portabilidad y eficiencia energética). Es precisamente esta tendencia hacia una mayor integración y uso masivo de procesamiento digital de la señal lo que ha propiciado el uso de tecnologías CMOS para la realización de sistemas de comunicación inalámbricos, en lugar de los tradicionalmente empleados para ello (Bipolar, BiCMOS, GaAs, etc.). De hecho, gracias a las mejoras de los procesos CMOS nanométricos actuales, se pueden alcanzar frecuencias de tránsito de centenas de GHz, por ejemplo 200GHz en una tecnología típica de 40nm. Ello permite que el diseño de circuitos operando en el rango de Radio Frecuencia (RF) puedan ser considerado en cierta manera de “baja frecuencia”, y por tanto diseñarse siguiendo procedimientos similares a los empleados en el pasado para los circuitos analógicos y de señal mixta [2].

Todo ello está dando lugar a que en los sistemas electrónicos, cada vez más funcionalidades sean llevadas a cabo digitalmente, en lugar de analógicamente, lo que se traduce en un desplazamiento de la frontera entre la parte analógica y la digital cada vez más cercana al punto donde se recibe o se emite la información. En este escenario, la mayor parte del procesado de la señal que realizan los circuitos analógicos se limitan a tareas de interfaz analógica-digital, es decir, acondicionamiento de la señal (preamplificación, filtrado, traslación en frecuencia, etc), conversión digital-analógico y analógico-digital, siendo ésta última el objetivo principal de esta tesis doctoral.

2. Convertidores Analógico-Digitales: Conceptos básicos y Estado del Arte

Un *convertidor analógico-digital* (ADC de “Analog-to-Digital Converter”) es un circuito electrónico que transforma una señal continua en el tiempo y en la amplitud (señal analógica) en otra señal discreta en el tiempo cuya amplitud está cuantificada y codificada, generalmente mediante un código binario de $N$ bits. La Fig.1(a) muestra el diagrama de bloques conceptual de
un ADC, el cual incluye los siguientes componentes: un filtro “anti-aliasing”, un circuito de muestreo y retención (S/H de “Sampling-and-Hold”), un cuantizador y un codificador. La operación de cada uno de estos bloques se ilustra en la Fig.1(b). En primer lugar, el filtro “anti-aliasing” elimina las componentes espectrales que se encuentran por encima de la mitad de la frecuencia de muestreo, $f_s$, a la cual opera el circuito S/H. En caso contrario, de acuerdo con el teorema de Nyquist, las componentes de alta frecuencia se plegarían en la banda, $B_W$, de la señal de entrada, $x_a$, corrompiendo de esta manera la información. La señal limitada en banda que resulta a la salida del filtro, $x_{bl}(t)$, se muestrea en el circuito S/H, dando lugar a una señal en tiempo discreto, $x_{s,n} = x_{bl}(nT_s)$, cuyo rango de amplitudes continuo se mapea en el cuantizador en un conjunto de niveles discretos de amplitud. Finalmente, el codificador asigna un código binario a cada uno de esos niveles, resultando en la secuencia de datos digitales de salida, $y_{d,n}$ [6].

![Diagrama de bloques conceptual y procesamiento de la señal](image)

**Fig. 1:** Conversión analógica-digital: (a) Diagrama de bloques conceptual. (b) Procesamiento de la señal.
Como se ilustra en la Fig.1(b), la conversión A/D comprende dos procesos fundamentales: muestreo y cuantización. Ambos realizan una transformación continua-discreta de la señal analógica de entrada; el primero en el tiempo y el segundo en amplitud. Los errores inherentes a estos dos procesos limitan el funcionamiento de un ADC, en términos de su velocidad de operación y de su precisión o resolución, incluso aunque los componentes de éste sean ideales. Estas dos características, velocidad y resolución, determinan las especificaciones fundamentales de un ADC, existiendo un compromiso de diseño entre ambas (y el consumo de potencia), de forma que a mayor velocidad de procesamiento, el ADC obtendrá una menor resolución y viceversa.

Las prestaciones, en términos de resolución, velocidad y consumo de potencia pueden cuantificarse mediante la siguiente figura de mérito o FOM (de “Figure Of Merit”):

\[
\text{FOM}_{\text{pJ/conv}} = \frac{P_w (W)}{2^{\text{ENOB (bits)}} \cdot \text{DOR (S/s)}} \cdot 10^{12}
\]

(1)

donde \(P_w (W)\) es la potencia en vatios, ENOB (de “Effective Number Of Bits”) es el número efectivo de bits y DOR (de “Digital Ouput Rate”) es la tasa de muestreo correspondiente a la frecuencia mínima de muestreo que determina el teorema de Nyquist, conocida como frecuencia de Nyquist.

La Fig. 2 ilustra el estado del arte de ADC realizados en tecnologías CMOS reportados hasta el año 2010, situándolos en el plano resolución – ancho de banda [7][8]. Sobre este plano se representan las prestaciones obtenidas por diferentes técnicas utilizadas para la conversión A/D, agrupados en dos categorías fundamentales: “Nyquist-Rate” y Sigma-Delta (ΣΔ). Como su nombre indica, los ADC de Nyquist, que pueden implementarse mediante varias técnicas (Flash, “Two-Step”, “Folding”, “Pipeline”, SAR o “Successive Approximation Register”) operan a la frecuencia de Nyquist. Por el contrario, los convertidores ΣΔ emplean una frecuencia de muestreo superior a la frecuencia de Nyquist. Al cociente entre la frecuencia de muestreo y la frecuencia de Nyquist se le conoce como razón de sobremuestreo u OSR (“OverSampling Ratio”).
Las características específicas de cada una de las técnicas de conversión incluidas en la Fig. 2 – cuya descripción está fuera del alcance de esta tesis – las adecúa a diferentes rangos de aplicación en términos de ancho de banda y resolución [9]. Como puede observarse, los ADC de tipo ΣΔ cubren un área muy extensa del plano resolución-velocidad, abarcando un rango de anchos de banda desde 100Hz hasta 100MHz. Sin embargo, las aplicaciones de mayor velocidad están dominadas por los ADC de Nyquist, especialmente los de tipo SAR y Flash.

Si se comparan las prestaciones de los ADC en términos de FOM₁ como se ilustra en la Fig. 3, puede verse como los ADC ΣΔ obtienen un mejor rendimiento hasta valores de DOR del orden de 100kS/s, obteniendo resultados similares a los SAR hasta 10MS/s. Sin embargo, como se muestra en la Fig. 2, la región del plano resolución-velocidad cubierta por los ADC ΣΔ es mayor que la correspondiente a todos los ADC de tipo Nyquist, siendo la tendencia en los
últimos años a aumentar aún más dicha región de dominancia de los ADC $\Sigma\Delta$, como demuestran algunos prototipos reportados, que reportan prestaciones del estado del arte, con valores de DOR por encima de 200MS/s y frecuencias de muestreo de varios GHz [10][11].

Además de las razones expuestas, los ADC $\Sigma\Delta$ ofrecen ventajas clave para su integración en SoCs. A diferencia de los ADC de Nyquist, cuya resolución depende fuertemente de la alta precisión de sus bloques componentes, las técnicas de sobremuestreo y de conformación de ruido de cuantización empleadas en los ADC $\Sigma\Delta$ permiten intercambiar velocidad por precisión. De esta forma puede obtenerse una operación relativamente insensible a las imperfecciones de la circuitería analógica a expensas de una mayor complejidad y velocidad en la circuitería digital asociada (necesaria para la decimación y filtrado). Por ello las técnicas de modulación $\Sigma\Delta$ resultan idóneas para la implementación de ADC de altas prestaciones integrados en tecnologías CMOS nanométricas, las cuales son más adecuadas para proporcionar circuitos digitales rápidos que circuitos analógicos precisos [12].

Fig. 3: Estado del arte de convertidores analógico-digitales CMOS a finales de 2010. Representación FOM$_1$ versus DOR. (DR="Dynamic Range", DOR="Digital Output Rate").
Todas estas ventajas explican el alto interés – no sólo a nivel académico sino también en el ámbito de la industria – de la comunidad científica internacional por los ADC \( \Sigma \Delta \), como se demuestra por el gran número de foros dedicados a este tipo de convertidores frente al resto de técnicas de ADC. Sin embargo, a pesar de dichas ventajas, la continua demanda de prestaciones cada vez más exigentes (en términos de velocidad, resolución y consumo de potencia), unido a las dificultades inherentes al diseño de circuitos analógicos en nodos tecnológicos de última generación, requieren el uso de estrategias apropiadas, tanto a nivel de sistema como de circuito, que permitan implementar los ADC \( \Sigma \Delta \) de forma más eficiente.

En este escenario se enmarca el trabajo de investigación llevado a cabo en esta tesis doctoral, cuyo objetivo principal es el diseño sistemático de ADC \( \Sigma \Delta \) realizados mediante técnicas de circuito de tiempo continuo, y cuyos fundamentos se resumen en el siguiente apartado. Una explicación más detallada de los mismos se pueden encontrar en el Anexo 1 de esta tesis.

3. **Moduladores \( \Sigma \Delta \) de Tiempo Continuo**

La Fig. 4 muestra el diagrama de bloques conceptual de un ADC \( \Sigma \Delta \) concebido para la conversión de señales paso de baja\(^2\), considerando dos casos: una implementación mediante técnicas de circuito de tiempo discreto (DT de “Discrete-Time”), mostrada en la Fig. 4(a); y una implementación basada en técnicas de tiempo continuo (CT de “Continuous-Time”), ilustrada en la Fig. 4(b). En ambos casos, el diagrama de bloques comprende tres componentes principales: un filtro “antialiasing”, un modulador \( \Sigma \Delta \) (M\( \Sigma \Delta \)) y un decimador digital. La operación del convertidor puede resumirse como sigue. Después de ser filtrada, la señal es sobremuestreada y cuantizada en el M\( \Sigma \Delta \). Este bloque filtra también el error de cuantización, conformando su espectro en frecuencia de tal forma que la mayor parte de su potencia queda fuera de la banda de la señal, donde es eliminada por el filtrado digital. La salida del modulador – codificada en un número reducido de bits – pasa a través del decimador digital donde, después del filtrado de los componentes que están fuera de la banda de la señal, los datos de salida son decimados de forma que se reduce \( f_s \) hasta la frecuencia de Nyquist, \( f_d \).

\(^2\) El diagrama de bloques conceptual de un ADC \( \Sigma \Delta \) paso de banda es análogo al mostrado en la Fig. 4, excepto que tanto el filtro anti-aliasing como el filtro del lazo del modulador deben ser de tipo paso de banda.
Fig. 4: Diagrama de bloques de: (a) ADC $\Sigma\Delta$ de tiempo discreto. (b) ADC $\Sigma\Delta$ de tiempo continuo.

Las prestaciones de un ADC $\Sigma\Delta$ ideal están determinadas en última instancia por el $M_{\Sigma\Delta}$, ya que éste es el responsable de realizar la conversión A/D. Por lo tanto, nos centraremos en este bloque de aquí en adelante.

**Fundamentos de Moduladores $\Sigma\Delta$**

Suponiendo un modelo linealizado del cuantizador en la Fig. 4, en el que el error de cuantización se puede modelar como una fuente aditiva de ruido blanco, se puede demostrar que la transformada $Z$ de la salida del modulador viene dada por la siguiente expresión:

$$Y(z) = \text{STF}(z) \cdot X(z) + \text{NTF}(z) \cdot E(z)$$  \hspace{1cm} (2)$$

donde $X(z)$ y $E(z)$ representan la transformada $Z$ de la señal de entrada y del error de cuantización, respectivamente; y STF($z$) y NTF($z$) representan la función de transferencia de la señal y del ruido de cuantización. En el caso de un $M_{\Sigma\Delta}$ DT, se puede demostrar que STF($z$) y NTF($z$) vienen dadas por [6]:

$$\text{STF}(z) = \frac{H(z)}{1 + H(z)}; \quad \text{NTF}(z) = \frac{1}{1 + H(z)}$$  \hspace{1cm} (3)$$
En el caso de los ΜΣΔ CT, puede demostrarse que en determinadas condiciones, se pueden derivar unas expresiones similares a (3) en el dominio continuo de la frecuencia, \( f \), obteniéndose que

\[
\text{STF}(f) = \frac{H(f)}{1 + H(f)}; \quad \text{NTF}(f) = \frac{1}{1 + H(f)}
\]  

(4)

De las expresiones (3) y (4), puede concluirse que si el filtro del lazo del modulador se diseña de forma que \( |H(f)| \to \infty \) en la banda de la señal, entonces \( |\text{STF}(f)| \to 1 \) y \( |\text{NTF}(f)| \to 0 \) en dicha banda. Es decir, la acción de la realimentación y de la ganancia del filtro del lazo del MSD es tal que la señal de entrada no se ve alterada (idealmente), mientras que se realiza un conformado\(^3\) del espectro del ruido de cuantización, de forma que se reduce (idealmente se elimina) la potencia del ruido de cuantización integrado en la banda de la señal, dado por [6][13]:

\[
P_Q \equiv \frac{X_{FS}^2}{12 \cdot (2^B - 1)^2 \cdot f_s \int_{f_L}^{f_U} \text{NTF}(f)^2 \, df}
\]

(5)

donde \( B \) y \( X_{FS} \) representan respectivamente el número de bits y el fondo de escala del cuantizador; y \( f_L, f_U \) denotan los los límites inferior y superior de la banda de la señal.

En el caso de señales paso de baja, y considerando una función de transferencia del ruido orden \( L \) y de tipo diferenciadora\(^4\), es decir \( \text{NTF}(z) = (1 - z^{-1})^L \), de la expresión en (5) se obtiene que:

\[
P_Q \equiv \frac{\pi^{2L} X_{FS}^2}{12 \cdot (2^B - 1)^2 \cdot (2L + 1) \cdot \text{OSR}^{(2L+1)}}
\]

(6)

donde \( \text{OSR} \) representa la razón de sobremuestreo.

---

\(^3\) Debido a esta acción de conformado del espectro del ruido de cuantización a los ADC ΣΔ se les conoce también como “noise-shaping” ADC [12].

\(^4\) Este tipo de funciones son las más frecuentemente empleadas en ΜΣΔ paso de baja [12].
La expresión (6) muestra como al aumentar \( L \), OSR y/o \( B \), se reduce la potencia del ruido de cuantización en la banda de la señal, y por tanto la resolución efectiva del convertidor A/D resultante. La combinación de estas tres estrategias no excluyentes da lugar a una pléyade de arquitecturas de MΣΔ, las cuales pueden clasificarse atendiendo a diversos criterios, entre otros: la naturaleza de la señal de entrada (paso de baja o paso de banda); el número de bits del cuantizador interno (un bit o multi-bit), el número de cuantizadores incluido en el lazo (dando lugar a arquitecturas de un único lazo o en cascada), la técnica de circuito empleada para la implementación del filtro del lazo (tiempo discreto o tiempo continuo). La explicación detallada de cada una de estas familias de MΣΔ – cada una con sus pros y sus contras – va más allá de los objetivos de esta tesis doctoral y puede encontrarse en multitud de monografías [6][13][14]. En su lugar en este resumen nos centraremos en analizar las ventajas e inconvenientes del empleo de técnicas de circuito de tiempo continuo – objeto principal de este trabajo de investigación.

**Ventajas de los Moduladores ΣΔ de Tiempo Continuo**

Comparando los dos diagramas de la Fig. 4, se pueden apreciar algunas diferencias simples, pero importantes, entre los ADC ΣΔ DT (Fig. 4(a)) y CT (Fig. 4(b)). Además de la ya mencionada y obvia diferencia correspondiente a la técnica de circuito y la dinámica empleada en el filtro del lazo, la diferencia más significativa que se aprecia es en la posición en la que tiene lugar la operación de muestreo – mostrada de forma explícita y conceptual como un bloque S/H en la Fig. 4. Puede observarse como en el caso de los convertidores ADC ΣΔ CT, la operación S/H tiene lugar dentro del lazo del modulador, justo en la entrada del cuantizador. Esta característica fundamental ofrece las siguientes ventajas:

- **Mayor velocidad de operación con menor consumo de potencia**, propiciada por la operación en tiempo continuo del filtro del lazo, en la que la dinámica de los circuitos no es parásita (como ocurre en los circuitos de condensadores en conmutación por ejemplo), sino una primitiva de diseño [13].

- **Filtrado extra “anti-aliasing” implícito**, ya que el filtro del lazo se puede emplear para este propósito, relajando las especificaciones o incluso eliminando la necesidad del filtrado previo “anti-aliasing” [14].
• **Menor impacto de los errores causados por la operación de muestreo.** Esto es una consecuencia directa del hecho de que la operación de muestreo no tiene lugar en el nudo de entrada del modulador, sino dentro del lazo. De este modo, los errores de muestreo son filtrados de manera análoga al ruido de cuantización [13].

• **No necesidad de llaves de muestreo en la entrada,** evitando la necesidad de emplear técnicas como “clock boosting”, necesarias para poder obtener una linealidad aceptable con bajas tensiones de polarización, como las que se emplean en tecnologías CMOS nanométricas.

• **Menor ruido térmico,** ya que al no ser muestreado, no hay efecto de plegamiento. Por tanto, la potencia de ruido térmico integrado en la banda de la señal es típicamente menor que la de los MΣΔ DT, en los que debido al muestreo, una gran cantidad del ruido térmico (KT/C) se pliega en la banda de la señal, constituyendo una limitación fundamental en la resolución efectiva [13].

• **Menor impacto del ruido de conmutación,** denominado “digital noise” o “switching noise”, ya que resulta atenuado por la acción del filtro del lazo, del mismo modo que el ruido de cuantización.

**Inconvenientes de los Moduladores ΣΔ de Tiempo Continuo**

Las principales desventajas y limitaciones de los MΣΔ CT son las siguientes:

• **Respuesta dinámica más complicada,** debido al procesamiento de señales de tiempo continuo y de tiempo discreto a través de un sistema no lineal. Esta característica dificulta el análisis matemático de los MΣΔ CT, y consecuentemente la síntesis de los mismos.

• **Mayor sensibilidad a las no linealidades del circuito,** especialmente los que están situados en el nudo de entrada del modulador. Esta limitación es particularmente importante en filtros del lazo realizado con integradores del tipo Gm-C, ya que el transconducto situado en la entrada realiza una conversión voltaje-corriente. Esta operación genera distorsión armónica que condiciona la linealidad de todo el modulador.
• **Mayor sensibilidad a los errores de tolerancia de los elementos de circuito.** Esto es algo inherente a los circuitos CT, ya que las constantes de tiempo vienen dadas como el producto de dos parámetros descorrelacionados entre sí, por ejemplo la transconductancia y el condensador de integración en un integrador Gm-C, o la constante RC en un integrador RC-activo. Ello requiere el empleo de estrategias de sintonizado o “tuning” para ajustar los coeficientes del filtro del lazo, los cuales están determinados por dichas constantes de tiempo.

• **Mayor impacto del error debido a la incertidumbre de los instantes de conmutación de la señal de reloj, conocido como error de “jitter”.** En un ΣΔ CT, hay dos bloques de circuito sujetos a este error: el circuito de S/H y el convertidor digital-analógico (DAC de “Digital-to-Analog Converter”) de la realimentación, en el cual se realiza una transformación DT-a-CT en el nudo de entrada, siendo por tanto éste último el que limita las prestaciones del modulador [15]-[17].

### 4. Objetivos de esta Tesis Doctoral

Los trabajos de investigación recogidos en esta tesis doctoral pretenden hacer frente a los problemas y limitaciones mencionados en el apartado anterior de los ΣΔ CT, con el objetivo fundamental de sistematizar el diseño de dichos moduladores, prestando especial interés a las topologías en cascada y tratando de optimizar sus prestaciones en términos de consumo de potencia y robustez frente las principales fuentes de error: non linealidad de los circuitos de entrada, tolerancia de los elementos de circuito y error de “jitter” del reloj. Este objetivo general se desglosa en los siguientes objetivos parciales:

1) Desarrollar una metodología de síntesis y diseño de alto nivel para topologías de ΣΔ CT en cascada que permita obtener arquitecturas más robustas y eficientes en términos de consumo de potencia y de sensibilidad a los errores de circuito.

2) Realizar un análisis y modelado preciso del error del “jitter” de reloj, con un doble propósito. Por una parte, encontrar un modelo preciso para la simulación de comportamiento de ΣΔ CT. Por otra parte, obtener ecuaciones de diseño
que permitan minimizar el impacto del error y optimizar así las prestaciones de los \( \Sigma \Delta \) CT para unas especificaciones dadas.

3) Encontrar soluciones a nivel de circuito que reduzcan el efecto de los errores no lineales en los \( \Sigma \Delta \) CT.

4) Demostrar la viabilidad del uso de \( \Sigma \Delta \) CT en cascada para la digitalización de señales de banda ancha (20MHz) con resoluciones medias (12bit).

5. Resultados y Discusión

Los trabajos recogidos en esta tesis doctoral se estructuran alrededor de los objetivos descritos en el apartado anterior. Los resultados obtenidos dan respuesta a los retos planteados en dichos objetivos, demostrando la viabilidad de los moduladores \( \Sigma \Delta \) CT para la realización de ADC de banda ancha y resolución media. A continuación, se resumen los resultados más importantes, los cuales se describen en detalle en las aportaciones que conforman la presente memoria, todas ellas correspondientes a publicaciones en foros de la máxima relevancia internacional.

**Propuesta de un Nuevo Método de Síntesis Directa de Moduladores \( \Sigma \Delta \) CT en Cascada**

En esta tesis doctoral se propone un nuevo nuevo metodología de síntesis y diseño de alto nivel especialmente orientada a \( \Sigma \Delta \) CT en cascada. El método – descrito en la Publicación 1 del Anexo 2 de esta memoria [18]– se basa en la síntesis directa en el dominio del tiempo continuo de \( \Sigma \Delta \) CT en cascada, en lugar de aplicar una transformada discreta-a-continua a un \( \Sigma \Delta \) DT equivalente, como se había propuesto anteriormente. En contraposición, el método propuesto permite optimizar la función de transferencia de la señal y del ruido de cuantización, distribuyendo los ceros de ésta última de forma óptima en la banda de la señal, de forma que se puede minimizar la potencia del ruido integrada en banda. Las arquitecturas obtenidas mediante el método propuesto son más eficientes que las sintetizadas a partir de un modulador DT equivalente, reduciendo el número de componentes analógicos necesarios. De este modo, se obtienen arquitecturas más eficientes en términos de consumo de potencia y robustez frente a las tolerancias de los coeficientes del filtro del lazo – uno de los principales factores limitantes de los \( \Sigma \Delta \) CT como se describe en el apartado 4 de este resumen.
El método propuesto se puede aplicar a cualquier topología de MΣΔ CT en cascada, como se demuestra en la primera publicación recogida en el Anexo 2 [19], en la que se sintetizan varias cascadas diferentes, entre otras: 2-1-1, 2-1-1-1, 2-2-1 y 3-2.

**Análisis y Modelado del Error del “jitter” del Reloj en MΣΔ CT con DAC NRZ**

Como se mencionó en el Apartado 4, uno de los factores limitantes del funcionamiento de los MΣΔ CT es el error de “jitter” del reloj. En la Publicación 2 del Anexo 2 [20] de esta tesis se presenta un análisis detallado de este error para el caso de DAC NRZ (de “Non Return to Zero”) y cuantización multi-bit. Este caso es uno de los más empleados en aplicaciones prácticas de media resolución (11-14 bits) y banda ancha (10-20 MHz), por lo que su estudio es de interés para el diseño óptimo de MΣΔ CT en tales aplicaciones.

El análisis llevado a cabo en esta tesis doctoral se basa en el uso de la formulación espacio estado (“estate-space formulation”) lo que dota al estudio matemático realizado de un carácter general y aplicable a cualquier topología de MΣΔ CT tanto de lazo único como en cascada. Como resultado, se demuestra que la potencia de ruido integrada en la banda de la señal debida al error de jitter puede separarse en dos componentes: uno que depende de la función de transferencia del filtro del lazo del modulador y otra que depende de los parámetros de la señal de entrada. Esta última componente, que no se considera en otros estudios previos, permite predecir con gran precisión la pérdida de resolución causada por el “jitter”, mostrando efectos no tenidos en cuenta anteriormente en la literatura.

Como resultado del análisis se obtienen ecuaciones de diseño para la potencia de ruido integrada en banda y la relación señal-ruido, las cuales pueden ser empleadas para la optimización de MΣΔ CT en términos de su sensibilidad al error de “jitter”. Las predicciones teóricas son validadas mediante simulación en el dominio del tiempo de diversas arquitecturas de moduladores de lazo simple y en cascada.

**Desarrollo de una Metodología “Top-Down/Bottom-Up” para el Diseño Sistemático de Moduladores ΣΔ CT en Cascada**

El método de síntesis directa en el dominio del tiempo continuo se integra conjuntamente con el análisis y modelado de las principales fuentes de error que afectan al funcionamiento de MΣΔ
CT, considerando tanto efectos de circuito (ganancia finita, GBW, mismatch, ruido, etc) como arquitecturales (exceso de retraso del laxo, “jitter” del reloj, etc) para desarrollar una metodología sistemática “top-down/bottom-up” que permita asistir el diseño desde las especificaciones de sistema hasta el nivel eléctrico de dispositivo.

Como se detalla en la Publicación 3 del Anexo 2 [21], la metodología propuesta combina optimización y simulación en los distintos niveles de abstracción de la jerarquía del modulador (arquitectura, bloques, circuito) e incorpora la generación de frentes Pareto-óptimos que permiten reducir el número de iteraciones en el proceso de diseño de alto nivel. El método se aplica al estudio de diversas arquitecturas en cascada de orden 5, concretamente 2-1-1-1, 2-2-1 y 3-2, considerando unas especificaciones de 12-bit en un ancho de banda de 20MHz.

**Casos de Estudio y Soluciones Circuitales**

Los análisis y metodologías desarrolladas en esta tesis se han aplicado al diseño dos MΣΔ CT en cascada, detallados en la Publicaciones 4 [22] y 5 [23] del Anexo 2, implementados en una tecnología CMOS de 130nm con una única fuente de alimentación de 1.2V:

- El primer circuito es una arquitectura 2-2-1 y cuantización de 4 bits en las tres etapas. El primer integrador se implementa mediante la técnica RC-activa, mientras que el resto de los integradores son de tipo Gm-C [22].

- El segundo diseño es una arquitectura 3-2 con cuantización de 4 bits en las dos etapas y completamente implementado mediante integradores Gm-C [23].

En ambos casos, se proponen circuitos transconductores para el filtro del lazo que implementan una técnica de cancelación del término cuadrático, con el fin de obtener mejor linealidad. En el segundo diseño se utiliza un transconductor basado en degeneración de fuente y enriquecimiento de la ganancia para el integrador frontal, al ser éste el más crítico.

Los dos diseños emplean DAC de realimentación en modo corriente (“current steering DAC”) así como algoritmos DEM (de “Dynamic Element Matching”) para compensar el error de desaparecimiento de los elementos unitarios de dichos DAC (fuentes de corriente unitarias).
Los dos circuitos se han verificado mediante simulación eléctrica a nivel de transistor, mostrando resultados satisfactorios y validando la metodología desarrollada en esta tesis.

Fig. 5: Ejemplo de modulador $\Sigma\Delta$ en cascada 3-2 diseñado en esta tesis: (a) Diagrama de bloques. (b) Esquemático del transconductor sintonizable utilizado en filtro del lazo. (c) Layout del modulador. (d) Espectro de salida obtenido por simulación eléctrica a nivel de transistor.
6. Conclusiones

Esta tesis doctoral representa una contribución al diseño de moduladores $\Sigma \Delta$ ($M \Sigma \Delta$) realizados mediante técnicas de tiempo continuo (CT) para la implementación de convertidores analógico-digitales (ADC) en tecnologías CMOS nanométricas. Los estudios llevados a cabo se centran principalmente en topologías en cascada, las cuales resultan especialmente apropiadas para aplicaciones de banda ancha (20MHz), en las que el uso de valores bajos de sobremuestreo obliga a aumentar el orden del filtrado del lazo del modulador para conseguir una resolución media (12 bits). A pesar de las potenciales ventajas en velocidad de las técnicas de circuito CT, se han reportado muy pocos circuitos integrados de $M \Sigma \Delta$ CT en cascada. Ello es debido principalmente a la mayor sensibilidad de los $M \Sigma \Delta$ CT a ciertos errores de circuito, como la tolerancia de las constantes de tiempo y el “jitter” del reloj.

En este contexto, el trabajo desarrollado en esta tesis presenta una serie de herramientas analíticas y metodológicas encaminadas a sistematizar el diseño de $M \Sigma \Delta$ CT en cascada, optimizando sus prestaciones en términos de consumo de potencia y área. Las principales contribuciones de esta tesis son las siguientes:

- Se ha desarrollado una nueva metodología de diseño de $M \Sigma \Delta$ CT en cascada basada en realizar la síntesis directamente en el dominio del tiempo continuo, en lugar de aplicando una transformada discreta-continua a un $M \Sigma \Delta$ de tiempo discreto equivalente. Como resultado, se obtienen circuitos más simples topológicamente y más robustos frente a errores de tolerancia de sus componentes que los circuitos obtenidos con técnicas de síntesis convencionales.

- Se ha analizado el impacto del error de “jitter” del reloj en $M \Sigma \Delta$ CT con cuantización multi-bit y convertidor digital-analógico con forma de onda sin retorno a cero (NRZ de “Non Return to Zero”). El estudio – basado en el uso de formulación espacio-estado – es aplicable tanto a topologías de modulador en cascada como de lazo simple, obteniéndose ecuaciones de diseño para la potencia del ruido integrado en la banda de la señal y para la relación señal ruido. El estudio demuestra matemáticamente que el efecto del jitter se debe a dos componentes del error: una debida a los parámetros del filtro del lazo del modulador, del sobremuestreo y del número de bits del cuantizador interno, y otra debida
a la frecuencia y amplitud de la señal de entrada (supuesta ésta sinusoidal). Dichas ecuaciones permiten optimizar el diseño de los MΣΔ CT, obteniendo una frecuencia de muestreo que minimiza la potencia del ruido “jitter” en la banda de la señal.

- Se han propuesto nuevas arquitecturas de MΣΔ CT en cascada obtenidas mediante la metodología de síntesis propuesta, destacando dos topologías de quinto orden 2-2-1 y 3-2, esta última ilustrada en la Fig. 5(a) considerando una implementación Gm-C.

- A nivel de circuito, se ha considerado el diseño del filtro del lazo de los moduladores empleando tanto integradores RC-activo como Gm-C. Para estos últimos, se ha propuesto una nueva topología de transconductor sintonizable, mostrado en la Fig. 5(b), que utilizan técnicas de linealización basadas en la cancelación del término cuadrático, y que extienden el ancho de banda requerido mediante la introducción de un cero de compensación en alta frecuencia.

- Se han demostrado las ventajas de las técnicas y metodologías propuestas a través del diseño e implementación en una tecnología CMOS de 130nm de dos moduladores en cascada.

  - El primero de ellos es una cascada 2-2-1 cuyo filtro del lazo está implementado por un integrador RC-activo frontal mientras que el resto son Gm-C.

  - La segunda topología es una cascada 3-2, implementada mediante integradores Gm-C y con resonación en las dos etapas para distribuir de forma óptima los ceros de la función de transferencia del ruido en el ancho de banda de la señal.

Ambos moduladores operan con una frecuencia de muestreo de 240MHz y emplean cuantización de 4 bits en todas las etapas, incluyendo algoritmos de corrección DEM en la primera etapa para reducir el impacto de la no linealidad debida al DAC. Los dos circuitos han sido validados mediante simulación eléctrica a nivel de transistor, considerando una única fuente de alimentación de 1.2V. El primer prototipo (2-2-1) obtiene una resolución efectiva de 13bits en un ancho de banda de 20MHz con un consumo de potencia estimado de 60mW. El segundo prototipo (3-2), cuyo layout se muestra en la Fig. 5(c), obtiene
12bits@20MHz, teniendo un consumo estimado de 70mW. Como ilustración la Fig. 5(d) muestra el espectro de salida del modulador.

Los resultados obtenidos en esta tesis demuestran la viabilidad del uso de ΣΔ CT en cascada para la implementación de ADC en aplicaciones de banda ancha y proporcionan herramientas metodológicas para desarrollar topologías que permitan aumentar las prestaciones de dichos ADC en las próximas generaciones de sistemas de comunicación.
Referencias


ANEXO 1: CONVERTIDORES SIGMA-DELTA DE TIEMPO CONTINUO – CONCEPTOS, ARQUITECTURAS, CIRCUITOS Y ERRORES

RESUMEN

Este anexo presenta una descripción panorámica de los moduladores ΣΔ de tiempo continuo, ofreciendo una explicación de sus fundamentos, arquitecturas principales, circuitos y errores.

Algunas partes de este anexo fueron incluidas en la siguiente publicación de la que el doctorando es coautor:

Annex 1

Continuous-time Sigma-Delta Converters
Basic Concepts, Architectures, Circuits and Errors

1.1 Introduction

Sigma-Delta Modulators (ΣΔMs) have demonstrated to be very suited for the implementation of the Analog-to-Digital (A/D) interface in many different electronic systems, covering a large number of applications – from instrumentation to telecom [Nors97][Geer02][Rio06][Schr05]. This type of A/D Converters (ADCs), composed of a low-resolution quantizer embedded in a feedback loop, uses oversampling (a sampling frequency much larger than the Nyquist frequency) to reduce the quantization noise and ΣΔ modulation to push this noise out of the signal band [Inos62]. The combined use of redundant temporal data (oversampling) and filtering (ΣΔ modulation) results in high-resolution, robust ADCs, which have lower sensitivity to circuit parasitics and tolerances, and are more suitable for the implementation of ADCs in nanometer CMOS technologies [Rodr03][Schr05].

The majority of ΣΔMs reported so far have been implemented using Discrete-Time (DT) circuit techniques, mostly based on Switched-Capacitor (SC) circuits [Rio06]. However, the increasing demand for ever faster ADCs in broadband communication systems has boosted the interest in Continuous-Time (CT) ΣΔMs. These modulators have intrinsic anti-aliasing filtering and are able to operate at higher sampling rates with lower power consumption than their DT counterparts [Bree01][Cher00][Ortm06].

CT-ΣΔMs have much in common with DT-ΣΔMs, whose basic properties and limitations have been described elsewhere [Nors97][Mede99][Pelu99][Rabi99][Geer02][Rio06]. However, there are some characteristics which are peculiar to CT-ΣΔMs. This annex gives an overview of their operating principles and architectures, circuit errors and models, design methodologies and practical considerations.
1.2 Fundamentals of A/D Conversion

An ADC is a system that transforms signals which are continuous in time and amplitude (analog signals) into DT signals which are quantized and codified in amplitude (digital signals). Fig. 1.1(a) shows the conceptual scheme of an ADC that includes the following components: an Anti-Aliasing Filter (AAF), a Sampling-and-Hold (S/H) circuit, a quantizer and a coder [Rosa02]. The operation of these blocks is illustrated in Fig. 1.1(b). First, the analog input signal, \( x_a(t) \), passes through the anti-aliasing filter, removing the spectral components above one half of the sampling frequency, \( f_s \), of the subsequent S/H. Otherwise, from the Nyquist’s sampling theorem [Oppe89], high frequency components of \( x_a(t) \) would be folded or aliased into the signal bandwidth, \( B_w \), thus corrupting the signal information. The resulting band-limited signal, \( x_{bl}(t) \), is sampled at a rate of \( f_s \) by the S/H circuit, thus yielding the discrete-time signal, \( x_{s,n} = x_{bl}(nT_s) \). Following the S/H, the quantizer maps the continuous range of amplitudes of \( x_{s,n} \) into a discrete set of levels. Finally, the coder assigns an unique binary number to each level providing the output digital data, \( y_{d,n} \).

As illustrated in Fig. 1.1(b) the fundamental processes involved in an ADC are: sampling and quantization. The sampling process performs the continuous-to-discrete time conversion of the input signal in time, whereas the quantization process performs the continuous-to-discrete conversion of the input signal in amplitude. These two transformations present inherent errors that limit the performance of an ADC, even assuming ideal components.

![Operation of an ADC](image)

**Figure 1.1:** Operation of an ADC. (a) Conceptual scheme. (b) Signal processing.
1.2.1 Sampling

Sampling imposes a limit on the bandwidth of the analog input signal. According to the Nyquist theorem, the minimum frequency, $f_s$, required for sampling a signal with no loss of information is twice the signal bandwidth, $B_w$, i.e. $f_N = 2B_w$, also called the Nyquist frequency. Based on this criterion, those ADCs in which analog signals are sampled at minimum rate ($f_s = f_N$) are called Nyquist-rate, or simply, Nyquist converters. Otherwise, if the ratio between $f_s$ and $f_N$, is larger than unity, the ADC is known as Oversampling Converter, and $M = f_s/f_N$ stands for the oversampling ratio.

One advantage of oversampling converters is that they simplify the requirements placed on the AAF. This is illustrated in Fig. 1.2. Note that the anti-aliasing filter for a Nyquist converter must have a sharp transition band, thus introducing phase distortion in signal components located near the cut-off frequency.

1.2.2 Quantization

Quantization itself also introduces a limitation on the performance of an ideal ADC. It degrades the quality of the input signal whose continuous-valued levels are mapped onto a finite number of discrete levels. In this process an error is generated, called quantization error. Contrary to the sampling process, the quantization of a DT signal is a non-reversible operation.

Fig. 1.3(a) shows the transfer characteristic of an ideal quantizer. This can be represented mathematically by a non-linear function as follows [Cand92],

$$y = g_q x + e_q(x)$$  \hspace{1cm} (1.1)

where $g_q$ denotes the slope of the line intersecting the code steps or quantizer gain; $e_q(x)$ stands for the quantization error. This error is a non-linear function of the input signal, $x$, as shown in Fig. 1.3(b). Note that, if $x$ is confined to the interval $[x_{min}, x_{max}]$, the quantization error is bounded by the interval $[-\Delta/2, \Delta/2]$, with $\Delta$ being the quantization step, defined as the separation between consecutive levels in the quantizer. For an $B$-bit quan-
tizer, $\Delta = X_{FS}/(2^B - 1)$, with $X_{FS}$ being the full-scale range of the quantizer (see Fig. 1.3(a)). For inputs outside of that interval, the absolute value of the quantization error grows monotonously. This situation is known as overloading of the quantizer.

1.2.3 Quantization white noise model

In order to evaluate the performance of an ideal quantizer, some assumptions are usually made on the properties of the quantization error. As shown in Fig. 1.3(b), $e_q(x)$ is strongly dependent on the input signal, $x$. Nevertheless, if $x$ varies randomly from sample to sample in the interval $[x_{\min}, x_{\max}]$, and the number of levels of the quantizer is large, it can be shown [Benn48] that the quantization error distributes uniformly in the range $[-\Delta/2, \Delta/2]$ with the rectangular probability density, $\rho_q(e_q)$, shown in Fig. 1.3(c), having a constant Power Spectral Density (PSD). Because of that, the quantization error can be modelled as an additive white noise source, $e_q$, as shown in Fig. 1.3(d), usually called quantization noise. As the total quantization noise power, $\sigma^2(e)$ is uniformly distributed in the range $[-f_s/2, f_s/2]$, its PSD equals

$$S_E(f) = \frac{\sigma^2(e)}{f_s} = \frac{1}{f_s} \Delta \int_{-\Delta/2}^{\Delta/2} e^2 de = \frac{\Delta^2}{12f_s}$$

and the in-band noise power, calculated as,

$$P_Q = \int_{-B_w}^{B_w} S_E(f) df = \frac{\Delta^2}{12M}$$

Figure 1.3: Ideal quantization process. (a) Ideal transfer characteristic. (b) Quantization error. (c) Probability density function of additive, white quantization noise. (d) Linear model of an ideal quantizer.
decreases with $M$ at a rate of $3\text{dB/octave}$ . This property is exploited by oversampling converters by using large values of $M$.

Strictly speaking, the white noise approximation is not valid for single-bit quantizers or comparators (very interesting in practice due to their simplicity). However, experience shows that the results obtained with this model are also applicable to the mentioned quantizers [Cand92].

1.2.4 Quantization noise shaping

An approach to further increase the accuracy of an ADC consists of reducing the error power within the signal band through the processing of the quantization error. Let us consider an $B$-bit quantizer with an oversampled input signal. If the oversampling ratio is large enough, with the signal only changing slightly from sample to sample, most of the changes in the quantization error happen at high frequencies —i.e., low-frequency components of consecutive samples of the quantization error are similar. Hence, low-frequency in-band components of the quantization error can be attenuated by subtracting the previous sample from the current one,

$$e_{\text{HP}}(n) = e(n) - e(n-1)$$  \hspace{1cm} (1.4)

Further reduction can be achieved by involving more previous error samples,

$$e_{\text{HP},1}(n) = e(n) - e(n-1)$$ \hspace{1cm} , 1st-or error proc.
$$e_{\text{HP},2}(n) = e(n) - 2e(n-1) + e(n-2)$$ \hspace{1cm} , 2nd-or error proc.
$$e_{\text{HP},3}(n) = e(n) - 3e(n-1) + 3e(n-2) - e(n-3)$$ \hspace{1cm} , 3rd-or error proc.
$$...$$ \hspace{1cm} ...

The procedure can be formulated in an unified manner in the $Z$-domain as

$$E_{\text{HP},L}(z) = (1 - z^{-1})^L \cdot E(z)$$  \hspace{1cm} (1.6)

showing that the processed error is a filtered version of the original. The filtering transfer function —often called Noise Transfer Function— is therefore

$$N_{\text{TF}}(z) = (1 - z^{-1})^L$$  \hspace{1cm} (1.7)

where $L$ denotes the order of the filtering realized on the quantization error [Rodr03].

For this transfer function
\[ |N_{TF}(e^{j\Theta})|^2 = |1 - e^{-j\Theta}|^{2L} = 2^{2L} \sin^2 \left( \frac{\Theta}{2} \right), \text{ with } \Theta = \frac{2\pi f}{f_s} = \frac{\pi f}{MB_w} \]  

(1.8)

Within the signal band \((f \leq B_w)\), \(\Theta \ll 1\) if \(M\) is large enough. Hence, the transfer function takes very small values in this range and the in-band power of the filtered quantization error results in

\[ P_Q = \int_{-B_w}^{+B_w} \frac{\Delta^2}{12f_s} |N_{TF}(f)|^2 df \approx \frac{\Delta^2}{12} \cdot \frac{\pi^{2L}}{(2L + 1)M^{(2L + 1)}} \]

(1.9)

that is much smaller than only applying oversampling —see (1.3).

Fig. 1.4 depicts the amplitude of \(N_{TF}\) for \(L = 1\). Note that the error reduction happens due to:

- the high-pass shape of the transfer function, that yields large in-band attenuation, pushing noise to high frequencies.
- the inverse dependence of the integration interval with \(M\).

Only the dark area at the bottom of Fig. 1.4 is integrated, so that the in-band error power is a small portion of the total thanks to the noise-shaping action — the smaller the larger \(M\) and/or \(L\). Note from (1.9) that the high non-linearity of the shaping results into a non-linear dependency of \(P_Q\) with \(M\) [Rio06].

### 1.3 Basics of \(\Sigma\Delta\) ADCs

\(\Sigma\Delta\) ADCs combine oversampling and noise shaping to reduce the quantization error within the signal band. These two strategies can be implemented by embedding a quantizer in a feedback loop as illustrated in Fig. 1.5(a)\(^\dagger\) [Rodr03]. This feedback system — known as a \(\Sigma\Delta\) Modulator (\(\Sigma\Delta M\)) — oversamples and quantizes the input signal, \(x\), and filters the quantization error, by shaping its PSD in such a way that most of its power lies outside of the signal band.

\(\dagger\) As will be discussed later on, \(\Sigma\Delta M\)s can be grouped into two groups: lowpass and bandpass, attending to the type of input signal. Fig. 1.5(a) corresponds to a lowpass \(\Sigma\Delta M\).
1.3.1 Understanding signal processing in a ΣΔM

In order to better understand the way in which a ΣΔM process the in-coming signal information as it is, whereas shapes the associated quantization error, let us consider the block diagram in Fig. 1.5(b). This system is the same as the one shown in Fig. 1.5(a) but does not contain any sampling process. Assuming that the quantizer in Fig. 1.5(b) is represented by the linear, additive noise model of Fig. 1.3(d), this system can be viewed as a two-input, \( x \) and \( e \), one output, \( y \), system, which in the frequency domain can be represented by:

\[
Y(f) = S_{TF}(f)X(f) + N_{TF}(f)E(f)
\]

(1.10)

where \( X(f) \) and \( E(f) \) are the Fourier transforms of the input signal and the quantization noise, respectively; \( S_{TF} \) and \( N_{TF} \) are the transfer functions of the input signal and quantization noise, respectively given by:

\[
S_{TF}(f) = \frac{g_q \cdot H(f)}{1 + g_q \cdot H(f)} \quad N_{TF}(f) = \frac{1}{1 + g_q \cdot H(f)}
\]

(1.11)

Note that, if the loop filter is designed such that \( H(f) \rightarrow \infty \) within the signal band, then \( S_{TF}(f) \rightarrow 1 \) and \( N_{TF}(f) \rightarrow 0 \), i.e, the input signal is allowed to pass whereas the quantization error is ideally cancelled. However, the error cannot be completely nulled in practice.
because $H(f)$ has a limited gain, and the PSD of the shaped quantization noise is given by:

$$S_Q(f) = S_E(f)|N_{TF}(f)|^2$$

(1.12)

and the shaped quantization noise in-band power is calculated as:

$$P_Q = \int_{\text{Signal band}} S_Q(f)df$$

(1.13)

The shaped quantization noise power is further reduced in the signal band thanks to the action of oversampling as discussed in Section 1.2.4. This can be implemented in different ways depending on the type of dynamics used for the loop filter, which can be either Continuous-Time (CT) or Discrete-Time (DT). The majority of reported $\Sigma\Delta$Ms use a DT loop filter, $H(z)$. Thus, assuming $g_q = 1$ and choosing $H(z)$ such that:

$$N_{TF}(z) = \frac{1}{1 + H(z)} = (1 - z^{-1})^L$$

(1.14)

the expression in (1.13) becomes the same as (1.9).

### 1.3.2 Performance metrics of $\Sigma\Delta$Ms

At this point, it is convenient to introduce the most important specifications commonly used to characterize the performance of oversampling $\Sigma\Delta$ converters.

- **Signal-to-Noise Ratio, SNR.** It is the ratio of the output power at the frequency of an input sinusoide to the uncorrelated in-band error power. Ideally, only quantization noise is accounted to compute $SNR$, expressed as:

$$SNR|_{\text{dB}} = 10\log_{10}\left(\frac{A_y^2}{2P_Q}\right)$$

(1.15)

where $A_y$ is the amplitude of the output sinusoide. In practice however, and due to non-idealities of the circuitry used to implement the converter, there are other error contributions —linear and non-linear— to the in-band error power, apart from quantization noise. To take into account all these errors, the **Signal-to-(Noise plus Distortion) Ratio (SNDR)** is usually defined.
Note that the SNR monotonously increases with \( A_x \). However, beyond a certain input amplitude, usually called overloading level, \( X_{OL} \), the quantizer input lies outside of the interval which produces the overloading of the latter and consequently a sharp drop is observed in the SNR curve. The value of the SNR at said input amplitude – the maximum value of SNR – is often called the \( SNR\text{-peak} \). This is illustrated in Fig. 1.6, that shows typical curves for the SNR and the SNDR of a \( \Sigma\Delta \)M as a function of the amplitude of a sinusoid signal applied at the modulator input. Usually, both curves coincide for small and medium input levels, since the distortion due to non-linear effects falls below the modulator noise floor. For large input levels, harmonic distortion becomes more evident, causing performance degradation and the deviation of the SNDR curve.

- **Dynamic range, \( DR \).** It is defined as the ratio of the output power at the frequency of an input sinusoid with maximum amplitude to the output power for a small input for which \( SNR = 0 \text{dB} \); i.e., so it cannot be distinguished from the error. Thus, ideally, a sinusoid with maximum amplitude at the converter input \( X_{FS}/2 \) will provide an output sinusoid sweeping the full-scale range \( Y_{FS} \) of the modulator quantizer, and hence

\[
DR_{\text{dB}} = 10\log_{10} \left( \frac{(Y_{FS}/2)^2}{2P_Q} \right) \quad (1.16)
\]

Considering the expression of \( P_Q \), given in (1.9), the above expression can be rewritten as:

\[
DR_{\text{dB}} \approx 20\log_{10}(2^B - 1) + 1.76 + 10\log_{10}\left( \frac{2L + 1}{\pi 2L} \right) + (2L + 1)10\log_{10}(M) \quad (1.17)
\]

which can be increased by properly combining the basic ingredients of \( \Sigma\Delta \)Ms, i.e: oversampling \( (M) \), noise-shaping filtering order \( (L) \) and the number of bits of the
internal quantizer ($B$). Each of these strategies have pros and cons which will be discussed later on.

- **Effective number of bits, ENOB.** The $DR$ of an ideal $N$-bit Nyquist-rate converter can be written as [Plas03]

$$DR_{\text{dB}} = 6.02N + 1.76$$  \hspace{1cm} (1.18)

Following the analogy, a similar expression can be established for $\Sigma\Delta$Ms

$$ENOB = \frac{DR_{\text{dB}} - 1.76}{6.02}$$  \hspace{1cm} (1.19)

where the $ENOB$ can be defined as the number of bits needed for an ideal Nyquist-rate converter to achieve the same $DR$ as the $\Sigma\Delta$ converter. Thus, the performance of oversampled $\Sigma\Delta$ converters and Nyquist-rate ADCs can be compared in simple way [Bose88].

To illustrate the ideal performance of $\Sigma\Delta$Ms, Fig. 1.7 plots $DR$ and $ENOB$ as a function of $M$ and $L$, considering a single-bit quantizer ($B = 1$). Note that for $M > 4$, the combined action of oversampling and noise-shaping considerably improve the performance of the modulator [Rio06].

**Figure 1.7:** Ideal performance of oversampled $\Sigma\Delta$ converters. $DR$ and $ENOB$ versus $M$ for different order $L$ of the modulator with $B = 1$ [Rio06].
1.3.3 Block diagram and components of a $\Sigma \Delta$ ADC

Because $\Sigma \Delta$Ms are feedback systems, the conceptual block diagram of Fig. 1.1 does not fit well to make a ADC based on the $\Sigma \Delta$M concept [Rodr03]. Indeed, the sampler and the quantizer of Fig. 1.1 are cascaded in an open loop configuration, as it is actually the case for a full Nyquist flash converter [Plas03]. Instead, the diagram of a $\Sigma \Delta$ ADC is better represented through Fig. 1.8, where Fig. 1.8(a) corresponds to DT-$\Sigma \Delta$ ADCs and Fig. 1.8(b) is for a CT-$\Sigma \Delta$ ADC. In both cases, low-pass signals are assumed to be processed. Otherwise, the filters involved must be changed from low-pass to band-pass transfer functions.

The diagram in Fig. 1.8 comprises three main blocks, whose operation in time and frequency domain is conceptually illustrated in Fig. 1.9 for a lowpass sign:

- **Anti-Aliasing Filter (AAF).** The function of this block, identical to that in Nyquist-rate ADCs, is attenuating the out-of-band components of the input signal in order to avoid aliasing when it is sampled. However, as already explained, the use of oversampling relaxes the attenuation requirements for this analog filter, because the frequency components of the input in the range $[B_w, f_s - B_w]$ do not fold within the baseband. Note that, in the case of CT-$\Sigma \Delta$ ADCs, the input signal could be either subject to AAF or feeds directly into the CT-$\Sigma \Delta$M without preceding any filtering. This can be done thanks to the implicit AAF which is embedded in CT-$\Sigma \Delta$Ms, as will be elaborated later.

![Diagram of a $\Sigma \Delta$ ADC](image)

**Figure 1.8:** Block diagram of an $\Sigma \Delta$ ADC. (a) DT-$\Sigma \Delta$ ADC. (b) CT-$\Sigma \Delta$ ADC.
- **Sigma-Delta Modulator ($\Sigma\Delta M$)**. It simultaneously performs the sampling and quantization of the in-coming signal. In addition, the quantization error is filtered by means of a noise-shaping technique. This, combined with oversampling, greatly enlarges the accuracy of the A/D conversion over that of the embedded quantizer as has been explained previously. Note that, DT-$\Sigma\Delta$Ms implement the sampling operation at the modulator input (see Fig. 1.8(a)), whereas CT-$\Sigma\Delta$Ms do it at the quantizer input and the loop filter is CT – see Fig. 1.8(b). Thus, the output signal is DT and a DT-to-CT transformation is needed to create the feedback signal, $y(t)$. The process of reconstruction this signal, by using proper output pulse shape of the embedded Digital-to-Analog Converter (DAC), plays a significant role on the overall CT-$\Sigma\Delta$M performance as will be discussed later [Ortm06][Rodr03]. In both cases, DT- and CT- ADCs, the output of the $\Sigma\Delta$M is a $B$-bit digital stream at $f_s$ sampling rate.

![Figure 1.9](image.png)

**Figure 1.9:** Illustration of the signal processing in a $\Sigma\Delta$ ADC [Rio06].
• **Error-Removal Filter + Decimator.** This is a purely digital block – and hence identical for both DT- and CT cases – that takes the high-frequency (oversampled) digital stream as input, removes its high-frequency components through high-selectivity digital filtering, and *decimates* it to reduce the sampling frequency down to the Nyquist frequency. The result is the input signal encoded at the Nyquist rate and with an equivalent resolution given by (1.19) [Rodr03].

Out of these blocks, the one influencing most the ADC performance is the ΣΔM, basically because it is the ultimate responsible for the accuracy in the A/D conversion. Thus, from now on, we will hence focus on this block – although keeping in mind that a ΣΔ ADC is more than just its ΣΔM [Rio06].

1.3.4 **Classification of ΣΔMs**

A large number of ΣΔM architectures have been reported in literature that implement some (or all) the following, non-exclusive, strategies to improve $DR$:

- **Increasing the loop filter order, $L$.** According to (1.17), for a given $M$, the increase in $DR$ when increasing the modulator order $L$ in one, leads to

$$
\Delta DR_{\text{dB}} \approx 10 \log_{10} \left[ \frac{2L + 3}{2L + 1} \cdot \left( \frac{M}{\pi} \right)^2 \right]
$$

(1.20)

However, the use of high-order shaping (usually $L > 3$) gives rise to stability problems. These problems can be circumvented using different techniques at the price of reducing $DR$ as compared with the ideal value given by (1.17) [Nors97].

- **Increasing the oversampling ratio, $M$,** leads to an increase of $(L + 1/2)$ bit/octave in the effective resolution of the modulator. However, high values of $M$ are limited in practice for wideband signals, because of the prohibitive sampling frequencies required, which force the circuitry to operate very fast, with the subsequent penalty in power consumption.

- **Increasing the number of bits of the internal quantizer, $B$,** leads to an increase of 6dB (1 bit) in the modulator $DR$ for each extra bit in the quantizer [Geer02]. The problem associated with using $B > 1$, is that a multi-bit DAC is required in the feedback loop of the modulators, that – on the contrary to single-bit ones, with only two levels – is not inherently linear. Thus, in practice the linearity in the DAC equals that wanted for the ΣΔM [Rio06].

The above mentioned strategies can be combined in many different ways, giving rise to a pleyade of ΣΔM topologies reported in literature and that can be grouped attending to dif-
different classification criteria [Rodr03]:

- The nature of the signals being handled: lowpass $\Sigma\Delta$Ms versus bandpass $\Sigma\Delta$Ms.

- The number of quantizers employed. $\Sigma\Delta$Ms employing only one quantizer are called single-loop structures. Those employing several quantizers have different names: cascade, dual-quantization, truncation-feedback, etc.

- Type of circuitry employed, primitives available in the fabrication technology, voltage supply, etc. Most of the reported DT implementations employ switched-capacitor circuits with high-quality passive capacitors – mixed-signal technology options. Others employ the passive capacitor structures available on standard CMOS technologies. Others employ active capacitors built with MOS transistors. Others employ switched-current circuits realized only with MOS transistors, etc.

- The type of dynamics for the loop filter. The majority of reported $\Sigma\Delta$Ms used DT loop filters. However, the increasing demand for even faster ADCs has motivated the use of CT loop filters, which combined with a DT quantizer (see Fig. 1.8(b)) leads to the so-called CT-$\Sigma\Delta$Ms – which are the main objective of this thesis.

Describing all possible $\Sigma\Delta$M architectures derived from previous classification goes beyond the scope of this thesis. A detailed study of them can be found in many papers and books [Nors97][Mede99][Schr05][Rio06][Ortm06]. Instead, we will focus on those aspects which are specific to CT-$\Sigma\Delta$Ms.

### 1.4 Continuous-Time $\Sigma\Delta$ Modulators

Although early implementations of $\Sigma\Delta$Ms were based on the use of CT, discrete-component, loop filters [Inos62][Inos63], the increasing development of SC circuits and their suitability to implement robust and linear filters using standard CMOS technologies, caused that the immense majority of $\Sigma\Delta$Ms were implemented using DT circuit techniques and particularly SC circuits [Schr05]. However, in the last years there has been a resurgence of CT $\Sigma\Delta$Ms prompted by the increasing demand for high data-rate ADCs [Ortm06]. As it will be described in this section, CT $\Sigma\Delta$Ms have the potential to operate at higher sampling rates with lower power consumption than their DT counterparts and, in addition, they implement an implicit AAF leading to a more compact implementation.

Looking at both topologies depicted in Fig. 1.8, one can see a few, but important, differences among DT- and CT-$\Sigma\Delta$Ms. Apart from the obvious and already mentioned difference between the nature of the loop filter, the most significant difference is related to the point where the $S/H$ process takes place, which possibly constitutes the key advantage of CT-$\Sigma\Delta$Ms [Ortm06]. In the case of CT-$\Sigma\Delta$, $S/H$ is realized inside the $\Sigma\Delta$M loop, which implies three fundamental benefits: relaxed dynamic (settling) requirements for the loop fil-
ter circuitry; implicit antialiasing filtering and elimination of the input switches. However, as both DT- and CT- signals are involved, the mathematical analysis (and consequently the synthesis) of CT-ΣΔMs becomes much more difficult than in the case of DT-ΣΔMs.

Both theoretical and practical issues associated to CT-ΣΔMs have been addressed in several monographs [Bree01][Cher00][Enge99][Shoa95][Rodr03]. Their claimed pros can be summarized as:

- **Extra anti-aliasing filter can be avoided**, or at least, the required specifications of the front-end AAF can be relaxed. Instead the CT loop filter $H(s)$ can be exploited to this purpose as will be explained in more detail in Section 1.4.4.

- **Less impact of errors caused during sampling operation.** This is a consequence of the fact that sampling is not realized at the input, where its error cannot be attenuated, but within the modulator loop. Indeed, one of the main benefits is avoiding the use of sampling switches, which among other advantages, allows loop filters to operate with low voltage supply. On the contrary, sampling switch-on resistance is an important limiting factor in SC implementations, and as the supply voltage reduces with technology downsampling, making necessary the use of circuit techniques like clock boosting, that introduce additional parasitics.

- **No “settling” error at the loop filter circuitry.** In DT circuits, signals must settle to their steady-state values according to dynamic features of the circuitry [Rio06]. Complete settling requires infinite time. In practice settling process must last until the influence of the circuit time-constants becomes negligible. In contrast, CT-ΣΔM present larger operation speed. This is inherent to the operation of CT circuits, where circuit dynamics is not a parasitic (as it happens for DT circuits), but a design primitive.

- **No sampling of the $k \cdot T/C$ (thermal) noise at the input capacitors** – a by-product of the location of the sampling operation. Therefore, the in-band noise power is lower than in DT-ΣΔMs where a large amount of thermal noise is fold back into the signal band, constituting a fundamental resolution limit [Ortm06].

- **Reduced digital noise** coupling since switching process is attenuated by the action of the modulator feedback, in the same way as for the quantization noise.

On the other hand, the main cons of CT-ΣΔMs are the following:

- **Very involved dynamic** due to the combination of non-linearity, continuous-time and discrete-time signals. This makes the mathematics of the CT-ΣΔM system much more complicated than for DT-ΣΔMs, which has a natural connection with their circuit-level implementation, through the use of the Z-transform of the finite
difference equations describing the behavior of the system.

- **Larger impact of circuit non-linearities.** This is inherent to CT circuits. These circuits require voltage-to-current transformation, and this yields nonlinear errors. These errors may have significant impact, particularly those appearing at the very input because they are not attenuated by the modulator feedback loop.

- **Time constant tuning is needed** for correct loop filtering. This is also inherent to CT circuits where time constants are given as the product of two un-correlated parameters.

- **Time uncertainty (or clock “jitter”) plays a significant role** because it maps directly onto errors in the feedback signal $y(t)$. This is not the case of DT implementations, which thanks to their sample-data nature, presents relaxed sensitivity to timing variations or delays within the loop filter, both of which constitute a strong limitation in CT-$\Sigma$ΔMs [Ortm06].

### 1.4.1 Approximated linear analysis of CT-$\Sigma$ΔMs

In order to understand basics and fundamental concepts of the signal processing in CT-$\Sigma$ΔMs, let us consider the conceptual block diagram shown in Fig. 1.10. For the analysis that follows, it will be considered that the feedback DAC has a gain of approximately unity in the signal band$^{\dagger2}$. Under this assumption and considering a linear model for the quantizer, the modulator in Fig. 1.10(a) can be transformed into the one depicted in Fig. 1.10(b).

![Figure 1.10](image)

**Figure 1.10:** (a) Conceptual block diagram of a CT-$\Sigma$ΔM. (b) Simplified model.

$^{\dagger2}$The effect of actual DAC waveform will be analysed in next section.
A basic analysis of Fig. 1.10(b) shows that the frequency transform of the modulator output and the loop filter input are respectively given by:

\[ U_i = g_1X(f) - g_1'Y(f) \]
\[ Y(f) = E_q(f) + g_qB(f) \]  

(1.21)

where \( E_q(f) \) and \( B(f) \) are respectively the frequency-domain transform of the quantization error, \( e(t) \), and the quantization input, \( b(t) \).

On the other hand, the sampling operation can be mathematically expressed as:

\[ b(t) = \hat{u}_o(t) \otimes g_{sh}(t) \]  

(1.22)

where the operator \( \otimes \) stands for the convolution, \( \hat{u}_o(t) \) is the sampled version of the integrator output, \( u_o(t) \), given by:

\[ \hat{u}_o(t) = \sum_n u_o[nT_s] \delta(t-nT_s) \]  

(1.23)

and \( g_{sh}(t) \) is the impulsive response of the S/H block, given by:

\[ g_{sh}(t) = \begin{cases} 
1 & 0 \leq t \leq T_s \\
0 & t > T_s, t < 0 
\end{cases} \]  

(1.24)

where \( T_s \) is the sampling time.

Applying the Fourier-transform of (1.23) and (1.24) and replacing the result in (1.22), we obtain that:

\[ B(f) = \text{sinc}(fT_s) \sum_n U_o(f-nf_s) \]  

(1.25)

where \( \text{sinc}(x) \equiv \sin(x)/x \). Note that, in those cases where \( M \gg 1 \), \( fT_s \ll 1 \) and hence,

\[ \text{sinc}(fT_s) \approx 1 - \frac{\pi^2}{6}(f/f_s)^2 + \frac{\pi^4}{120}(f/f_s)^4 \approx 1 \]  

(1.26)

Assuming a band-limited input signal, i.e the input frequency, \( f_i \in (0, B_w) \), and neglecting the spectral components of \( y(t) \) above \( f_s/2 \), it can be shown that:
\[ Y(f) \equiv S_{TF}(f) \cdot X(f) + N_{TF}(f) \cdot E_q(f) \]  \hspace{1cm} (1.27)

where

\[ S_{TF}(f) = \frac{g_1g_q H(f)}{1 + g'_1g_q H(f)} \quad \text{and} \quad N_{TF}(f) = \frac{1}{1 + g'_1g_q H(f)} \]  \hspace{1cm} (1.28)

which are the same expressions as those obtained in (1.11) with \( g_1 = g'_1 = g_q = 1 \).

### 1.4.1.1 First-order CT-ΣΔM

As discussed earlier, the loop filter must be designed such that \( H(f) \to \infty \) within the signal band. The simplest CT function that verifies this condition is:

\[ H(f) = \frac{1}{2\pi f\tau} \]  \hspace{1cm} (1.29)

where \( \tau \) stands for the time constant of the circuit implementing \( H(f) \). Thus, replacing \( H(f) \) in (1.27) and (1.28) gives:

\[ Y(f) = \frac{g_1g_q}{g'_1g_q + 2\pi f\tau} \cdot X(f) + \frac{2\pi f\tau}{g'_1g_q + 2\pi f\tau} \cdot E_q(f) \]  \hspace{1cm} (1.30)

Assuming \( g_1 = g'_1 \) and \( g_q = 1/g_1 \) and taking the limit of the above expression for \( f \cdot \tau \to 0 \), the Fourier transform of the modulator output can be written as:

\[ Y(f) \equiv X(f) + 2\pi f\tau \cdot E_q(f) \]  \hspace{1cm} (1.31)

that corresponds with the Fourier Transform of the input signal plus a shaped version of the quantization error.

The in-band noise can be derived from (1.13) and (1.31), giving:

\[ P_Q = \frac{\Delta^2}{12f_s} \cdot \frac{\pi \tau B_w/2 - \arctg(\pi \tau B_w/2)}{\pi \tau} \]  \hspace{1cm} (1.32)

It is usually a common situation in CT-ΣΔMs to make \( \tau \approx T_s = 1/f_s \) [Ortm06], because this maximizes the performance of the modulator. Fig. 1.11 illustrates this by plotting the SNR vs. \( \tau \) in a second-order (\( L = 2 \)) CT-ΣΔM, for different values of the oversampling ratio. Note that, the maximum value of the SNR is achieved when \( \tau \approx T_s \). Taking this into account and assuming the Taylor series expansion for \( M \approx \pi \), the above expression can
be simplified as:

\[
P_Q = \frac{\Delta^2}{12} \cdot \frac{\pi}{M} - \left[ \frac{(\pi/M) - (1/3)(\pi/M)^3 + (1/5)(\pi/M)^5}{\pi} \right] \approx \frac{\Delta^2 \pi^2}{3M^3} \tag{1.33}
\]

which corresponds to the in-band noise power of a \( \Sigma \Delta M \) with \( L = 1 \) and \( B = 1 \).

1.4.1.2 Second- and \( L \)th-order CT-\( \Sigma \Delta M \)

The above approximated analysis can be extended to 2nd- and \( L \)th-order CT-\( \Sigma \Delta M \)s. Let us consider the modulator in Fig. 1.12(a), which implements a 2nd-order loop filter. Assuming that \( \tau \cdot f_s = 1 \), \( g_q = 1/g_2g_1' \) and that \( H(f) \) has the same expression as (1.29), the frequency transform of the modulator output can be written as:

![Figure 1.11: SNR vs. \( \tau \) in a 2nd-order CT-\( \Sigma \Delta M \) for different values of \( M \).](image)

(a)

(b)

![Figure 1.12: Generic single-loop CT-\( \Sigma \Delta M \). (a) 2nd-order. (b) \( L \)th-order.](image)
\[ Y(f) = \frac{g_1}{g'_1} \cdot X(f) + (2\pi f f_0)^2 E_q(f) \]  \tag{1.34}

In a more general case of a \( L \)th-order loop filter like the one shown in Fig. 1.12(b), the following expression is obtained:

\[ Y(f) \approx \frac{g_1}{g'_1} \cdot X(f) + \left(1/H(f)\right)^L \cdot E_q(f) = \frac{g_1}{g'_1} \cdot X(f) + (2\pi f f_0)^L \cdot E_q(f) \]  \tag{1.35}

Following the same procedure as in Section 1.4.1.1, the in-band noise power can be obtained, giving the same result as in (1.9).

### 1.4.2 DT-to-CT equivalence and the impulse-invariant transformation

The above analysis assumed that \( M \approx 1 \) and an ideal DAC impulsive response. However, in a CT-\( \Sigma \Delta \)M the output signal must be transformed from DT- to CT- in the feedback loop. This signal reconstruction is very critical and has a significant impact on the overall behaviour of the modulator [Shoa95]. There are a pleyade of DAC waveforms that can be used in CT-\( \Sigma \Delta \)Ms. Fig. 1.13 shows a survey of the different possibilities including the nomenclature used for the feedback waveforms – extracted from [Ortm06]. Among others the most commonly used DACs incorporate rectangular feedback pulses of basically three types: Non-Return-to-Zero (NRZ) (Fig. 1.13(a)), Return-to-Zero (RZ) (Fig. 1.13(b)) and Half-delay Return-to-Zero (HRZ) (Fig. 1.13(c)). Their impulsive response can be written as:

\[
DAC(t) = \begin{cases} 1, & p_1 T_s \leq t \leq p_2 T_s \\ 0, & \text{io} \end{cases}
\]  \tag{1.36}

and their corresponding Laplace S-transform is given by:

\[
DAC(s) = \frac{e^{-sp_1 T_s}}{s} - \frac{e^{-sp_2 T_s}}{s} \begin{cases} p_1 = 0 & p_2 = 1 & \text{for NRZ} \\
p_1 = 0 & p_2 = 1/2 & \text{for RZ} \\
p_1 = 1/2 & p_2 = 1 & \text{for HRZ} \end{cases}
\]  \tag{1.37}

Let us consider the above transfer function for the DAC and the basic block diagram of a CT-\( \Sigma \Delta \)M shown in Fig. 1.10. Because of the presence of a S/H inside the loop, the overall (open) loop filter of the modulator is indeed a DT function as it illustrated in Fig. 1.14. Note that, as the signal travels across the open loop path, it is first transformed into a CT signal by the DAC. Assuming the DAC shapes in (1.36) the following feedback waveform is obtained per each period,
where \( u(\bullet) \) denotes the unit step waveform and \( p_1 \) and \( p_2 \) are given in (1.37) for the three basic DAC shapes. After this transformation, the signal shaped by the CT filter \( H(s) \), which in Laplace domain can be expressed as,

\[
Z(s) = H(s) \cdot \frac{-s \cdot p_1 \cdot T_s - e^{-s \cdot p_2 \cdot T_s}}{s}
\]  

(1.39)

Finally, the signal \( z(t) \) is sampled, which in time domain can be expressed as:

\[
z(n) = z(t) \cdot \sum_{n=0}^{\infty} \delta(t - n \cdot T_S)
\]  

(1.40)

**Figure 1.13:** Common DAC feedback impulse responses [Ortm06]. Rectangular waveforms: (a) Non-Return-to-Zero (NRZ); (b) Return-to-Zero (RZ); (c) Half-Return to Zero (HRZ). Decaying waveforms: (d) Linear decaying; (e) Quadratic decaying; (f) Exponential decaying, Switched-Capacitor Resistor (SCR). Other waveforms: (g) Cosine. (h) Non-linear slope. (i) Linear slope.
where $\delta(\bullet)$ is the Dirac delta. By combining previous expressions, the transfer function of the overall feedback path is calculated as:

$$H(z) = Z \left[ L^{-1}[DAC(s) \cdot H(s)] \cdot \sum_{n=0}^{\infty} \delta(t-n \cdot T_s) \right]$$

(1.41)

where $Z(\bullet)$ stands for the Z-transform operator, $L(\bullet)$ stands for the Laplace-transform operator.

Based on the equivalent DT loop filter transfer function shown in (1.41), the most usual procedure to design CT-\Sigma\DeltaMs consists of, first, matching this equivalent filter with a reference DT loop filter chosen to fulfill specs; then, solving for the coefficients of the CT filter; and finally implementing this filter by circuits. Careful choice of the CT filter structure is needed to have sufficient degrees of freedom to implement the reference DT loop filter [Enge99].

### 1.4.3 Direct synthesis method

An alternative method for the design of the loop filter uses the desired NTF as a starting point, just in the same manner as for the DT case. Usually, an inverse Chebychev distribution of the NTF zeroes is considered because it has advantages in terms of SNR and stability [Risb94]. Once the desired NTF has been chosen, the necessary loop filter can be derived from the linearized model [Bree01]. As an illustration, Fig. 1.15(a) shows a third-order single-loop CT-\Sigma\DeltaM which has been synthesized using a direct synthesis method [Ortm06]. The scaling coefficients, $k_i$, have been obtained considering a Chebyshev type II distribution of NTF zeroes, giving $\{k_1, k_2, k_3, \gamma\} = \{0.51, 0.97, 1.95, 0.04/(k_2 k_3)\}$. The corre-

![Figure 1.14: Equivalent DT transfer function in CT-\Sigma\DeltaMs.](image-url)
sponding output spectrum is shown in Fig. 1.15(b), considering a sampling frequency of \( f_s = 100\text{MHz} \), a NRZ DAC waveform and a 3-bit quantizer.

There are two major drawbacks to the direct synthesis method:

- Previous knowledge of discrete time modulators is not reused. This rises questions about stability.

- Simulations are harder due to the fact that every simulation has to be done in continuous time.

The above reasons have prompted that most implemented CT-\( \Sigma \Delta \)M ICs are synthesized using a DT-to-CT method, including both single-loop and cascade \( \Sigma \Delta \)M architectures [Bree04]. However, as demonstrated in this thesis, using the direct synthesis method, more robust and efficient cascade architectures can be obtained as compared to DT-to-CT transformation.

**Figure 1.15:** 3rd-order CT-\( \Sigma \Delta \)M with Chebyshev loop filter approximation [Ortm06]. (a) Block diagram. (b) Output spectrum.
1.4.4 Implicit anti-aliasing filtering

As stated previously, CT-ΣΔMs have the advantage of including an implicit AAF. This property has been analytically demonstrated in previous works [Cand85][Shoa95], and can be explained as follows. Let us consider the conceptual diagram of a CT-ΣΔM in Fig. 1.14(a). This block diagram can be transformed in the one shown in Fig. 1.16(a), in which the loop filter and the implicit S/H block are relocated across the summation point and placed in front of the CT-ΣΔM and the feedback loop filter. Note that the resulting Forward Filter (FF), \( FF(s) \), is not necessarily identical to the Feedback loop filter, \( LF(s) \). This is a direct consequence of the fact that in a CT-ΣΔM, the input signal is CT and the output signal is DT. Therefore, it is not possible to define a straight Z-domain or S-domain STF [Cand85][Shoa95][Ortm06].

The block diagram shown in Fig. 1.16(a) reveals that, as was discussed in previous sections, a CT-ΣΔM behaves as a DT-ΣΔM due to the sampling operation in the feedback path, but with an additional CT Forward Filter, \( FF(s) \). So, the corresponding STF frequency response can be obtained from the block diagram in Fig. 1.16(b). From this figure, the AAF can be approximately expressed as [Shoa95]:

\[
F_{AAF}(\omega) = \frac{FF(j\omega)}{FF(e^{j\omega})}
\]

(1.42)

where \( FF(j\omega) \) is the FF filter of the CT-ΣΔM and \( FF(e^{j\omega}) \) its DT equivalent. The above equation shows that the AAF-behaviour can be defined for different loop filter characteristics, i.e low-pass, band-pass, etc [Ortm06].

\[\begin{align*}
\begin{array}{c}
\text{Figure 1.16: (a) Equivalent representation of a CT-ΣΔM and (b) Implicit AAF.}
\end{array}
\end{align*}\]
As an illustration, the aliasing behaviour of a 2nd- and 3rd-order CT-ΣΔMs shown in Fig. 1.17 is discussed. The original CT FF filter for both architectures is given by:

\[
FF_{2nd-ord}(s) = k_{in}\left(\frac{f_s}{s}\right)^2 \quad FF_{3rd-ord}(s) = k_{in}\left(\frac{f_s}{s}\right)^3
\]  

(1.43)

Figure 1.17: Implicit AAF in: (a) 2nd-order CT-ΣΔM- (b) 3rd-order CT-ΣΔM.
and the equivalent DT FFs are:

\[
FF_{2\text{nd-ord}}(z) = k_{\text{in}} \left( \frac{z^{-1}}{1 - z^{-1}} \right)^2 \\
FF_{3\text{rd-ord}}(z) = k_{\text{in}} \left( \frac{z^{-1}}{1 - z^{-1}} \right)^3
\]  

(1.44)

Inserting the above expressions in (1.42) and after a few simplifications we obtain the AAF transfer function for the 2nd- (\(L = 2\)) and 3rd-order (\(L = 3\)) CT-\(\Sigma\Delta\)M, given by:

\[
F_{\text{AAF}}(\omega) = \left| \frac{f_s/(j\omega)(1 - e^{-j\omega})}{e^{-j\omega}} \right|^L \approx \left[ \sin c \left( \frac{\pi f}{f_s} \right) \right]^L
\]

(1.45)

which consists of the well-known sinc-function, defined as \(\sin c(x) \equiv \sin(x)/x\). The effect of AAF is better illustrated by simulations as shown in Fig. 1.18, where the output spectra of a 2nd-order DT- and CT-\(\Sigma\Delta\)Ms are plotted considering two input sinewave signals, one in-band and the other out-of-band. It can be noted the effect of the implicit AAF in the CT-\(\Sigma\Delta\)M, causing a notable attenuation (almost 60dB) of the aliased signal, as compared to the DT case.

1.5 DT-to-CT synthesis methods and basic CT-\(\Sigma\Delta\)M architectures

As stated in previous section, most CT-\(\Sigma\Delta\)Ms are synthesized starting from an equivalent DT-\(\Sigma\Delta\)M that fulfills the required specifications and applying a DT-to-CT transformation. The most common transformation method is the impulsive-invariant – explained in

![Figure 1.18](image-url)

**Figure 1.18**: Antialiasing filtering in 2nd-order CT-\(\Sigma\Delta\)Ms for an input signal at \(f_{\text{in}} = 1\text{kHz}\) and a "non-desired" signal at \(f_s = 5\text{kHz}\) with \(f_s = 1\text{MHz}\). (a) DT. (b) CT.
Section 1.4.2. This method allows the design of a CT loop filter, which together with a specific DAC transfer function, $DAC(s)$, exactly matches the noise-shaping behaviour of the original DT loop filter. Thus, for given specific $\Sigma$ΔM architecture, the DT-to-CT transformation can be done using (1.41) for the corresponding loop filter [Ortm06]. Most DT loop filters can be divided into partial fractions of type, $1/(z - z_k)$, for the low-pass case, and of type, $1/(z^2 + z_k^2)$, for the band-pass case. For that reason, it is very useful to know the $S$-$Z$ equivalents of basic LP and BP $Z$-domain transfer functions as summarized in Table 1.1 [Cher00][Ortm06], where rectangular DAC waveforms are considered. Based on the equivalence of basic transfer functions, more complex loop filter transfer functions can be synthesized as will be illustrated later on.

In addition to the above-mentioned impulse-invariant transformation method, there are other, less-usual, DT-to-CT transformation methods that have been used to synthesize CT-$\Sigma$ΔMs: the modified Z-transformation [Shoa95][Abus02] and the state-space representation method [Schr96][Olia03]. Both methods are summarized below.

<table>
<thead>
<tr>
<th>Z-domain</th>
<th>S-domain</th>
</tr>
</thead>
<tbody>
<tr>
<td>$\frac{z^{-1}}{1-z^{-1}}$</td>
<td>$\frac{\omega_o}{s}$, where $\omega_o = \frac{f_s}{p_2-p_1}$</td>
</tr>
<tr>
<td>$\frac{z^{-2}}{(1-z^{-1})^2}$</td>
<td>$\frac{\omega_1s + \omega_o}{s}$, where $\omega_o = \frac{f_s^2}{p_2-p_1}; \omega_1 = \frac{1}{2}\frac{f_s(p_1 + p_2 - 2)}{p_2 - p_1}$</td>
</tr>
<tr>
<td>$\frac{z^{-3}}{(1-z^{-1})^3}$</td>
<td>$\frac{\omega_2s^2 + \omega_1s + \omega_o}{s}$, where $\begin{cases} \omega_o = \frac{f_s^2}{p_2-p_1}; \omega_1 = \frac{1}{2}\frac{f_s(p_1 + p_2 - 3)}{p_2 - p_1} \ \omega_2 = \frac{1}{12}\frac{f_s(p_2(p_2-9) + p_1(p_1-9) + 4p_1p_2 + 12)}{p_2 - p_1} \end{cases}$</td>
</tr>
</tbody>
</table>

**Bandpass CT-$\Sigma$ΔMs**

<table>
<thead>
<tr>
<th>Z-domain</th>
<th>S-domain</th>
</tr>
</thead>
<tbody>
<tr>
<td>$\frac{z^{-1} \cdot (1-z^{-1})}{1+z^{-2}}$ (NRZ)</td>
<td>$\frac{\omega_o \cdot s}{s^2 + \omega_o^2}$</td>
</tr>
<tr>
<td>$\frac{1-\frac{\sqrt{2}}{2}}{1+z^{-2}} \cdot \frac{z^{-1} - (\frac{\sqrt{2}}{2} \cdot z^{-2})}{1} (RZ)$</td>
<td></td>
</tr>
<tr>
<td>$\frac{\sqrt{2}}{2} \cdot \frac{z^{-1} - (1-\frac{\sqrt{2}}{2} \cdot z^{-2})}{1+z^{-2}}$ (HRZ)</td>
<td></td>
</tr>
</tbody>
</table>
1.5.1 Modified Z-transformation method

The modified Z-transform method is based on the general modified Z-transform, that allows to calculate the DT system behaviour at all instants of time. Thus, in order to find out the equivalent CT loop filter for a certain modulator architecture with a certain feedback DAC pulse shape, the DT loop filter transfer function is computed and compared with the original DT loop filter function, similarly to the case of impulse invariant method, giving the following equivalence [Ortm06]:

\[ H(z) = \sum_i Z_{m_i} \{ H(s) DAC(s) \} \] (1.46)

where \( m_i \) is the characteristic parameter of the modified Z-transform. The value of \( m_i \) is normalized to the sampling period and bounded between, \( 0 < m_i < 1 \), whereas the extremes 0 confirm to the previous sample instant and 1 to the next [Ortm06]. Thus, assuming a rectangular DAC waveform, (1.46) can be expressed as:

\[ H(z) = \sum_i \text{Re} \left( \frac{H(s)}{s} \cdot \frac{e^{m_1 T_s s}}{z - e^{-m_1 T_s s}} \right) - \sum_i \text{Re} \left( \frac{H(s)}{s} \cdot \frac{e^{m_2 T_s s}}{z - e^{-m_2 T_s s}} \right) \] (1.47)

where \( m_1 = 1 - t_d/T_s \); \( m_1 = 1 - (t_d + \tau)/T_s \); \( t_d \) and \( \tau \) are, respectively, the time delay and pulse width of the DAC waveform; \( p_i \) are the poles of \( H(s)/s \) and \( \text{Re}(x) \) stands for the residue of \( x \) [Shoa95][Abus02].

Generally speaking, for every time instant in which the CT loop filter changes its behaviour, an additional delay factor is introduced. This is the role played by coefficients \( m_1 \) and \( m_2 \) in (1.47). As an illustration of the modified Z-transformation, Table 1.2 shows several usual examples of S-domain transfer functions and their corresponding modified transforms [Ortm06].

<table>
<thead>
<tr>
<th>S-domain</th>
<th>Zm-domain equivalent</th>
</tr>
</thead>
<tbody>
<tr>
<td>( \frac{1}{s^2} )</td>
<td>( \frac{m T_s}{z - 1} + \frac{T_s}{(z - 1)^2} )</td>
</tr>
<tr>
<td>( \frac{1}{s(s + s_k)} )</td>
<td>( \frac{1}{s_k} \left( \frac{1}{z - 1} - \frac{e^{-s_k m T_s}}{z - e^{-s_k T_s}} \right) )</td>
</tr>
<tr>
<td>( \frac{1}{s^3} )</td>
<td>( \frac{T_s^2}{2} \left[ \frac{m^2}{z - 1} + \frac{2m + 1}{(z - 1)^2} + \frac{2}{(z - 1)^3} \right] )</td>
</tr>
<tr>
<td>( \frac{1}{s^2 (s + s_k)} )</td>
<td>( \frac{1}{s_k} \left( \frac{s_k m T_s - 1}{z - 1} + \frac{s_k T_s}{(z - 1)^2} + \frac{e^{-s_k m T_s}}{z - e^{-s_k T_s}} \right) )</td>
</tr>
</tbody>
</table>
1.5.2 State-space representation method

Let us consider the conceptual block diagram shown in Fig. 1.14. Using the impulse-invariant transformation [Proa98], the DT equivalent of the loop filter transfer function can be written as:

\[
H(z) = \frac{n(L-1)z^{(L-1)} + \cdots + n_1 z + n_0}{d_L z^{L} + d_{L-1} z^{(L-1)} + \cdots + d_1 z + d_0}
\] (1.48)

where \(n_i\) and \(d_i\) are function of the coefficients of the original CT modulator loop filter, \(H(s)\). Therefore, \(N_{TF}(z)\) can be derived from (1.48) as:

\[
N_{TF}(z) = \frac{1}{1 + H(z)} = \frac{d_N z^L + d_{N-1} z^{L-1} + \cdots + d_1 z + d_0}{d_L z^{L} + (d_{L-1} + n_{L-1}) z^{L-1} + \cdots + (d_1 + n_1) z + (d_0 + n_0)} = \frac{d_L + d_{L-1} z^{-1} + \cdots + d_1 z^{-(L-1)} + d_0 z^{-L}}{d_L + (d_{L-1} + n_{L-1}) z^{-1} + \cdots + (d_1 + n_1) z^{-(L-1)} + (d_0 + n_0) z^{-L}}
\] (1.49)

Fig. 1.19 shows the transpose of the Direct II implementation of (1.49) [Proa98]. This block diagram does not have any direct correspondence with the physical implementation of the modulator and is only used to represent the relationship between the input \(e(n)\), output \(q(n)\) and state variables of \(N_{TF}(z)\). This formulation is known as the state-space representation of \(N_{TF}(z)\) and can be implemented by the block diagram in Fig. 1.20, which is described by the following finite difference equations [Proa98]:

**Figure 1.19:** Transpose of the Direct II implementation of \(N_{TF}(z)\).

**Figure 1.20:** State-space representation of \(N_{TF}(z)\).
\[ v(n+1)_0 = \overline{F}_0 \cdot v(n)_0 + \overline{p}_0 \cdot e(n) \]
\[ q(n) = \overline{g}_0^T \cdot v(n)_0 + e(n) \]

(1.50)

where \( \overline{F}_0 \) is the state matrix, \( \overline{v(n)_0} \) is the \( L \times 1 \) state vector, \( \overline{p}_0 \) and \( \overline{g}_0 \) are \( L \times 1 \) vectors, respectively given by:

\[
\overline{F}_0 = \begin{bmatrix}
0 & 0 & 0 & \ldots & 0 & \frac{n_0 + d_0}{d_L} \\
1 & 0 & 0 & \ldots & 0 & \frac{n_1 + d_1}{d_L} \\
0 & 1 & 0 & \ldots & 0 & \frac{n_2 + d_2}{d_L} \\
0 & 0 & 1 & \ldots & 0 & \frac{n_3 + d_3}{d_L} \\
\ldots & \ldots & \ldots & \ldots & \ldots & \ldots \\
0 & 0 & 0 & \ldots & 1 & \frac{n_{L-1} + d_{L-1}}{d_L}
\end{bmatrix}
\]

\[
\overline{p}_0 = \begin{bmatrix}
n_0 \\
n_1 \\
n_2 \\
\vdots \\
n_{L-1}
\end{bmatrix}
\]

\[
\overline{g}_0 = \begin{bmatrix}
0 \\
0 \\
0 \\
\vdots \\
1
\end{bmatrix}
\]

(1.51)

Equation system (1.50) can be solved recursively to find the relation between the initial state \( v(0)_0 \), previous inputs \( e(k) \), current input \( e(n) \) and output \( q(n) \) of the system [Proa98].

### 1.5.3 Basic CT-ΣΔM architectures

The DT-to-CT transformation methods described in previous sections have been used extensively to synthesize a number of CT-ΣΔM architectures. Indeed, practically any given DT-ΣΔM topology reported in literature can be transformed into its CT-ΣΔM counterpart by using any of these DT-to-CT methods. However, describing every DT topology and its corresponding CT transformation is beyond the scope of this thesis and it can be found in a number of monographs and books [Abus02][Cher00][Ortm06][Shoa95].

#### 1.5.3.1 Single-quantizer lowpass CT-ΣΔM architectures

We will start the review of basic CT modulator architectures with the single-loop second-order topology shown in Fig. 1.21(a). This modulator uses FE integrators with a Z-domain transfer function given by:

\[ I(z) = \frac{z^{-1}}{1 - z^{-1}} \]

(1.52)
The open loop filter transfer function of the ΣΔM in Fig. 1.21(a) – defined as the transfer function from the quantizer output to the quantizer input, is given by [Ortm06]:

\[
LF(z) = -a_2I(z) - a_1a_2^2(z) = -\frac{a_2}{z-1} - \frac{a_1a_2}{(z-1)^2}
\]  

(1.53)

Considering the S-Z transformations given in Table 1.1 and assuming a NRZ DAC waveform, it is easy to show that the DT-to-CT transformation of (1.53) is given by:

\[
LF(s) = -\left(\frac{a_2}{2} - \frac{a_1a_2}{2}\right)f_s - a_1a_2^2 \frac{f_s^2}{s}
\]  

(1.54)

One possible implementation of the open loop filter in (1.54) is shown in Fig. 1.21(b), where \( I(s) = \frac{f_s}{s} \) is the CT integrator transfer function, and \( g_i \), are the feedback coefficients given by:

\[
g_1 = g_1' = a_1a_2; \quad g_2 = \left(a_2 - \frac{a_1a_2}{2}\right)
\]  

(1.55)

From (1.54) and (1.55), the CT loop filter yields:

\[
H(s) = LF(s) = -\frac{f_s}{s}g_2^2 - g_1\frac{f_s^2}{s^2}
\]  

(1.56)

whose scaling coefficients can be choosing such that the CT-ΣΔM in Fig. 1.21(b) behaves

**Figure 1.21:** Second-order ΣΔM. (a) DT block diagram. (b) CT equivalent.
exactly as its DT counterpart in Fig. 1.21(a). This is illustrated in Fig. 1.22 that represents the output spectra of both modulators and the scaling coefficients proposed in [Marq98] have been used.

It is important to note that, the transfer function found in (1.56) and its associated modulator architecture, varies with the DT-to-CT transformation method and the DAC waveform used. Thus, for a general rectangular DAC waveform, the corresponding feedback coefficients of a 2nd-order and a 3rd-order CT-ΣΔMs are given by [Ortm06]:

\[
\begin{align*}
2\text{nd-order} & \quad g_1' = \frac{a_1a_2}{p_2-p_1}, \quad g_2 = \frac{a_1a_2}{2} \cdot \frac{2 + p_1 + p_2 - 2}{p_2 - p_1} \\
3\text{rd-order} & \quad g_1' = \frac{a_1a_2a_3}{p_2-p_1}, \quad g_2 = \frac{a_1a_2a_3}{2} \cdot \frac{2 + p_1 + p_2 - 3}{p_2 - p_1} \\
& \quad g_3 = \frac{a_1a_2a_3}{12} \cdot \frac{p_2(p_1 - 9) + p_2(p_2 - 9) + 4p_1p_2 + 6/a_2(1/a_2 + a_1 - 1)}{p_2 - p_1} 
\end{align*}
\]

(1.57)

Alternatively, if a modified Z-transformation is used and considering a SCR DAC (see Fig. 1.13(f)), with an impulsive response given by:

\[
DAC(s) = e^{-st_d} \left( \frac{1 - e^{-t_p(s + 1/\tau_{DAC})}}{s + 1/\tau_{DAC}} \right)
\]

(1.58)

where \( t_p = t_1 - t_d \). Then, the resulting coefficients of Fig. 1.21(b) are [Ortm06]:

![Figure 1.22: Output spectra of the modulators in Fig. 1.20. (a) DT (b) CT.](image-url)
Theoretically, the above described methodology could be used to synthesize an arbitrary 2nd-order lowpass CT-$\Sigma$M. However, it is well-known that for those $\Sigma$DMs with $L > 2$, and particularly those with a pure differentiator NTF – i.e FIR filters with $(1 - z^{-1})^L$ transfer function, are prone to instability [Adam97]. For that reason, alternative high-order single-quantizer DT-$\Sigma$DMs topologies have been proposed in literature [Nors97][Enge99]. Fig. 1.23 shows the most usual high-order CT-$\Sigma$DM topologies including the so-called interpolative $\Sigma$DM (Fig. 1.23(a)) proposed by Lee and Sodini [Lee87]; cascade of integrators with feedforward summation and local resonator feedbacks (Fig. 1.23(b))[Abus02]; and the cascade of integrators with distributed feedback and distributed input paths (Fig. 1.23(c)) [Abus02] [Nors97][Schr05].

Most of the high-order topologies, like the ones shown in Fig. 1.23, are based on the use of several feedback and/or feedforward transmission of the signals in the modulator loop in order to implement IIR NTFs with multiple zeroes and poles. These zeroes and poles can be distributed using either a Butterworth or Chebychev filter approximation such that the in-band noise power is minimized.

An important drawback of the high-order CT-$\Sigma$DMs shown in Fig. 1.23 is the increased complexity of the analog circuitry. Therefore, in order to optimize the stability-resolution trade-off, most high-order CT-$\Sigma$DMs are synthesized directly in the CT domain instead of applying a DT-to-CT transformation method. In any case, the strategies followed to preclude from instabilities leads to lower values of $DR$ as compared with what can be obtained according to the ideal values in (1.17) [Rio06].

1.5.3.2 Cascade CT-$\Sigma$DM architectures

A well-known alternative to circumvent instabilities while obtaining high-order noise shaping consists of using the so-called MASH (multi-stage noise-shaping) $\Sigma$DMs, often referred to as cascade or multi-stage $\Sigma$DMs [Marq98][Rodr03][Nors97]. This architecture is conceptually depicted in Fig. 1.24. Each stage, consisting of a single-loop CT-$\Sigma$DM (typically either second or first order), modulates a signal that contains the quantization error

\begin{align*}
g_{1,\text{Mod2-SCR}} &= \frac{a_1 a_2 T_s}{\tau_{DAC} \left(1 - e^{-T_s/2/\tau_{DAC}}\right)} \\
g_{2,\text{Mod2-SCR}} &= \frac{a_2 \left(-a_1 T_s + (2a_1 \tau_{DAC} + 2T_s) \left(1 - e^{-T_s/2/\tau_{DAC}}\right)\right)}{\tau_{DAC} \left(1 - e^{-T_s/2/\tau_{DAC}}\right)^2}
\end{align*}

(1.59)

†3. Bandpass CT-$\Sigma$DMs have NTF with zeroes at different frequencies from DC. For that reason, additional design considerations need to be accounted as will be described in Section 1.5.3.3.

†4. The interested reader can read the equivalence between CT- and DT- high-order topologies in a number of papers and monographs. Particularly detailed description can be found in [Abus02].
Figure 1.23: Illustrating high-order single-quantizer CT-$\Sigma$ΔMs. (a) Lee-Sodini (Interpolative) topology. (b) Cascade of integrators with feedforward summation and local resonator feedbacks (5th-order topology). (c) Cascade of integrators with distributed feedback paths (5th-order topology).
generated in the previous stage. Once in the digital domain, the stage outputs are processed and combined by the cancellation logic so that only the quantization error of the last stage remains. Also, this error is shaped by a transfer function whose order equals the sum of the respective orders of all the stages in the cascade [Rio06].

The principle underlying cascade $\Sigma\Delta$Ms can be a priori extensible to whatever number of stages. However, in practice, it is well-known that the number of stages – and consequently the order of the modulator – is limited by circuit non-idealities, particularly mismatch. This error causes incomplete cancellation of low-order quantization errors at the modulator output [Rio06]. This effect – known as noise leakage – is especially critical in cascade CT-$\Sigma\Delta$Ms because of their higher sensitivity to circuit element tolerances. This explains the very few reported cascade CT-$\Sigma\Delta$Ms ICs reported so far [Bree04].

However, the increased demand for wideband ADCs has prompted the interest in cascade CT-$\Sigma\Delta$Ms in order to implement high-order noise-shaping with low oversampling ratios whereas guaranteeing stability [Olia03][Ortm06]. Most published proposed synthesis methods based on applying a DT-to-CT transformation to an equivalent – well known – cascade DT-$\Sigma\Delta$M. However, as will be demonstrated in this thesis, the use of DT-to-CT synthesis methods yields an increase of the analog circuit complexity, with the subsequent penalty in silicon area, power consumption, and sensitivity to parameter variations. Indeed, more efficient cascade CT-$\Sigma\Delta$M architectures can be shown if a direct synthesis method is obtained [Tort06].

As a matter of example, in the following, the DT-to-CT transformation of a cascade 2-1 DT-$\Sigma\Delta$Ms shown in Fig. 1.25(a) will be described [Ortm06]. To do such a transformation it is needed to take into account not only the loop filter transfer function of the $i$-th stage, $LF_i$, but also the inter-stage loop filter transfer functions, $LF_{ij}$, representing the transfer function from the output of preceding stages to the input of the quantizer of the following stages. Thus, the corresponding expressions for the DT $LF_S$ of the modulators in Fig. 1.25(a) are the following:

Figure 1.24: Conceptual block diagram of a cascaded CT $\Sigma\Delta$M.
\begin{align}
LF_{1DT}(z) &\equiv \frac{q_1}{y_1} = -a_1 a_2 F(z) - a_2 I(z) \\
LF_{2DT}(z) &\equiv \frac{q_2}{y_2} = -a_3 I(z) \\
LF_{12DT}(z) &\equiv \frac{q_2}{y_1} = (g_1 LF_{1DT} - b_1)c_1 a_3 I(z)
\end{align}

(Figure 1.25: Cascade 2-1 \(\Sigma\Delta M\). (a) DT. (b) CT equivalent.)
Assuming a NRZ DAC waveform, and taking into account the S-Z equivalences given in Table 1.1, the corresponding CT $LF$s are obtained, giving:

\[
LF_{1CT}(s) = -\frac{a_1 a_2 f_s^2}{s^2} - \frac{1}{2} \frac{a_2 (2 - a_1) f_s}{s}
\]

\[
LF_{2CT}(s) = \frac{a_3 f_s}{s}
\]

\[
LF_{12CT}(s) = -\frac{c_1 a_3^3}{s^3} - \frac{c_1 a_3 (1/a_1 - 1) f_s^2}{s^2} - \frac{c_1 a_3 [b_1 + 1/3 - 1/(2a_1)] f_s}{s}
\]

(1.61)

To get a functional CT-\Sigma\Delta M topology that satisfies (1.61) while keeping identical digital Cancellation Logic (CL) as its corresponding DT counterpart (Fig. 1.25(a)), every state variable (integrator output) and DAC output must be connected to the integrator input of the ulterior stages in the cascade [Ortm01]. This increases the number of analog components needed, leading to the CT-\Sigma\Delta M topology shown in Fig. 1.25(b), which at least ideally, behaves equivalently to its DT counterpart [Ortm06].

1.5.3.3 Bandpass CT-\Sigma\Delta M architectures

BandPass \Sigma\Delta Ms (BP-\Sigma\Delta Ms) are a particular class of \Sigma\Delta Ms that place the zeroes of NTF in a given bandwidth around an Intermediate Frequency (IF) location, usually named notch frequency, $f_n$. Therefore, BP-\Sigma\Delta Ms differ from their LP counterparts in that the loop filter is of bandpass type instead of lowpass type as illustrated in Fig. 1.26 [Schr89][Gail89]. This has an obvious application in the front-end of wireless communication systems. Indeed, BP-\Sigma\Delta Ms are very suited for the implementation of ADCs in such systems because, compared with lowpass ADCs, BP-\Sigma\Delta Ms do not need to digitize the whole Nyquist band (from DC to $f_s$) (see Fig. 1.26). Instead, they digitize just the signal band, thereby requiring much less power consumption to obtain similar dynamic range [Enge99][Rosa02]. In addition, IF A/D conversions allows to move great part of the signal

![Conceptual block diagram of a BP-\Sigma\Delta M and its output spectrum.](image)

**Figure 1.26:** Conceptual block diagram of a BP-\Sigma\Delta M and its output spectrum.
processing from the analog domain to the digital domain, including: quadrature mixing, channel selection, gain control and demodulation. This results in robust Radio Frequency (RF) receivers with high degree of programmability and adaptability to a number of standard specifications.

BP-$\Sigma$ΔMs share much in common with their LP counterparts, except for the obvious difference that the quantization noise is suppressed around $f_n$ instead of DC. A common choice is using $f_n = f_s/4$, i.e just in the middle of the Nyquist band. It can be shown that this location optimizes the trade-off between antialiasing filtering and image-reject filtering in digital wireless transceivers [Rosa02][Rodr03].

The design and analysis of BP-$\Sigma$ΔMs is the same as that of LP-$\Sigma$ΔMs, but considering bandpass loop filters instead of lowpass loop filters. Indeed, it can be shown that the main figures of merits, i.e in-band noise power, DR, SNR, SNDR have the same expressions as the ones obtained in Section 1.3.2 [Rodr03]. In practice, it means that a BP-$\Sigma$ΔM can be synthesized by replacing integrators by resonators in the modulator loop filter. These resonators may be implemented either as DT circuit techniques or CT techniques, the latter giving rise to the so-called CT BP-$\Sigma$ΔMs Section [Nors97][Cher00][Rosa02][Shoa95].

Since Schreier and Snelgrove proposed the idea of BP $\Sigma$Δ modulation in 1989 [Schr89], a number of CT BP-$\Sigma$ΔM ICs have been published [Enge99] [Tort06][Hsu00][Schr06]. Similarly to lowpass modulators, CT BP-$\Sigma$ΔMs can be synthesized either using a direct synthesis method or any of the DT-to-CT synthesis methods described in previous sections. In the case of a DT-to-CT transformation is used, DT resonators are transformed into CT resonators using $S-Z$ equivalences shown in Table 1.1. As a matter of example, Fig. 1.27(a) shows the block diagram of a 4th-order CT BP-$\Sigma$ΔM. This modulator is equivalent to the DT modulator shown in Fig. 1.27(b) and their in-loop resonators have a resonant frequency at $f_n = f_s/4$. This translates in an output spectrum with a noise shaping like the one shown in Fig. 1.27(c). Note that the architecture in Fig. 1.27(a) uses multiple feedback loops including two different DAC waveforms – RZ and NRZ – each one with separately feedback coefficients. This is needed to obtain similar noise-shaping than that of the DT BP-$\Sigma$ΔM in Fig. 1.27(b) because it allows to use resonator transfer functions of the type $s/(s^2 + \omega^2)$, which are easier to realize through Gm-C circuits than the CT filters resulting from the impulsive-variable transformation method [Shoa95][Cher00].

1.6 Circuits and Errors

In previous sections, CT-$\Sigma$ΔMs have been analysed from an ideal point of view. In practice, such an ideal performance is degraded as a consequence of the error mechanisms associated to their circuit implementation. These errors can be divided into two main categories [Cher00][Ortm06]:

†5. One advantage of CT resonators is that they can implement continuously-tunable resonant frequencies, which allows the corresponding BP-$\Sigma$ΔMs to have a programmable frequency band [Shoa90].
• **Building-block errors**, which are the non-ideal effects derived from the CT-ΣΔM loop filter implementation such as finite opamp DC gain (in the case of RC-active integrators), integrator time-constant error, integration incomplete transient response, circuit element tolerances, non-linearities (specially at the input front-end Gm-C integrators), circuit noise, etc.

• **Architectural timing errors**, namely: quantizer metastability, excess loop delay and clock jitter error.

As a consequence of these non-idealities, the effective resolution of any CT-ΣΔM archi-
tecture is reduced as compared to the ideal values presented in previous sections. In some conditions, and particularly in the case of timing errors, the performance of CT-ΣΔMs may become totally degraded.

The rest of the Annex analyses the impact of main non-idealities and non-linearities affecting the performance of CT-ΣΔMs. To this purpose, their main building blocks will be described first.

### 1.7 CT Integrators

CT integrators are the most important and critical building blocks of CT-ΣΔMs [Ortm06]. These circuits constitute the basic elements of the modulator loop filter of low-pass CT-ΣΔMs. Moreover, they can be combined to build resonators in order to implement bandpass CT-ΣΔMs.

There are four practical CT integrator structures – conceptually depicted in Fig. 1.28[Tsiv94]: active-RC integrators (Fig. 1.28(a)); Gm-C (Fig. 1.28(b)); MOSFET-C (Fig. 1.28(c)) and active Gm-C or Gm-MC (Fig. 1.28(c)). From an ideal point of view, all these implementation have the same transfer function, given by:

$$I(s) = \frac{v(s)}{x(s)} = \frac{1}{s\tau} \quad (1.62)$$

where \(\tau\) is the integrator time constant, which is the product of the resistive and capacitive elements of the CT integrator as shown in Fig. 1.28.

In practice, the behaviour of the CT integrator implementations in Fig. 1.28 is different, involving a number of trade-offs. Thus, active-RC integrators have the advantages of better linearity and larger signal swing, whereas Gm-C integrators usually can operate at higher

![Figure 1.28: Alternative circuit techniques for the implementation of CT Integrators: (a) Active RC. (b) Gm-C. (c) MOSFET-C. (d) Gm-MC.](image-url)
frequencies with less power consumption. MOSFET-C integrators, which allow a continuous time-constant tunability, present a poor linearity and indeed, have been much less used in practical CT-ΣΔM implementations [Ortm06]. Among others, most frequently used implementations of CT-ΣΔMs include either active-RC integrators or Gm-C integrators or a combination of both types of integrators. The following subsections sum up the most important characteristics of these CT integrator topologies.

1.7.1 Gm-C Integrators

As illustrated in Fig. 1.28(b), Gm-C integrators are based on the connection of a transconductance element and a capacitor. The input voltage, $x$, is multiplied by the transconductance, $g_m$, giving rise to a current which drives the load capacitance, $C$. The resulting ideal transfer function is given by:

$$I(s) = \frac{g_m}{sC}$$  

(1.63)

Gm-C integrators can be easily tuned and are specially suitable for low-voltage applications. Their main limitation is caused by the non-linearity in the voltage-to-current conversion of the transconductor element, which forces in some applications to replace the front-end integrator with an active-RC (which can be much more linear) while the remaining integrators in the loop filter are implemented using Gm-C. Alternative strategies to improve linearity in Gm-C integrators are based on the combination of fully differential topologies with source degeneration. The prize to pay is an increase of the power consumption [Tsiv94].

Another important limitation of Gm-C integrators is their high sensitivity to parasitic capacitances, $C_p$, as illustrated in Fig. 1.29. This capacitance alters directly the integrator time constant, modifying (1.63) as:

$$I(s) = \frac{g_m}{sC} \rightarrow I(s) = \frac{g_m}{s(C + C_p)}$$  

(1.64)

The effect of $C_p$ can be reduced by including a virtual ground, which is implemented by an operational amplifier as shown in Fig. 1.28(d). The resulting integrator, called active Gm-C or Gm-MC integrator, is more robust against parasitic capacitances connected at the amplifier input because only small voltage fluctuations are produced thanks to the action of the virtual ground. Moreover, smaller values of $C$ can be implemented because the effec-

![Figure 1.29: Gm-C integrator with parasitic capacitance, $C_p$.](image)
tive capacitance is amplified by the Miller effect of the opamp. However, the opamp is an active element and therefore, increases the power consumption as compared to simple Gm-C integrators.

Gm-C integrators can be used to build resonators\[^{\dagger6}\] as illustrated in Fig. 1.30. Resonators are basic building blocks which can be used to implement bandpass CT-ΣΔMs and low-pass CT-ΣΔMs with NTF zeroes at different frequencies than DC. In the case of the resonator in Fig. 1.30, the resonant frequency, \( f_n \), is given by:

\[
 f_n = \frac{1}{2\pi} \sqrt{\frac{g_{m2}g_{mR}}{C_1 C_2}}
\]  

(1.65)

which can be electronically tuned by \( g_{mR} \) [Rabi99].

### 1.7.2 Active-RC integrators

Another alternative of CT integrator implementation that has been used in plenty of CT-ΣΔM ICs is the well-known active-RC integrator, conceptually shown in Fig.1.28(a), whose ideal transfer function is given by:

\[
 I(s) = \frac{1}{sRC}
\]  

(1.66)

This integrator is more robust than Gm-C topologies against capacitor parasitics in part due to the virtual ground. Besides, it achieves high linearity provided that the input resistor, \( R \), – responsible for the V/I conversion – is linear enough. Another source of distortion comes from the non-linear amplifier transfer function, which can be reduced by increasing the value of \( R \) at the price of increasing thermal noise [Ortm06]. This trade-off can be obvi-

---

\[^{\dagger6} \] Gm-C based resonators can be also implemented by a transconductor driving a LC tank, instead of a simple capacitor. Both monolithic and off-chip inductors have been used for their implementation involving different design trade-offs among silicon area, resonant frequency accuracy, quality factor, etc. [Geer02][Schr06].
ously solved by increasing the bias current in order to reduce the power dissipation.

The main concern of active-RC integrators is their lower speed as compared to open-loop Gm-C integrators. Nevertheless, and depending on the application, active-RC can be a good choice to solve the trade-off among linearity, speed, power consumption and thermal noise. Indeed, one might think of the very demanding restrictions imposed to the opamp Gain-BandWidth (GBW), this specification is notably relaxed as compared to the Discrete-Time (DT) case, for instance in a Switched-Capacitor (SC) integrator. Indeed, it can be shown that the ideal integrator unity-gain frequency,

\[ f_u = \frac{1}{2\pi RC} \tag{1.67} \]

can be chosen to be approximately equal to the sampling frequency, \( f_s \), which leads to a much more relaxed design (in terms of power dissipation) as compared to the DT case, where the typical requirement is \( f_u \approx 5f_s \).

In order to take advantage of the benefits of both active-RC and Gm-C integrators, the most common situation in practice (particularly in CT-ΣΔMs targeting medium-high resolution within medium bandwidths) consists of including a front-end active-RC integrator while the remaining integrators are implemented by using Gm-C techniques.

1.8 Building-block errors

As pointed out in Section 1.6, CT-ΣΔM errors can be classified into two main categories: building-block errors and timing errors. This section is focused on the former ones, that are responsible for the increase of in-band noise power and/or harmonic distortion in the modulator. In order to analyse the impact of a non-ideal (linear) building-block errors, the following procedure is commonly followed [Mede99][Ortm06]:

- Obtain an integrator\(^{\S7}\) equivalent circuit considering the non-ideal effect under study.

- Analyse the impact of the non-ideality on the integrator transfer function, \( I(s) \), such that \( I(s) \rightarrow I(s, e) \), with \( e \) being the error vector including all non-ideal variables included in the integrator equivalent circuit.

- In order to compute the effect of \( e \) on a \( L \)th-order CT-ΣΔM, integrator transfer functions are replaced with \( I(s, e) \), and a linear model of the quantizer is considered to get the non-ideal NTF, \( NTF(s, L, e) \).

\(^{\S7}\) Similar study is followed for resonators in the case of BP-ΣΔMs [Rosa02].
• $NTF(s, L, \varepsilon)$ is integrated within the signal band in order to obtain the In-Band-Noise (IBN) power, also represented as $P_{Q_e}$, given by:

$$IBN_e \equiv P_{Q_e} \equiv \int_{\text{Signal band}} \frac{\Delta^2}{12 f_s} NTF(f, L, \varepsilon) df \tag{1.68}$$

which, after some approximations can be explicitly shown as a function of $\varepsilon$ and the modulator parameters, i.e $B, L, M$. Note that, once $P_{Q_e}$ is known, the corresponding non-ideal DR and SNR can be obtained.

The above procedure can be mathematically formulated as:

$$I(s) \rightarrow I(s, \varepsilon) \rightarrow NTF(s, L, \varepsilon) \rightarrow \left\{ \begin{array}{l} IBN(M, B, L, \varepsilon) \\ \text{SNR}(M, B, L, \varepsilon) \\ \vdots \end{array} \right\} \tag{1.69}$$

The detailed description of the above formulation for each CT-$\Sigma$AM building-block non-ideality is beyond the scope of this annex, and can be found in a number of manuscripts$^8$. Instead, a summary of the most significant effects is described below, starting with the well-known effect of integrator leakage.

### 1.8.1 Integrator leakage

The ideal model for the active-RC integrator shown in Fig. 1.28(a) assumed an infinite value for opamp DC gain, i.e $A_{DC} \to \infty$. However in practice, a finite value $A_{DC}$ must be considered and the integrator transfer function of Fig. 1.28(a) is modified as:

$$I(s, \varepsilon_{A_{DC}}) \bigg|_{\text{Active-RC}} = \frac{1}{\varepsilon_{A_{DC}} + \tau s (1 + \varepsilon_{A_{DC}})} \tag{1.70}$$

where $\tau = RC$ and $\varepsilon_{A_{DC}} \equiv 1/A_{DC}$ stands for the error due to finite DC gain, which obviously becomes zero when $A_{DC} \to \infty$. Note that, as a consequence of this error, the integrator presents losses or leakage when $s \to 0$. For that reason, this error is commonly referred to as leakage error [Mede99].

In the case of Gm-C integrators, leakage error is caused by finite output resistance as illustrated in Fig. 1.31, whose transfer function is given by:

---

$^8$ The interested reader can find a in-depth description of the effect of building-block errors (mainly considering active-RC implementations) on the performance of CT-$\Sigma$AMs in [Ortm06]
where and , with being the finite output conductance. Note that both expressions (1.70) and (1.71) are quite similar. Indeed, multiplying both the numerator and denominator of (1.70) by \(1 - \varepsilon_{ADC}\), and assuming that \(\varepsilon_{ADC} \ll 1\), we obtain the following transfer function:

\[
I(s, \varepsilon_{ADC})_{\text{Gm-C}} = \frac{1}{\varepsilon_{ADC} + \tau s} \quad (1.71)
\]

that is the same as (1.71) except for a gain error, given by \(1 - \varepsilon_{ADC}\). Therefore, the impact on a single-loop lowpass CT-ΣΔM is approximately the same considering both integrator circuit implementations.

Following the analytical procedure described earlier, it can be shown that the IBN degraded by \(A_{DC}\) in a single-loop \(L\)-th order CT-ΣΔM with NRZ feedback DAC is approximately given by [Gerf03]:

\[
P_Q(A_{DC}) = \frac{\Delta^2}{12k_4g_q} \left[ \frac{2L}{M}\varepsilon_{ADC}^2 + \sum_{i=1}^{L} \left( \frac{\pi^{2i}2^{(L-i)}L(L-1)\cdots(L-i+1)}{(2i+1)M^{2i+1}i!} \right) \right] \quad (1.73)
\]

where \(g_q\) is the quantizer gain and \(k_4\) is the feedback scaling coefficient of the front-end integrator. Note that, the above expression approximates the ideal in-band noise power if \(\varepsilon_{ADC} \approx 1/M\) – exactly the same as happens in DT CT-ΣΔMs. This result is illustrated in Fig. 1.32, that shows the impact of finite DC gain on the SNR in a 2nd-order CT-ΣΔM for different values of \(M\).

It can be noted from (1.73) and Fig. 1.32 that the values required for \(A_{DC}\) are not very

![Conceptual Gm-C integrator with finite output resistance.](image)

\(^9\)In the case of bandpass CT-ΣΔMs, the modulator loop filter is based on resonators instead of integrators. Therefore, integrator gain errors affect the resonator transfer function, and hence, the corresponding NTF of the resulting bandpass CT-ΣΔM. In this case, the differences between (1.70) and (1.71) may result in different NTFs and, therefore, different impact of the finite DC gain error on the IBN of the bandpass CT-ΣΔM [Cher00][Rosa02].
demanding in practice. However – as also happens in the case of DT-ΣΔMs – this is not the case of cascade CT-ΣΔMs. In this case, if the integrator leakage is considered, the NTFs of the different stages in the cascade are modified and their quantization errors are incompletely cancelled in the digital domain, so that the non-ideal parts of the quantization noise leak into the overall modulator output [Rio06], causing an increase in the in-band noise power which can be expressed as [Ortm06]:

\[
P_Q(e_{ADC})_{\text{cascade}} \approx P_Q|_{\text{ideal}} + \sum_{i=1}^{L-1} \left( P_Q(e_{ADC})_{\text{ith-stage}} - P_Q|_{\text{ith-stage ideal}} \right) \quad (1.74)
\]

which corresponds to the ideal IBN of the cascade modulator plus the non-ideal parts due to integrator leakage of the IBN in all previous stage in the cascade.

In the same way as happens with DT-ΣΔMs, sensitivity of cascade CT-ΣΔMs to leakage error is higher than in the case of single-loop architectures. For instance, in a cascade 2-1-1 the required DC gain for the front-end stage integrators is \( A_{DC} \approx M^2 \) – in contrast to \( A_{DC} \approx M \) required for a single-loop 2nd-order CT-ΣΔM. The requirements for the subsequent stages in the cascade are more relaxed than the front-end stage, being \( A_{DC} \approx M^2 \) and \( A_{DC} \approx M \), for the second- and third stages, respectively.

### 1.8.2 Integrator gain error

Integrator gain error is caused by technology process variations of the integrator time constant\(^{10}\), \( \Delta \tau \), which yield to a modification of the ideal integrator transfer function given by:

\[
I(s) = \frac{1}{s \tau} \rightarrow I(s, e_{\tau}) = \frac{1}{s \tau (1 + e_{\tau})} \approx (1 - e_{\tau})I(s) \quad (1.75)
\]

---

\(^{10}\)For this reason, this error is sometimes named time-constant error [Cher00].
where $\varepsilon_\tau = \Delta \tau / \tau$, stands for the time-constant tolerance error.

In the case of DT implementations, the integrator gains are mapped into capacitor ratios, with variations typically lower than 0.1% in modern technology processes [Rio06]. However, in CT circuit realizations, time constants are mapped into resistor-capacitor products or transconductance-capacitor products, respectively for active-RC and Gm-C implementations. These products can present variations in the order of $\varepsilon_\tau = 20-30\%$, which represents a critical limiting factor, particularly in the case of cascade topologies [Ortm06].

Following the procedure described at the beginning of this section, the IBN degradation caused by integrator gain errors can be calculated, yielding the following expression for a $L$-th order single-loop CT-$\Sigma$M:

$$P_Q^{(\varepsilon_\tau)}_{\text{SL}} \approx \frac{\pi^2 L\Delta^2}{12(2L+1)} \frac{1}{k_i g_q M^{2L+1}} \prod_{i=1}^{L} \frac{1}{(1-\varepsilon_\tau_i)^2} = P_Q^{\text{ideal}} \prod_{i=1}^{L} \frac{1}{(1-\varepsilon_\tau_i)^2}$$

(1.76)

where $\varepsilon_\tau$ is the time constant error of the $i$-th integrator. Note that, although $\varepsilon_\tau$ decreases the modulator performance, the modulator still shows the same order shaping as the ideal one, and hence, realistic values of $\varepsilon_\tau$ can be tolerated. However, this is not the case of cascade CT-$\Sigma$ΔMs, where the impact of $\varepsilon_\tau$ is very critical, severely degrading the performance of the modulator.

Although there have been some attempts to analyse the impact of $\varepsilon_\tau$ on the performance of cascade CT-$\Sigma$ΔMs, calculations become enormously sophisticated. For instance, Ortmanns et al. [Ortm06] show that the IBN degraded by time constant errors in a $L$th-order cascade CT-$\Sigma$ΔM is approximately given by:

$$P_Q^{(\varepsilon_\tau)}_{\text{Cascade}} \approx \frac{1}{K-1} \left[ \prod_{i=1}^{K-1} d_i \right] \left[ \frac{\pi^2 L_i \Delta_i^2}{12(2L_i+1)} \frac{1}{k_i g_q^2 M^{2L_i+1}} \right] + \sum_{i=1}^{K-1} \left[ \prod_{i=1}^{K-1} d_i \right] \left[ \frac{\pi^2 L_i \Delta_i^2}{12(2L_i+1)} \frac{1}{k_i g_q^2 M^{2L_i+1}} \sum_{i=1}^{L} \left( \frac{1}{\varepsilon_\tau_i} - 1 \right)^2 \right]$$

(1.77)

where $K$ is the number of stages in the cascade, $d_i$ is the inter-stage gain coefficient and $L_i$ and $\varepsilon_\tau_i$ are the order and the time constant error of the $i$-th stage, respectively.

Instead of using such complicated – and not always so precise and usable – expres-
sions, many authors evaluate this effect by means of MonteCarlo simulations using behavioural models [Tort06].

The impact of $\varepsilon_{\tau}$ is much more critical in cascade CT-$\Sigma\Delta$Ms, which are severely more sensitive to variations in the practical values of circuit element tolerances than their single-loop counterparts. This fact explains why there are very few reported cascade CT-$\Sigma\Delta$M ICs [Bree04][Bree07]. Indeed, cascade CT-$\Sigma\Delta$Ms cannot be implemented without some kind of compensation techniques, such as on-chip tuning [Shoa97][Xia04][Xia04] and/or digital calibration [Bree04][Ortm05]. The use of these strategies may mitigate the effect of element tolerances, albeit mismatches still remains. These techniques can be combined with proper synthesis methods in order to obtain more robust cascade CT-$\Sigma\Delta$M topologies as demonstrated in this thesis.

1.8.3 Integrator transient response – Finite GBW and Slew-Rate

As CT-$\Sigma\Delta$M loop filters are operating in the CT domain, their transient response is not so strictly limited to be settled within a finite time slot – usually half of the clock signal period – as it is for the DT-$\Sigma\Delta$Ms. Thus, non-dominant integrator poles and their cause, finite Gain-BandWidth (GBW) product, is more than an issue in DT circuitry than it is in CT ones [Cher00]. Indeed, from a general point of view, it can be said that non-dominant integrator poles degrade the loop stability of the entire modulator by pushing the modulator poles closer to the imaginary axis. Therefore, this non-ideal effect must be taken into account in order to optimize the design in terms of power dissipation and speed, even in the case of CT-$\Sigma\Delta$Ms, in spite of their less sensitivity to this error. This is particularly critical in high-speed applications, where 2nd-order (two-pole) models should be considered in the design process. In this case, the analysis becomes mathematically too complex, thus requiring the use of time-domain simulations using precise behavioural models like that presented in [Ruiz05].

A number of approaches have been reported to analyse the impact of GBW in the performance of CT-$\Sigma\Delta$Ms [Ortm06]. Among others, the work proposed by Ortmanns, Gerfers et al. [Ortm04] gives more accurate results using a comprehensive model for active-RC based CT-$\Sigma\Delta$Ms. This work is summarized in next subsection. The interested reader can find more detailed description in [Ortm04].

1.8.3.1 Effect of finite GBW

Let us assume that the operational amplifier in Fig. 1.28(a) has a single-pole transfer function given by:

$$A(s) = \frac{A_{DC}}{s + \frac{1}{\omega_{opamp}}}$$  (1.78)
where \( \omega_{opamp} \) is the dominant pole of the amplifier and \( GBW \equiv A_{DC} \omega_{opamp} \) is the gain-bandwidth product. Considering the above opamp transfer function, it can be shown that the transfer function of an active-RC integrator with \( n_A \) input paths is given by [Ortm04]:

\[
I(s, \varepsilon_{GBW}) \equiv \frac{1}{s} \frac{\varepsilon_{GBW}}{\omega_p s + 1} \tag{1.79}
\]

where

\[
\varepsilon_{GBW} \equiv \frac{GBW}{n_A}, \quad \omega_p = GBW + f_s \sum_{l=1}^{n_A} k_l \tag{1.80}
\]

and \( k_l \) is the scale coefficient of \( lth \)-path.

Note that, neglecting the effect of the opamp pole, \( \omega_p \), the impact of \( \varepsilon_{GBW} \) is approximately the same as that of the integrator gain error, \( \varepsilon_c \), and therefore, its effect on the modulator IBN is given by (1.76)-(1.77), by properly replacing \( \varepsilon_c \) with \( \varepsilon_{GBW} \).

If the effect of \( \omega_p \) is not neglected, the calculus of IBN due to GBW becomes extremely complex. Instead of doing such a complicate mathematical analysis, the authors in [Ortm04] propose a behavioural model in which \( \varepsilon_{GBW} \) can be divided into two errors: finite integrator gain error and an excess loop delay in the modulator. This model is illustrated in Fig. 1.33 for a single-loop 2nd-order modulator. The feedback delays, \( \tau_{Di} \), are given by:

\[
\tau_{D1st} = \frac{1 - e^{-\omega_{p2}/f_s}}{\omega_{p2}}, \quad \tau_{D2nd} = \frac{\left(1 - e^{-\omega_{p2}/f_s}\right)\omega_{p1}^2 - \omega_{p2}^2 \left(1 - e^{-\omega_{p1}/f_s}\right)}{\omega_{p1} \omega_{p2} \left(\omega_{p1} - \omega_{p2}\right)} \tag{1.81}
\]

where \( \omega_{pi} \) are the poles resulting from (1.80) for the different integrators [Ortm04].

One of the benefits of this model is that it allows to compensate for finite GBW error using similar techniques as for the excess loop delay error – which will be discussed in next sections.

1.8.3.2 Slew Rate, SR

Another effect of the finite integrator transient response is the finite Slew Rate (SR),
Figure 1.33: Modeling finite GBW as extra loop delays [Ortm04].
defined as the maximum integrator output rate due to the limited current used to charge the integrating capacitor. In the case of CT integrators, the maximum SR can be mathematically expressed as:

\[
\text{SR}_{\text{max}} = \left. \frac{dv_o}{dt} \right|_{\text{max}} = f_s \left. V_{\text{in}} \right|_{\text{max}}
\]  

(1.82)

where \( v_o \) is the output voltage and \( V_{\text{in}} \) is the maximum input signal amplitude of the integrator. Considering an isolated integrator, \( V_{\text{in}} \) is mainly limited by the bias current, \( I_B \), of the differential input pair, as illustrated in Fig. 1.34. In this case the input-output DC characteristic of the transconductor can be formulated as:

\[
\begin{cases} 
-I_B & v_a < -\sqrt[3]{I_B/\beta} \\
\beta v_a \sqrt{2I_B/\beta} - v_a & -\sqrt[3]{I_B/\beta} \leq v_a \leq \sqrt[3]{I_B/\beta} \\
I_B & v_a > \sqrt[3]{I_B/\beta} 
\end{cases}
\]

(1.83)

where \( \beta \) is the large-signal transconductance of the transistor and \( \left| V_{\text{in}} \right|_{\text{max}} = \sqrt[3]{I_B/\beta} \).

Similarly to GBW, the effect of SR in CT-\( \Sigma \Delta \)Ms is less critical than in the case of DT-\( \Sigma \Delta \)Ms – even if single-bit quantization is used\(^{11}\). However, due to the strong dependence of SR on the exact waveforms of the different signals involved in the dynamics of a CT-\( \Sigma \Delta \)M, the analysis of the impact of SR becomes mathematically too complex and designers usually relay on simulations to get the required SR specifications in a given design [Ortm06]. As an illustration, Fig. 1.35 shows the impact of SR on a Gm-C 2nd-order single-bit CT-\( \Sigma \Delta \)M. Note that, in addition to increase in-band noise, harmonic distortion appears in the output spectrum of the modulator due to the strong non-linearity introduced by limited SR.

![Figure 1.34: (a) Input-output DC characteristic of a (b) Differential transconductor.](image-url)

\(^{11}\)Multi-bit quantization reduces integrator input/output swings, thus attenuating the effect of SR.
1.8.4 Non-linear errors

CT-ΣΔMs suffer from harmonic distortion caused by non-linear circuit errors. These errors are a direct consequence of the non-linear characteristics of CMOS integrated devices, namely: transistors, resistors and capacitors. In the same way as happens with other circuit non-ideal effects, the most critical building blocks are those placed at the modulator front-end – basically the first integrator – because the errors caused by the remaining blocks in the modulator loop are attenuated by the gain of previous ones. Thus, considering only the influence of the front-end integrator, there are several sources of non-linearity which must be taken into account by designers. As illustrated in Fig. 1.36, main non-linear errors in CT active-RC integrators are caused by voltage-dependency of the amplifier DC gain, integrator resistances and capacitors, which can be mathematically expressed as [Ortm06]:

\[
C = f_C(v_{out}) \approx C_{nom}(1 + C_{V1}v_{out} + C_{V2}v_{out}^2)
\]

\[
R = f_R(v_{in}) \approx R_{nom}(1 + R_{V1}v_{in} + C_{V2}v_{in}^2)
\]

\[
A_{DC} = f_A(v_{out}) \approx A_{DCnom}(1 + A_{V1}v_{out} + A_{V2}v_{out}^2)
\]

![Figure 1.35: Illustrating the effect of SR on a Gm-C 2nd-order CTΣΔM.](image)

![Figure 1.36: Non-linear error sources in: (a) Active-RC integrator (b) Gm-C integrators.](image)
In the case of Gm-C integrators, the main source of non-linearity is associated to the V/I conversion process carried out by the non-linear transconductance, given by [Bree01]:

\[
i(v_{in}) = \beta v_{in,\text{N}} \sqrt{2I_B/\beta} - v_{in} \approx \sum_{k=1}^{\infty} g_{m_k} v_{in}^k \approx g_{m_1} v_{in} + g_{m_3} v_{in}^3
\]  

\hspace{1cm} (1.85)

Among others, non-linear V/I conversion (implemented by either the input resistor in active-RC integrators or the input transconductance in Gm-C implementations) is the most limiting factor degrading the linearity of CT-ΣΔMs because its associated harmonic distortion adds directly to the input signal and is subsequently digitized [Bree01][Ortm06].

Assuming a fully-differential circuit implementation of Fig. 1.36(b) and that \( M \gg 1 \), it can be shown that the third-order harmonic distortion at the output of CT-ΣΔMs due to non-linear V/I conversion is given by [Bree01]:

\[
THD \approx HD_3 \approx \frac{g_{m_3} V_i^2}{g_{m_1}}
\]  

\hspace{1cm} (1.86)

where \( V_i \) is the modulator input amplitude.

The above expression can be used to approximately predict the harmonic distortion due to the non-linear V/I operation, which in the end, constitute the ultimate limiting factor of the linearity of a Gm-C CT-ΣΔM based ADC. Thus, in order to quantify the effect of non-linear errors in CT-ΣΔMs, most authors make use of simulations – either using behavioural or transistor-level models [Leuc01]. Recently, Sankar et al. proposed an analytical model for the non-linearity of CT integrators which can be used to both purposes: simulation and mathematical analysis [Sank07]. Fig. 1.37 illustrates this model for a Gm-C (Fig. 1.37(a)) and an active-RC (Fig. 1.37(b)) integrator. Basically, the model consists of replacing the ideal transfer function of a CT integrator by the following one:

\[
I(s)|_{\text{NL}} = f(x)I(s)|_{\text{ideal}}
\]  

\hspace{1cm} (1.87)

where

\[
f(x) = \begin{cases} 
  x - g_3/(4g_m)x^3 \\
  x - [2g_3/g_m(2 + g_mR^2)]x^3 
\end{cases}
\]  

\hspace{1cm} (1.88)

Using this model, the authors in [Sank07] demonstrate that non-linear CT integrators cause not only harmonic distortion but also an increase of the in-band noise power.
1.8.5 Circuit noise

Circuit noise constitutes the ultimate limiting factor of any \(\Sigma\Delta M\) [Mede99]. It is well known that this noise is originated by two physical mechanisms in CMOS circuits: thermal and flicker noise [Gray93]. Thus, practical designs must take into account the contribution of these noise sources generated by all \(\Sigma\Delta M\) building blocks. Among others, those blocks connected to the input node of the modulator — basically the front-end integrator and the corresponding feedback DAC — are the most important contributors because their noise is added directly to the input signal, thus appearing with no filtering at the output spectrum of the modulator, and increasing the in-band noise [Rosa02].

In the case of CT-\(\Sigma\Delta M\)s, all high-frequency noise components are filtered before they are sampled, because sampling process takes place at the input of the quantizer. Therefore, the remaining aliased noise components are attenuated by the corresponding noise shaping [Ortm06]. This is an advantage of CT-\(\Sigma\Delta M\)s as compared to their DT counterparts, where circuit noise is sampled at the input, causing aliased noise sources to increase the in-band noise power. This phenomenon gives rises to the well-known \(KT/C\) noise in SC \(\Sigma\Delta M\)s [Mede99].

Taking into account the above considerations, the analysis of electrical noise in CT-\(\Sigma\Delta M\)s is very simple and consists of obtaining the input-referred (unsampled) equivalent noise source. This calculus depends on the particular circuit-level implementation of the CT-\(\Sigma\Delta M\) and, in the more general case, yield to the analysis of the input-referred noise in a CT integrator. This analysis – beyond the scope of this thesis – can be found in many manuscripts and books dealing with the design of analog CMOS circuits [Gray93]. As an illus-
tration, Fig. 1.38 shows the main noise sources in an active-RC CT-ΣΔM together with the equivalent circuit needed to calculate the input referred noise. In this case, the in-band noise power is given by [Ortm06]:

\[
P_{\text{Noise}} \approx 32KTB_w \left( R + \frac{4n_{e,\text{th}}}{3g_{m\text{OTA}}} \right) + \frac{8K_f n_{e,f} \ln \left( B_w \right)}{C_{0x} W L} \left( \frac{B_w}{f_u} \right)
\]

where \( n_{e,\text{th}} \) and \( n_{e,f} \) stand for the thermal and flicker noise excess factors, \( g_{m\text{OTA}} \) is the amplifier input transconductance, \( K_f \) is a flicker noise technology parameter.

### 1.9 Excess loop delay

Ideally, the feedback DAC output in a CT-ΣΔM should respond immediately to the quantizer clock edge. However, in practice, there is a delay due to the finite transient response of the DAC circuitry. This delay – illustrated in Fig. 1.39 – is often referred to as excess loop delay, and mathematically expressed as a fraction of the sampling period, \( \tau_d = \rho_d T_s \), where \( 0 < \rho_d \leq 1 \).

The excess loop delay error introduces additional poles that increase the order of both the signal and noise transfer functions – \( S_{TF} \) and \( N_{TF} \) – which may lead to an unstable behaviour of the resulting CT-ΣΔM. The analysis of this effect is mathematically complex, and indeed there has been different approaches reported to find a close-form expression of the stability conditions [Cher99a][Roma00][Ortm06]. Some studies are based on analysing the equivalent DT- system and then make a DT-to-CT transformation [Cher99a][Ortm06]. Here, a direct CT methodology is followed as proposed in [Roma00] – considering two cases studies: 1st- order and 2nd- order single-loop CT-ΣΔMs.

![Figure 1.38: Main noise sources in active-RC integrators [Ortm06].](image)

![Figure 1.39: Step response of the DAC.](image)
1.9.1 Error analysis

Thus, in the case of a 1st-order CT-ΣΔM with excess loop delay, it can be shown that the S-transform of the output is approximately given by [Roma00]:

\[
Y(s) = \frac{g_q g_1/T_s \cdot G_H(s) \cdot H(s)}{1 + (g_1' \cdot g_q')/T_s \cdot G_H(s) \cdot e^{-\tau_d s}} X(s) + \frac{1}{1 + (g_1' \cdot g_q')/T_s \cdot G_H(s) \cdot e^{-\tau_d s}} E(s) \tag{1.90}
\]

where \(H(s) = I(s) = 1/(s \tau)\) and \(G_H(s) = \frac{1-e^{-s T}}{s} \) is the S-transform of the S/H circuit.

Considering \(M \gg 1\), then \(e^{-s T} \approx 1 - s T\) and (1.90) can be simplified into:

\[
Y(s) \approx \frac{g_q g_1}{g_q g_1' + (1 - \rho_d g_q g_1') s \tau} X(s) + \frac{s \tau}{g_q g_1' + (1 - \rho_d g_q g_1') s \tau} E(s) \tag{1.91}
\]

In this case, the stability of the modulator can be guaranteed if we assume that a quantizer gain of \(g_q = 1/(\rho_d g_1')\), thus nulling the zeroes of \(S_{TF}\) and \(N_{TF}\).

This is not the case of a 2nd-order CT-ΣΔM, where the excess loop delay modifies the S-transform of the modulator output as follows:

\[
Y(f) \approx \frac{g_q g_1 g_2}{(s \tau)^2 + g_q g_1 g_2' \cdot e^{-\tau_d s} + g_q g_2' \cdot (s \tau) e^{-\tau_d s}} X(f) + \frac{(s \tau)^2}{(s \tau)^2 + g_q g_1 g_2' \cdot e^{-\tau_d s} + g_q g_2' \cdot (s \tau) e^{-\tau_d s}} E(f) \tag{1.92}
\]

Assuming \(M \gg 1\) and applying the Ruth-Hurwitz’s stability criterion, it can be shown that a 2nd-order CT-ΣΔM is stable in the presence of excess loop delay if and only if the following condition is satisfied:

\[
\rho_d \leq \frac{g_2'}{g_1' g_2} \tag{1.93}
\]

The above condition has been obtained considering a linearized, additive noise model for the quantizer. Considering a non-linear model, a simulation-based analysis demonstrates that the stability condition in (1.93) is modifies as:

\[
\rho_d \leq \frac{g_2'}{2 g_1' g_2} \tag{1.94}
\]
The above result has been verified by simulation results. This is illustrated in Fig. 1.40, that shows the time response of the front-end integrator in a 2nd-order CT-ΣΔM for a 1-kHz input tone with half-scale amplitude. It is shown how, as ρ_d is increases, the amplitude of the integrator output increases, becoming unstable for ρ_d = 1.5, which is in close agreement with the theoretical stability condition – ρ_d ≤ 1 in this example.

Excess loop delays causes similar degradation in different modulator architectures, i.e. single-loop, cascade, lowpass, bandpass, etc. As an illustration, Fig. 1.41 shows the impact of excess loop delay in multi-feedback CT-BΨΣΔMs. As a consequence of the poles introduced by ρ_d ≠ 0, the noise-shaping transfer functions, S_{TF} and N_{TF}, are modified, thus increasing the in-band noise power as illustrated in Fig. 1.41(c). This effect becomes specially critical in telecom applications, in which large values of ρ_d – ρ_d ≅ 0.4 in the example of Fig. 1.41(b)-(c) – may eventually make CT-BΨΣΔMs unstable.

Mathematically speaking, complex analyses are required to obtain the stability condi-

†12. This architecture uses different types of DACs—each with separately feedback coefficients—to obtain similar noise-shaping than that of its corresponding DT-BΨΣΔM. This strategy allows us to use resonator transfer function of the type s/(s^2 + ω^2), which are easier to realize through g_m C circuits than the CT filters resulting from a DT-to-CT transformation.
tion in most common CT-ΣΔM architectures. Instead of that, simulation-based analyses are normally used to know the critical value of leading to instability. Indeed, the simulation-based analysis presented in [Cher99a] demonstrates that, in the more general case of a \( L \)-th-order (bandpass) CT-ΣΔM, the critical value of \( \rho_d \) is approximately given by:

\[
\rho_d \bigg|_{\text{critical}} \approx \frac{1}{|H(f)|_{\text{out-of-band}}} 
\]

where \( H(f) \) is the loop-filter transfer function.

### 1.9.2 Excess-loop-delay compensation techniques

In order to palliate the effect of excess loop delay, a number of compensation techniques have been reported in the open literature [Bena97] [Cher99a][Kell08][Ortm06]. Among others, the most commonly used strategies are based on the use of additional feedback DACs – with their corresponding tunable scaling coefficients – in order to cancel out the additional poles of \( N_{TF} \) [Cher99a]. This technique is illustrated in Fig. 1.42 for a 2nd-
order single-loop architecture, where an additional HRZ DAC is used [Ortm06]. The compensation scaling coefficient can be determined by matching the actual open-loop $LF$ transfer function with the ideal one. This calculation – detailed in [Ortm06] – can be done in the Z-domain yielding to the following relationships among ideal and real feedback coefficients:

$$k_1^* = k_1, \quad k_2^* = \frac{3k_1\tau_d}{2} + 2k_2, \quad k_h = k_1\tau_d + 2k_2$$  \hspace{1cm} (1.96)

where $k_i^*$ are the scaling feedback coefficients of the compensated modulator, while $k_i$ are the coefficients of the original (ideal) modulator.

An interesting and robust implementation based on the strategy described above was proposed by Yan and Sánchez-Sinencio [Xia04] and is illustrated in Fig. 1.43. As shown in Fig. 1.43(a), this technique consists in adding one extra feedback DAC (labelled DAC_B) which is connected from the output to the input of the internal quantizer, together with an additional half clock cycle delay. The clock timing diagram is shown in Fig. 1.43(b). The half-delay latch placed in front of DAC_B holds the data when clock (CLK) is low, whereas when CLK is high, it simply works as a digital buffer, and any change at the input propagates instantly to the output. In this way, the operation of the modulator is not affected even if the excess loop delay of the internal ADC varies from zero to nearly one clock period [Xia04]. The main benefit of this technique is that it reduces the impact of excess loop delay without adding any extra feedback coefficient – which needs some kind of calibration, as explained above†13.

---

†13.Indeed the excess-loop-delay compensation technique proposed in [Xia04] is the strategy most commonly used by reported CT-$\Sigma$AM ICs, and it has been used in the designs presented in this thesis.
The above strategies compensate for the excess loop delay in the analog part of the CT-ΣΔM. Recently, alternative solutions have been proposed to cancel out this error in the digital domain. This is the case of the digital cancellation technique proposed by Fontaine et al. [Gail89] – illustrated in Fig. 1.44, where a digital feedback loop is inserted after the internal quantizer and the analog coefficients are modified to produce an $N_{TF}$ almost equivalent to the ideal delay-free loop filter. A half-clock-delay latch is also used to relax the comparator speed and to provide maximum isolation of the quantizer from DAC switching events.

All these techniques together with other ones proposed in literature have been recently compared in an excellent paper by M. Keller et al. [Kell08], in terms of their impact on SNR, DR, output swing and dynamic requirements of both single-loop and cascade CT-ΣΔM architectures. In conclusion, it can be said that in present designs, excess loop delay is an error that must be taken into account, but their effect can be controlled by using proper design and architecture techniques. This non-ideal timing effect is particularly critical in high speed applications, where CT-ΣΔMs are more appropriate than their DT- counterparts.

![Figure 1.43](image1.png)

**Figure 1.43:** Excess-loop-delay cancellation technique presented in [Xia04].

![Figure 1.44](image2.png)

**Figure 1.44:** Digital compensation of excess loop delay [Gail89].
1.10 Comparator metastability

Previous analyses assume an ideal quantizer except for the inherent quantization error. In practice, quantizers are implemented by flash ADCs, in which non-ideal effects are mainly caused by comparator errors, namely: offset and hysteresis [Bose88]. As for the case of DT-ΣΔMs, the impact of comparator errors is attenuated by the gain of the complete loop filter and hence, they can be considered negligible as compared to building-block errors [Mede99].

Nevertheless, although comparator offset and hysteresis are less critical than other CT-ΣΔM errors, they must be taken into account in high-performance applications, particularly when high-resolution is required and multi-bit quantization is used [Ortm06]. In this case, there is a tradeoff among static resolution (limited by offset and hysteresis) and transient response of the comparators, which becomes severely degraded by the exponentially increased input capacitance with the number of bits. Moreover, the flash architecture requires a reference resistor ladder. Thus, in order to reduce the effect of capacitor feedthrough from the comparators into the reference ladder, the resistors need to be small, thus increasing the power dissipation [Ortm06]. In order to circumvent this multiple tradeoff among offset, hysteresis, speed and power dissipation, some authors propose alternative solutions to implement high-resolution quantizers by using tracking quantizer [Dorr05] or successive approximation ADCs [Sami02].

In addition to the errors caused by the comparator, the quantizer operation is degraded by two timing-induced errors, namely: clock jitter and comparator metastability. The former – discussed in Section 3.6 – has a little impact on the resolution of the modulator. The latter – caused by the signal dependency of the quantizer delay – is particularly critical in the case of CT-ΣΔMs, and can be considered as a variable excess loop delay – analysed in previous section – but associated to the quantizer block instead to the DAC transient response.

Comparator metastability is illustrated in the electrical simulation shown in Fig. 1.45(a) [Cher99]. This phenomenon consists of the variation of the comparison time with the input signal, \( v_i \). Ideally, the time delay depicted in Fig. 1.45(a) should be independent on the input signal. However, as a consequence of the finite comparator gain, there is a dependence of the comparison time with the input signal amplitude. This dependence can be mathematically expressed as [Cher99]:

\[
d_m = d_0 + \frac{d_1}{|v_i|^a}
\]  

(1.97)

†14. The interested reader can find more details about the effect of comparator errors on the performance of ΣΔMs in [Bose88].

†15. As metastability is a quantizer-induced error, its effect is less critical than excess loop delay, which directly affects the loop filter transfer function.
where $d_0$ stands for the comparison time delay for large input signal amplitudes and $\alpha$ is an adjustable parameter. The effect of this signal-dependent delay is illustrated in Fig. 1.45(b) for a 2nd-order CT-$\Sigma\Delta$M [Cher99], showing a severe increase of the in-band noise power as compared to considering a constant time delay.

The effect of metastability is relatively easy to circumvent by including latches between the quantizer and the feedback DAC. Clocking each latch stage on the opposite clock phase from the previous stage gives the previous stage a good deal of time to settle. The price to pay is the additional delay introduced in the feedback loop [Cher00]. Indeed, the effect of metastability is a critical issue as the clock frequency increases and the timing errors become limiting factors. However, the use of multiple latches has been demonstrated very effective even for sampling frequencies in the GHz range. This is the case of the 2nd-order CT-$\Sigma\Delta$M reported in [Enge99], where a 2-GHz clock signal is used. As illustrated in Fig. 1.46, the modulator in [Enge99] uses a comparator based on two latches. However, additional latches are used to synchronize the last latch’s output transitions with the sampling clock times. These additional latches can reduce comparator’s metastability. The number of latches vary depending on a number of practical issues. Thus, for typical process parameters, 3-latch solution is adequate to meet the metastability specification. However, to meet the metastability specification over all process corners, a 5-latch comparator is necessary [Enge99].

1.11 Clock jitter error

The performance of CT-$\Sigma\Delta$Ms may become largely impacted by time uncertainties in the clock-signal edges – illustrated in Fig. 1.47(a) – commonly referred to as clock jitter [Cher00]. Clock jitter occurs at those points within the modulator architecture where signals are transformed from the CT- domain to the DT- domain and vice versa, i.e at the S/H and reconstruction DAC, respectively as illustrated in Fig. 1.47(a). The error introduced by the
Figure 1.46: 2-GHz 2nd-order CT-ΣΔM architecture with multiple latches to reduce metastability [Enge99].

Figure 1.47: Clock jitter in CT-ΣΔMs. (a) Main jitter error sources. (b) 1-bit RZ vs. NRZ CT DAC waveforms. (c) DT vs. CT feedback DAC waveforms.
S/H is attenuated within the signal band by the modulator noise-shaping effect, and can hence be neglected. However, the jitter error at the DAC – illustrated in Fig. 1.47(b) for a NRZ and RZ 1-bit waveforms – occurs without attenuation at the input node, thereby limiting modulator accuracy. The reason why CT-ΣΔMs are more sensitive to clock jitter than DT-ΣΔMs is illustrated in Fig. 1.47(c), where typical SC waveform is compared to a CT current-mode waveform. In the SC case, most of the charge transfer occurs at the start of the clock period, so that the amount of charge lost due to a timing error is relatively small. By contrast, in the CT case, charge is transferred at a constant rate over a clock period, and so charge loss from the same timing error is a larger proportion of the total charge [Veld03].

Jitter analysis of high-speed CT-ΣΔMs has attracted significant interest in technical literature [Zwan96][Olia98][Tao99][Cher00][Bree01][Olia03][Hern04] [Chan06] [Redd07] [Vasu09]. Most studies have addressed only the case of modulators with single-bit quantizers and RZ DACs whereas a much smaller number of studies have been focused on modulators employing multi-bit quantizers and NRZ DAC waveforms [Hern04] [Redd07]. This may be due to the fact that analysis of these multi-bit NRZ waveforms is mathematically more complex than their RZ counterparts. As a consequence, designers willing to use these waveforms have to rely on inexact semi-empirical estimations based on simulation results [Cher00][Hern04][Xia04], whereas very little has been done in the theoretical area [Redd07].

Despite the lack of theoretical coverage, multibit quantizers and NRZ DACs are appealing for practical usage because they have low sensitivity to jitter. Many of the recently reported prototypes for medium-to-high resolutions (11-14bit) and large signal bandwidths (1-15MHz) employ either multi-bit quantizers, or NRZ DACs, or both [Moya03][Pato04]. This thesis is basically aimed at bridging the gap between theory and practice by providing an analytical coverage of jitter error in multi-bit CT-ΣΔMs with NRZ DACs. As compared to both the effect of the modulator loop filter transfer function and that of the input signal are covered herein. The state-space formulation is used to derive closed-form relations between jitter error, sampling frequency, modulator specifications (resolution and signal bandwidth), circuit topology (loop filter transfer function and number of bits of the internal quantizer) and input signal parameters (amplitude and frequency). This state-space formulation is general, architecture-independent, and can be applied to any kind of CT ΣΔMs either cascade or single-loop.

The study described in this thesis highlights effects that are significant for medium-to-high-frequency applications like the ones targeted in this thesis. As the number of bits of the internal quantizer increases, the signal-dependent term dominates over the modulator-dependent term, as it would be expected, since the quantizer approaches the ideal case with no quantization error. As a consequence, lowering the sampling frequency might increase the impact of jitter instead of decreasing it as has been assumed up to now. In fact, it is found that for a given set of modulator specifications, there is an optimum value for the sampling frequency that minimizes the in-band noise power dominated by jitter.
References


ANEXO 2: PRINCIPALES PUBLICACIONES SOBRE LOS TRABAJOS RECOGIDOS EN LA TESIS DOCTORAL

RESUMEN

Este anexo incluye cinco publicaciones del doctorando que constituyen la principal aportación a su trabajo de tesis doctoral. Tres de ellas han sido publicadas en revistas internacionales indexadas con índice de calidad relativo en “Journal Citation Reports” (JCR) en la categoría de “Electrical & Electronic Engineering”. Las otras dos publicaciones se corresponden con artículos presentados en el congreso “IEEE International Symposium on Circuits and Systems (ISCAS)”, que es el principal congreso organizado por la sociedad “Circuits and Systems” del IEEE, al que acuden habitualmente más de 1000 expertos en el área de Micro electrónica, y más concretamente de circuitos y sistemas - directamente relacionado con la temática de esta tesis doctoral. En todos los casos, las publicaciones han sido aceptadas tras ser sometidas a un proceso de revisión por pares.

Las referencias completas de las publicaciones incluidas son las siguientes:


PUBLICACIÓN 1

Título de la Publicación: A New High-Level Synthesis Methodology of Cascaded Continuous-Time ΣΔ Modulators

Autores: Ramón Tortosa, José M. de la Rosa, Francisco V. Fernández, Angel Rodríguez-Vázquez

Tipo de publicación: Revista internacional indexada con índice de calidad relativo

Nombre de la revista: Transactions on Circuits and Systems-II: Express Briefs

Editorial: IEEE

ISSN: 1057-7130

Indice de impacto: 0.922

Referencia completa de la publicación:


RESUMEN

Este artículo propone un método eficiente para la síntesis de moduladores ΣΔ en cascada implementados mediante técnicas de circuito de tiempo continuo. El método propuesto se basa en la síntesis de la cascada completa directamente en el dominio del tiempo continuo, en lugar de aplicando una transformación discreta-a-continua a un modulador de tiempo discreto equivalente, como se había hecho anteriormente a esta publicación.

Además de posibilitar una distribución óptima de los ceros del filtro del lazo, la metodología propuesta conduce a arquitecturas más eficientes en términos de la complejidad de la circuitería analógica, del consumo de potencia y de la robustez frente a los errores del circuito.
A VLSI High-Performance Priority Encoder Using Standard CMOS Library .............. S. Abdel-hafeez and S. Harb 597
A Low-Power Digit-Based Reconfigurable FIR Filter ........................................ K.-H. Chen and T.-D. Chiueh 617
VLSI Block Placement With Alignment Constraints ....................... S. Chen, S. Dong, X. Hong, Y. Ma, and C. K. Cheng 622
Robust Regularization for Normalized LMS Algorithms ..................... Y.-S. Choi, H.-C. Shin, and W.-J. Song 627
Modified Overlap Technique Using Fermat and Mersenne Transforms ............ R. Conway 632
Robust and Fuzzy Spherical Clustering by a Penalty Parameter Approach ................ H. Doğan and C. Güzeliş 637
An On-Sensor Bit-Serial Column-Parallel Processing Architecture for High-Speed Discrete Fourier Transform ................................ T. Eki, S. Kawahito, and Y. Tadokoro 642
IIP2 and DC Offsets in the Presence of Leakage at LO Frequency .............. I. Elahi, K. Muhammad, and P. T. Balsara 647
Complex Discretization Behaviors of a Simple Sliding-Mode Control System ................................ Z. Galias and X. Yu 652
A Novel Tunable Transconductance Amplifier Based on Voltage-Controlled Resistance by MOS Transistors ................................ I.-S. Han 662
New Curvature-Compensation Technique for CMOS Bandgap Reference With Sub-1-V Operation ................................ M.-D. Ker and J.-S. Chen 667
Time Encoding Machines With Multiplicative Coupling, Feedforward, and Feedback ................................ A. A. Lazar 672
On the Subband Orthogonality of Cosine-Modulated Filter Banks ..................... K. A. Lee and W. S. Gan 677
New Asymptotic Stability Criteria for a Two-Neuron Network With Different Time Delays ......................................................... S. Li, X. Liao, C. Li, and K. Wong 682
Frequency-Domain Analysis of Effects of the Location of a Feedback Resistor in a Current Feedback Amplifier .................... H. Lim and J. Park 687
Leakage Power Characteristics of Dynamic Circuits in Nanometer CMOS Technologies ................................ Z. Liu and V. Kursun 692

(Content Continued on Back Cover)
A Fully Multiplexed First-Order Frequency-Planar Module for Fan, Beam, and Cone Plane-Wave Filters .......... A. Madanayake and L. Bruton 697
Efficient Systolic Implementation of DFT Using a Low-Complexity Convolution-Like Formulation .......... P. K. Meher 702
Hardware-Efficient Systolization of DA-Based Calculation of Finite Digital Convolution ......................... P. K. Meher 707
Modeling of DC–DC Buck Converters for Large-Signal Frequency Response and Limit Cycles .................. K. Natarajan and M. Yektai 712
Winner-Take-All-Based Visual Motion Sensors ........................................ E. Özalevli, P. Hasler, and C. M. Higgins 717
Necessary and Sufficient Condition for a Class of Planar Dynamical Systems Related to CNNs to be Completely Stable ........................................ N. Takahashi and T. Nishi 727
A New High-Level Synthesis Methodology of Cascaded Continuous-Time ΣΔ Modulators ..................... R. Tortosa, J. M. de la Rosa, F. V. Fernández, and A. Rodríguez-Vázquez 739
An All-MOS High-Linearity Voltage-to-Frequency Converter Chip With 520-kHz/V Sensitivity .................. C.-C. Wang, T.-J. Lee, C.-C. Li, and R. Hu 744
An Efficient Implementation of the Delay Compensation for Sub-Band Filtered-x Least-Mean-Square Algorithm .............................................................. L. Wang, M. N. S. Swamy, and M. O. Ahmad 748
A Subspace Multiuser Beamforming Algorithm for the Downlink in Mobile Communications .......................................................... N. Wang, P. Agathoklis, and A. Antoniou 753
Blind Equalization of Nonirreducible Systems Using the CM Criterion ........................................ Y. Xiang, V. K. Nguyen, and N. Gu 758
Power Amplifier Selection for LINC Applications .................................................................................. J. Yao and S. I. Long 763
High-Performance Repetitive Control of PWM DC-AC Converters With Real-Time Phase-Lead FIR Filter ........................................................................ Y. Ye, K. Zhou, B. Zhang, D. Wang, and J. Wang 768
An Adaptive Predictor With Cascaded Forward-Backward Structure .............................................. H.-G. Yeh and M. Vaklev 773
Observer Design for Lipschitz Nonlinear Systems: The Discrete-Time Case ..................................... A. Zemouche and M. Boutayeb 777
A Differential CMOS T/R Switch for Multistandard Applications ........................................ Y. P. Zhang, Q. Li, W. Fan, C. H. Ang, and H. Li 782
Analysis of a Switched-Capacitor Second-Order Delta–Sigma Modulator Using Integrator Multiplexing ................................................................. C. M. Zierhofer 787

CALLS FOR PAPERS

Special Issue on Nanoelectronic Circuits and Nanarchitectures .......................................................... 792
ISCAS 2007 .......................................................................................................................................... 793
IEEE BIOCAS 2006 ............................................................................................................................ 794

Information for Authors .............................................................................................................................. 796
A New High-Level Synthesis Methodology of Cascaded Continuous-Time \(\Sigma\Delta\) Modulators

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Abstract—This brief presents an efficient method for synthesizing cascaded sigma–delta modulators implemented with continuous-time circuits. It is based on the direct synthesis of the whole cascaded architecture in the continuous-time domain instead of using a discrete-to-continuous time transformation as has been done in previous approaches. In addition to placing the zeroes of the loop filter in an optimum way, the proposed methodology leads to more efficient architectures in terms of circuitry complexity, power consumption and robustness with respect to circuit errors.

Index Terms—Analog–digital conversion, continuous-time sigma–delta (\(\Sigma\Delta\)) modulation.

I. INTRODUCTION

CONTINUOUS-TIME (CT) sigma–delta modulators (\(\Sigma\Delta\)Ms) are suited to analog-to-digital (A/D) interfaces in submicrometer CMOS [1]. Although most \(\Sigma\Delta\)Ms employ discrete-time (DT) circuits, CT techniques are applicable to broadband data communication systems due, among other features, to their intrinsic anti-aliasing filtering and their suitability for fast operation with low power consumption [2], [3].

Compared to DT-\(\Sigma\Delta\)Ms, a drawback of CT modulators is their higher sensitivity to some circuit errors, namely: clock jitter, excess loop delay and time constant tolerances [2], [3]. Among other things, the impact of these errors influences the choice of the architecture. Particularly, most reported CT-\(\Sigma\Delta\)Ms employ single-loop topologies [4], [5] to circumvent the larger impact of tolerances on cascaded architectures. However, some recent contributions demonstrate that cascaded CT-\(\Sigma\Delta\)M ICs are feasible and well suited to broadband applications [6]. This is significant because cascaded architectures have larger modularity and less stability problems than their single-loop counterparts for the same filtering order.

Different authors have addressed the synthesis of high-order cascaded CT-\(\Sigma\Delta\)Ms [7]–[9]. In all cases, the proposed methods are based on applying a DT-to-CT transformation to an equivalent DT topology that fulfils the required specifications. In most cases, the use of such transformation yields an increase of the analog circuit complexity, with the subsequent penalty in silicon area, power consumption, and sensitivity to parameter variations.

Fig. 1 shows the conceptual block diagram of a \(m\)-stage cascaded CT-\(\Sigma\Delta\)M. Each stage, consisting of a single-loop CT-\(\Sigma\Delta\)M (typically either second or first order), modulates a signal that contains the quantization error generated in the previous stage. Once in the digital domain, the stage outputs \(y_k\) are processed and combined by the cancellation logic so that only the quantization error of the last stage remains. Also, this error is shaped by a transfer function whose order equals the sum of the respective orders of all the stages in the cascade.

Cascaded CT-\(\Sigma\Delta\)Ms are typically synthesized from equivalent DT systems and use the same digital cancellation logic [8] as the DT prototype. This DT-to-CT equivalence can be guaranteed because at each stage the corresponding feedback transfer function from the quantizer output to the quantizer input is of discrete-time nature [2]. Assuming a rectangular impulsive response at the digital-to-analog converter (DAC), this equivalent DT loop filter transfer function is calculated as [10], [11]

\[
F(z) = \sum_{p_i} \text{Re} \left( \frac{F(s)}{s} e^{m_1 T_s z} \right) - \sum_{p_i} \text{Re} \left( \frac{F(s)}{s} e^{m_2 T_s z} \right)
\]

(1)

This brief presents a direct synthesis method for cascaded architectures. On the one hand, this method yields better placing of the noise transfer function zeroes and poles. On the other hand, it reduces the number of analog components. Thus, more robust and efficient architectures are obtained than when using DT-to-CT transformation. The method is illustrated in this brief through the synthesis of a 2-1-1-1 cascaded CT-\(\Sigma\Delta\)M for 12-bit at 40-MS/s.
where \( f_s = 1/T_s \) is the sampling frequency; \( m_1 = 1 - t_d/T_s \); \( m_2 = 1 - (t_d + \tau)/T_s \); \( t_d \) and \( \tau \) are, respectively, the time delay and pulsedwidth of the DAC waveform; \( p_i \) are the poles of \( F(s)/s \) and \( \text{Re}(\varphi) \) stands for the residue of \( \varphi \).

To get a functional CT-ΣΔM whose cancellation logic coincides with that of the original DT-ΣΔM, every state variable and DAC output must be connected to the integrator input of the ulterior stages in the cascade [8]. This increases the number of analog components (transconductors, amplifiers, and DACs) needed. For instance, Fig. 2(a) shows a cascaded 2-1-1 CT-ΣΔM obtained from an existing DT-ΣΔM [12]. Note that eight scaling coefficients \( (k_{2g-2a}) \) and their corresponding signal paths are needed to connect the different stages of the modulator. As a counterpart, if the CT-ΣΔM is directly synthesized by following the technique in this brief, the number of integrating paths can be reduced—see Fig. 2(b).

III. PROPOSED METHODOLOGY

Let us consider the more general case of the \( m \)-stage cascaded CT-ΣΔM shown in Fig. 1. The overall output \( y_o \) is given by

\[
y_o(z) = \sum_{k=1}^{m} y_k(z) C L_k(z)
\]

where \( y_k(z) \) and \( C L_k(z) \) denote, respectively, the output and the cancellation transfer function of the \( k \)-th stage.

If the modulator input \( x(t) \) is set to zero, the output of each stage can be written as

\[
y_k(z) = \frac{E_k(z) + \sum_{i=1}^{k-1} Z \left[ L^{-1}\left[H_D F_{ik}\right]_{[nT_s]}\right] y_k(z)}{1 - Z \left[ L^{-1}\left[H_D F_{kk}\right]_{[nT_s]}\right]}
\]

where \( Z \) stands for the \( z \)-transform, \( L^{-1} \) is the inverse Laplace transform, \( H_D = H_{DAC}(s) \) is the DAC transfer function, and

\[
F_{ij} = \frac{\text{Input Quantizer } j}{y_k(s)}
\]

represents the transfer function from \( y_k(s) \) to the input of the \( j \)-th quantizer [see Fig. 2(b)].

Using the notation \( Z[L^{-1}[H_D F_{km}]]_{[nT_s]} \equiv Z_{km} \), the output of each stage is given by

\[
y_k(z) = \frac{E_k(z)}{1 - Z_{kk}} + \sum_{i=1}^{k-1} Z_{ik} y_k(z)
\]

and the output of the modulator can be written as

\[
y_o = \sum_{k=1}^{m} y_k C L_k = \sum_{k=1}^{m} \left( \frac{E_k(z)}{1 - Z_{kk}} + \frac{1}{1 - Z_{kk}} \sum_{i=1}^{k-1} Z_{ik} y_k(z) \right) C L_k.
\]

The cancellation logic transfer function \( C L_k \) is calculated by annulling the quantization errors of the first \( m - 1 \) stages. This gives

\[
C L_k(z) = \frac{-Z_{km} C L_m}{1 - Z_{mm}} = \frac{-Z \left[ L^{-1}[H_D F_{km}]]_{[nT_s]} \right] C L_m(z)}{1 - Z \left[ L^{-1}[H_D F_{mm}]]_{[nT_s]} \right]}
\]

where the cancellation logic transfer function of the last stage, \( C L_m(z) \), can be chosen to be the simplest form that preserves the required noise shaping.

Note that the design equations (2)–(7) do not only take into account the single-stage loop filter transfer functions \( F_{ii} \), but also the inter-stage loop filter transfer functions \( F_{ij} \), \( i \neq j \). The latter are CT integrating paths appearing only when the modulator stages are connected to form the cascaded ΣΔM and must be included in the synthesis methodology to obtain a functional modulator with a minimum number of inter-stage paths. Therefore, the following systematic procedure can be proposed for the synthesis of cascaded CT ΣΔMs.1

1. First, the poles of the single-loop transfer functions \( F_{ii}(s) \) are optimally placed in the signal bandwidth for given specifications. The poles of the individual stages can be placed such that the overall pole distribution within the signal bandwidth is equivalent to that proposed in [13].

2. Secondly, each individual stage is optimized following a similar procedure as the one proposed in [14], that is, numerator coefficients in \( F_{ii} \) are optimized to maximize the resolution while maintaining the system stability. This process is carried out entirely in the CT domain and no equivalence to an existing DT modulator needs to be considered. Once \( F_{ii} \) are defined, \( F_{ij} \), \( i \neq j \) are automatically determined by the inter-stage integrating paths as outlined in Fig. 2(b).

3. Thirdly, once the individual stages are designed, (7) is used to obtain the cancellation transfer functions.

1In this procedure, the modulator order, oversampling ratio, and number of bits of internal quantizers are assumed to be determined for the given specifications from well-known expressions [1].
For illustration, the 2-1-1 CT-$\Sigma$ΔM of Fig. 2(b) was synthesized using (2)–(7) to achieve 16-bit resolution in a 750-kHz bandwidth, with a sampling frequency of 48 MHz (oversampling ratio $M = 32$) [12]. For simplicity, in order to facilitate the comparison of the performance of both modulators in Fig. 2, the coefficients of the first stage ($k_{i1}, k_{g1}, k_{f1}, k_{f2}$) are taken to be equal in both systems and are obtained from a DT-to-CT transformation of the first stage of the DT-$\Sigma$ΔM in [12]. The rest of the coefficients in Fig. 2(b) are chosen such that the time constant of the integrators is the inverse of the sampling frequency ($T_s = 1/f_s$). In summary

\[ k_{i1} = -k_{f1} = 1/4 \]
\[ k_{f2} = -3/8 \]
\[ k_{g1} = k_{i2} = -k_{f3} = k_{i3} = -k_{f4} = 1. \]  

(8)

Thus, the single-loop and inter-stage transfer functions are

\[ F_{11} = -\left(\frac{3T_s}{8}s + \frac{1}{4}\right) \]
\[ F_{22} = F_{33} = \frac{1}{sT_s} \]
\[ F_{13} = -\left(\frac{3T_s}{8}s + \frac{1}{4}\right) \]
\[ F_{23} = \left(\frac{1}{sT_s}\right)^2 \]

(9)

and the cancellation logic transfer functions can be calculated using (7)–(9). Considering a nonreturn-to-zero (NRZ) DAC, the following are obtained:

\[ CL_1 = \frac{z^{-1}}{48}(7 + 2z^{-1} - 7z^{-2} - 5z^{-3}) \]
\[ CL_2 = z^{-1}((1 + z^{-1})(1 - z^{-1})^2 \]
\[ CL_3 = 2(1 - z^{-1})^3 \]

(10)

where $CL_3$ is chosen to have three zeroes at dc, corresponding to the zeroes contributed by the first three integrators.

To compare the robustness of both modulators in Fig. 2, the effect of mismatch on the signal-to-noise ratio (SNR) was simulated using SIMSIDES—a SIMULINK-based time-domain behavioral simulator for $\Sigma$ΔMs [15]. For this purpose, maximum values of mismatch were estimated for a 0.18-$\mu$m CMOS technology. On the one hand, capacitor mismatch ($\sigma_C$) lower than 1% are standard in modern technologies. On the other hand, MOS transconductance mismatch ($\sigma_{gm}$) is related to drain current mismatch ($\sigma_{Id}$) by the following expression:

\[ 2\sigma_{gm}/gm = \sigma_{Id}/Id. \]

(11)

In the case of the 0.18-$\mu$m technology addressed, assuming typical transistor sizes and a maximum spacing between transistors of 1500 $\mu$m, a maximum $\sigma_{Id}/Id \leq 2\%$ is obtained. Then, taking into account that in a linearized transconductor, a minimum of 4 transconductance elements are used and that the tuning circuit introduces an additional error, maximum values of $\sigma_{gm}/gm \leq 2.5\%$ are expected.

Both modulators in Fig. 2 were simulated considering a $G_m$-C implementation. The results are shown in Fig. 3, where the SNR loss is represented as a function of $\sigma_{gm}$ and $\sigma_C$. For each point of these surfaces, 150 simulations were carried out using random variations with the corresponding standard deviations. The value of the SNR loss represented in Fig. 3 stands for the difference between the ideal SNR, i.e., with no parameter variation, and the SNR with 90% of the 150 simulations above it. It is shown that the lower analog component count in Fig. 2(b) is reflected in a lower variance of the modulator coefficients, leading to better behavior in terms of sensitivity to mismatch.

The same reasoning can be applied to the requirements in terms of dc gain of the transconductors. Since the number of transconductors connected to the same node is higher in the previous method, the equivalent impedance associated with these nodes tends to be lower and the requirement in terms of the individual transconductor output impedance is higher. Therefore, a higher dc gain is needed. Fig. 4 illustrates this point. Note that the SNR-peak starts dropping at a dc gain $\geq 5$ dB higher in the case of the system designed following the previous method. For high dc gains, the two curves collide because the effect of this error becomes negligible.

IV. SYNTHESIS EXAMPLE

As an application of the proposed methodology, the 2-1-1-1 cascaded CT-$\Sigma$ΔM shown in Fig. 5 was synthesized to achieve 12-bit resolution within a 20-MHz signal bandwidth. In order to fulfill these specifications without being limited by the clock jitter error, the sampling frequency, $f_s$, and the number of bits of
the internal quantizers (and DACs), $B$, must be properly chosen. In the case of a fifth-order modulator like the one shown in Fig. 5, the in-band jitter noise power is minimized for $f_s = 240$ MHz and $B = 4$ [16].

Another critical source of error in CT $\Sigma\Delta$Ms is the excess loop delay. As shown in [17], this error can be compensated for by adding an extra feedback branch between the output and the input to the quantizer (DAC2 in Fig. 5) and two D-latches. By adding this extra branch with the appropriate gain, the loop impulse response is exactly the same as that of the original. This extra feedback term can be easily included in the calculation of the cancellation logic by modifying appropriately the $F_{ij}$ transfer functions. In practice, this extra feedback branch will only affect the cancellation logic if the input to other stages is tapped at quantizer inputs or if the last stage includes a second DAC. In a practical implementation it might be advantageous to make DAC2 programmable [5].

Considering the factors above, the 2-1-1-1 architecture in Fig. 5 was synthesized using the methodology described in Section III. The first stage is formed by a resonator which has its pole placed at $\omega_p = 2\pi \sqrt{7/9B_{sw}}$, minimizing the quantization noise transfer function in the signal bandwidth, $B_{sw}$. Resistor variations can be tuned out using a combination of a discrete rough tuning of the resistors ($R_{R1}$, $R_{fb}$ and $R_i$) and a continuous fine tuning of the transconductors $k_{ff}$ and $k_{gl}$. This tuning can also be used to cancel the effect of finite gain-bandwidth product (GB) of the front-end opamp, due to the fact that this error can be modelled as an integrator gain error [5]. All the other transconductors could be tuned in order to keep the time constant $C/g_m$ unchanged over $C$ variations. In this case, the single-loop and inter-stage transfer functions are

$$F_{11} = -\frac{b_{11}s + b_{10}}{s^2 + \omega_p^2}$$

$$F_{ii} = -\frac{1}{T_i s^i}, \quad i = 2, 3, 4$$

$$F_{14} = -\frac{b_{10}}{(T_i s)^3 (s^2 + \omega_p^2)}$$

$$F_{24} = -\frac{1}{(T_i s)^3}$$

$$F_{34} = -\frac{1}{(T_i s)^2}$$

where

$$\omega_p = \sqrt{\frac{k_{gl}}{R_i C_1 C_2}}$$

and coefficients $b_{11}$, $b_{10}$, and $b_{10}$ are given by

$$b_{11} = \frac{k_{ff}}{R_{fb} C_1}; \quad b_{10} = \frac{k_{ff} k_{gl}}{R_{fb} C_1 C_2}; \quad b'_{10} = \frac{k_{gl}}{R_{fb} C_1 C_2}.$$  (14)

These coefficients are found through an iterative simulation-based process that optimizes the first stage of the modulator in order to maximize the SNR while maintaining stability. The outcome of this process—done entirely in the CT domain—is summarized in Table I. This table includes the values of loop filter coefficients, $k_i$ (implemented as transconductances) as well as the capacitances, $C_i$, and resistances, $R_i$ obtained from the optimization process. The expressions of $CL_4$, can be obtained from (7) and (12), giving

$$CL_4 = -z^{-1}(n_{14} + n_{13} z^{-1} + n_{12} z^{-2} + n_{11} z^{-3} + n_{10} z^{-4})$$

$$CL_2 = \frac{1}{6} z^{-1}(1 + 4z^{-1} + z^{-2}) \times (1 - 2\cos(T_{sw} p) z^{-1} + z^{-2})$$

$$CL_3 = \frac{1}{2} z^{-1}(1 + z^{-1})(1 - z^{-1}) \times (1 - 2\cos(T_{sw} p) z^{-1} + z^{-2})$$

$$CL_4 = (1 - z^{-1})^2 (1 - 2\cos(T_{sw} p) z^{-1} + z^{-2})$$  (15)

### Table I: Modulator Design Values

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>$R_{R1}$</td>
<td>1 MΩ</td>
</tr>
<tr>
<td>$R_i$</td>
<td>2.9 kΩ</td>
</tr>
<tr>
<td>$k_{zz}$</td>
<td>50 μA/V</td>
</tr>
<tr>
<td>$k_{11}$</td>
<td>500 μA/V</td>
</tr>
<tr>
<td>$k_{21}$</td>
<td>742 μA/V</td>
</tr>
<tr>
<td>$k_{31}$</td>
<td>820 μA/V</td>
</tr>
<tr>
<td>$k_{41}$</td>
<td>450 μA/V</td>
</tr>
<tr>
<td>$C_1$</td>
<td>7.5 pF</td>
</tr>
<tr>
<td>$C_1\ldots C_4$</td>
<td>1.875 pF</td>
</tr>
</tbody>
</table>
TABLE II
NONIDEALITIES CONSIDERED IN THE SIMULATION

<table>
<thead>
<tr>
<th>Non-idealities</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>Gain (dB)</td>
<td>660 MHz</td>
</tr>
<tr>
<td>Phase Margin</td>
<td>60°</td>
</tr>
<tr>
<td>Parasitics Input Capacitance</td>
<td>0.2 pF</td>
</tr>
<tr>
<td>Parasitics Output Capacitance</td>
<td>0.2 pF</td>
</tr>
<tr>
<td>Differential Output Swing</td>
<td>0.5 V</td>
</tr>
<tr>
<td>Resistor (Ω)</td>
<td>74.4kΩ</td>
</tr>
</tbody>
</table>

DC Gain | 50 dB |
Differential Input Amplitude | 0.3 V |
Differential Output Amplitude | 0.3 V |
VDD | 3.6 V |

Fig. 6. Output spectrum of the 2-1-1-1 CT $\Sigma\Delta$M in Fig. 5.

Fig. 7. SNDR versus input amplitude.

where coefficients $n_{ij}$ are given by

$$
\begin{align*}
\eta_{10} &= n_{14} = -\frac{b_0}{T_s^2 2^p} \left[ \sin(T_s \omega_p) - T_s \omega_p + \frac{1}{6} (T_s \omega_p)^3 \right] \\
\eta_{11} &= n_{12} = \frac{-b_0}{T_s^2 2^p} \left[ (T_s \omega_p)^3 \frac{2}{3} - \cos(T_s \omega_p) - 4 \sin(T_s \omega_p) \right] \\
\eta_{12} &= -\frac{b_0}{T_s^2 2^p} \left[ (T_s \omega_p)^3 \frac{1}{3} - 4 \cos(T_s \omega_p) + 1 \right] \\
&\quad - 2T_s \omega_p \left( 1 + 2 \cos(T_s \omega_p) \right) \\
&\quad - 2T_s \omega_p \left( 1 + 2 \cos(T_s \omega_p) \right)
\end{align*}
$$

The modulator in Fig. 5 was simulated using SIMSDESIDE, taking into account the non-ideal effects listed in Table II. Fig. 6 shows an output spectrum for a $-8$ dBV@6-MHz sinewave signal, demonstrating a correct operation within the signal bandwidth. The effective resolution is 76 dB (12.4 bits) as shown in Fig. 7, where the signal-to-noise-plus-distortion ratio (SNDR) is plotted as a function of the input signal amplitude.

V. CONCLUSION

This brief presents a new methodology for synthesizing cascaded continuous-time $\Sigma\Delta$Ms. The resulting circuits are less complex and more robust than those obtained with conventional methodologies. Examples supported by realistic behavioral simulations are given to validate the presented approach.

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PUBLICACIÓN 2

**Título de la Publicación:** Clock jitter error in multi-bit continuous-time sigma-delta modulators with non-return-to-zero feedback waveform

**Autores:** Ramón Tortosa, José M. de la Rosa, Francisco V. Fernández, Angel Rodríguez-Vázquez

**Tipo de publicación:** Revista internacional indexada con índice de calidad relativo

**Nombre de la revista:** Microelectronics Journal

**Editorial:** Elsevier

**ISSN:** 0026-2692

**Indice de impacto:** 0.859

**Referencia completa de la publicación:**


**RESUMEN**

Este artículo presenta un estudio detallado del error de “jitter” del reloj en moduladores ΣΔ de tiempo continuo con DAC NRZ. Se demuestra que la potencia de ruido en la banda de la señal causada por el jitter puede descomponerse en dos componentes fundamentales: una que depende la función de transferencia del filtro del lazo del modulador y la otra que depende de la amplitud y la frecuencia de la señal de entrada. Esta última componente, no considerada en estudios anteriores, permite predecir de forma precisa la pérdida de resolución ocasionada por el error de “jitter”, mostrando efectos que habían sido tenidos en cuenta en los estudios reportados con anterioridad a esta publicación, y que son especialmente críticos en aplicaciones de telecomunicaciones de banda ancha. El estudio que se presenta en este artículo se fundamenta en la formulación espacio-estado, lo que hace que el análisis sea general y aplicable a cualquier topología de moduladores tanto en cascada como de lazo simple. Como resultado del mismo se obtienen ecuaciones de diseño para la potencia del ruido integrado en banda como para la relación señal ruido. Dichas ecuaciones de pueden utilizar para optimizar las prestaciones del modulador en relación a las especificaciones a conseguir con un consumo de potencia y una potencia del error de “jitter” mínimos. Como validación del análisis se presentan simulaciones en el dominio del tiempo de diversas arquitecturas de moduladores con aplicación en VDSL.
Clock jitter error in multi-bit continuous-time sigma-delta modulators with non-return-to-zero feedback waveform

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Received 29 November 2006; received in revised form 18 September 2007; accepted 4 October 2007
Available online 26 November 2007

Abstract

This paper presents a detailed study of the clock jitter error in multi-bit continuous-time ΣΔ modulators with non-return-to-zero feedback waveform. It is demonstrated that jitter-induced noise power can be separated into two main components: one that depends on the modulator loop-filter transfer function and the other dependent on input signal parameters, i.e. amplitude and frequency. The latter component, not considered in previous approaches, allows us accurately to predict the resolution loss caused by jitter, showing effects not taken into account previously in literature despite the fact that they are especially critical in broadband telecom applications. Moreover, the use of state-space formulation makes the analysis quite general and applicable to either cascade or single-loop architectures. Closed-form expressions are derived for in-band error power and signal-to-noise ratio that can be used to optimize modulator performance in terms of jitter insensitivity. Time-domain simulations of several modulator topologies (both single-loop and cascade) intended for VDSL application demonstrate the validity of the presented approach.

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Keywords: Analog-to-digital conversion; Continuous-time ΣΔ modulation; Clock jitter

1. Introduction

Nowadays, the increasing demand for ever faster analog-to-digital converters (ADCs) in broadband communication systems has boosted the interest in continuous-time (CT) sigma-delta modulators (ΣΔMs). These modulators have intrinsic anti-aliasing filtering and the potential to operate at higher sampling rates and with lower power consumption than their discrete-time (DT) counterparts [1,2]. However, CT ΣΔMs are more sensitive than DT ΣΔMs to some circuit non-idealities. Particularly, their performance in high-speed applications is largely impacted by time uncertainties in the clock-signal edges, commonly referred to as clock jitter [1]. Clock jitter occurs at those points within the modulator architecture where signals are transformed from the CT-domain to the DT-domain and vice versa, i.e., at the sample-and-hold and reconstruction digital-to-analog converter (DAC), respectively. The error introduced by the sample-and-hold is attenuated within the signal band by the modulator noise-shaping effect, and can hence be neglected. However, the jitter error at the DAC occurs without attenuation at the input node thereby limiting modulator accuracy.

Jitter analysis of high-speed CT ΣΔMs has attracted significant interest in technical literature [1–7]. Most studies have addressed only the case of modulators with single-bit quantizers and return-to-zero (RZ) DACs whereas a much smaller number of studies have been focused on modulators employing multi-bit quantizers and non-return-to-zero (NRZ) DAC waveforms. This may be due to the fact that analysis of these multi-bit NRZ waveforms is mathematically more complex than their RZ counterparts. As a consequence, designers willing to use these waveforms have to rely on inexact semi-empirical estimations based on simulation results [1,7,8]. To the best of the authors’
knowledge, only the work in [7] addresses the case of NRZ DACs. However, in [7] some effects are not considered which, as shown in this paper, might become critical in medium-to-high-frequency applications.1

Despite the lack of theoretical coverage, multi-bit quantizers and NRZ DACs are appealing for practical usage because they have low sensitivity to jitter. Many of the recently reported prototypes for medium-to-high resolutions (11–14 bit) and large signal bandwidths (1–15 MHz) employ either multi-bit quantizers, or NRZ DACs, or both [9,10]. This paper is basically aimed at bridging the gap between theory and practice by providing an analytical coverage of jitter error in multi-bit CT ΣΔMs with NRZ DACs. As compared to [7] both the effect of the modulator loop-filter transfer function and that of the input signal are covered herein.

We use state-space formulation [11] to derive closed-form relations between jitter error, sampling frequency, modulator specifications (resolution and signal bandwidth), circuit topology (loop-filter transfer function and number of bits of the internal quantizer) and input signal parameters (amplitude and frequency). This state-space formulation is general, architecture-independent, and can be applied to any kind of CT ΣΔMs either cascade or single-loop.

The study described in this paper highlights effects not covered by previous approaches; effects that are significant for medium-to-high-frequency applications. As the number of bits of the internal quantizer increases, the signal-dependent term dominates over the modulator-dependent term, as it would be expected, since the quantizer approaches the ideal case with no quantization error. As a consequence, lowering the sampling frequency might increase the impact of jitter instead of decreasing it as has been assumed up to now. In fact, it is found that for a given set of modulator specifications, there is an optimum value for the sampling frequency that minimizes the in-band noise power dominated by jitter.

This paper is organized as follows. Section 2 describes a model for the jitter effect on CT ΣΔMs, with emphasis on those architectures using NRZ DACs. Section 3 applies the state-space formulation to derive closed-form expressions for the in-band noise power and the signal-to-noise ratio dominated by the jitter error. Section 4 compares those expressions with previous approaches. Finally, Section 5 shows several time-domain simulations of different modulators using both single-loop and cascade topologies in order to validate the theoretical predictions given by the presented approach.

1Basically, jitter error contains two terms: one associated with the input signal and the other associated with the modulator loop transfer function. However, the work in [7] takes only into account the loop filter dependency in order to optimize the design of the loop filter in terms of jitter.

2Note that Fig. 1 is a conceptual representation of a generic single-loop CT ΣΔM. However, the analysis presented here is still valid for other architectures, like high-order cascade topologies. Indeed, the results of this study have been incorporated into a new system-level synthesis methodology for cascade CT ΣΔMs [12], which has been recently applied to the design of a cascade 3–2 (4-bit) CT ΣΔMs [13].

3In DT modulators the sampler is at the input and all signals in the loop are DT.

4In order to simplify the notation, \( y(n_T) \) is written as \( y(n) \) with \( T \) being the sampling period.

2. Modeling clock jitter error in CT ΣΔMs with NRZ DACs

Fig. 1 shows the conceptual block diagram of a single-loop CT ΣΔM.2 The loop filter is CT and a CT-to-DT transformation is performed at the sampler placed after this filter.3 An inverse transformation, DT-to-CT, is performed at the DAC to obtain the CT feedback signal \( y(t) \) from the modulator output \( y(n) \).4 Jitter occurs at the points where these two transformations take place. On one hand, the error introduced at the sampler is subject to the same processing (assuming linear models) as the quantization noise, and hence pushed out-of-band by the modulator noise-shaping effect. As a consequence its contribution within the signal band can be neglected. On the other hand, the error associated with the DAC directly adds to the input signal and therefore makes a significant contribution within the signal band.

Let us focus on the DAC jitter error. Fig. 2 illustrates how this error occurs in the time domain for RZ and NRZ multi-bit DAC feedback waveforms. Assume in both cases that the DAC output is a current, \( I_{DAC} \), and that the time uncertainty caused by jitter is represented by \( \Delta T(n) \). This time uncertainty produces a corresponding uncertainty in the total charge associated with the \( n \)th clock period,

\[
\Delta Q(n) \equiv \Delta I_{DAC}(n) \Delta T(n),
\]

where \( \Delta I_{DAC}(n) \) represents the amplitude of the signal transition at the edge of the period. Note in Fig. 2 that, since the output signal \( I_{DAC} \) in a RZ DAC goes to zero at each clock cycle, signal transition amplitudes are larger for RZ, \( \Delta I_{DAC}(n)_{RZ} = I_{DAC}(n) \), than for NRZ DACs, \( \Delta I_{DAC}(n)_{NRZ} = I_{DAC}(n) - I_{DAC}(n-1) \). Also, as the number of bits in the quantizer increases, \( |\Delta Q(n)| \) decreases for NRZ DACs but remain practically unchanged for RZ DACs.

A DAC output waveform with jitter can be represented as the sum of an unjittered output waveform and a stream...
of pulses with amplitude $\Delta I_{DAC}(n)$ and width $\Delta T(n)$—often referred to as jitter error sequence [1]. In the case of a NRZ DAC, the jitter error sequence can be related to the modulator output signal by [14]

$$\nu(n) \approx [y(n) - y(n - 1)] \frac{\Delta T(n)}{T_s},$$

(2)

where $T_s$ is the sampling period. Assuming that $\Delta T(n)$ corresponds to a stationary process with zero mean and standard deviation $\sigma_{\Delta T}$, the power of the jitter error signal can be expressed as

$$P_{\nu} = E[\nu^2] = \frac{\sigma_{\Delta T}^2}{T_s^2} E[[y(n) - y(n - 1)]^2],$$

(3)

where $E[\cdot]$ represents the mathematical operator expectation [15].

The following definition will be used:

$$y(n) = x(n) + q(n),$$

(4)

i.e., the output $y(n)$ can be mathematically expressed as the combination of the input signal $x(n)$ and an error signal $q(n)$. Using (4), $E[[y(n) - y(n - 1)]^2]$ is expanded as follows:

$$E[[y(n) - y(n - 1)]^2] = E[[x(n) - x(n - 1)]^2] + 2E[[x(n) - x(n - 1)]q(n) - q(n - 1)].$$

Assuming that $x(n)$ and $q(n)$ are uncorrelated, (5) can be simplified to:

$$E[[y(n) - y(n - 1)]^2] \approx E[[x(n) - x(n - 1)]^2] + E[[q(n) - q(n - 1)]^2] = E[\Delta x(n)^2] + E[\Delta q(n)^2],$$

(6)

where $\Delta x_n \equiv x(n) - x(n - 1)$ and $\Delta q_n \equiv q(n) - q(n - 1)$.

The equation above contains two terms. The first one depends on the input signal. Considering a sinewave input signal of amplitude $A$ and angular frequency $\omega_i = 2\pi f_i$, this term $\Delta x_n$ can be simplified as

$$\Delta x_n \approx \frac{\sin(\omega_i T_s)}{2\pi f_i T_s}$$

and hence,

$$E[(\Delta x_n)^2] \approx T_s^2 A^2 \omega_i^2 E[\cos(\omega_i T_s)]^2 = T_s^2 A^2 \omega_i^2 \frac{1}{2}.$$

(8)

Regarding the second term in (6), the following approximate expression is derived in Appendix A:

$$E[(\Delta q_n)^2] \approx E\{[Z^{-1}(1 - z^{-1})N_{TF}(z) e(z)]^2\}$$

$$= \frac{X_{FS}^2}{12(2^B - 1)^2} \times \int_0^\pi \frac{1}{(1 - e^{-j\omega})N_{TF}(1 - e^{-j\omega})^2} d\omega,$$

(9)

where $X_{FS}$ is the full scale, $B$ is the number of bits of the internal quantizer, $N_{TF}(z)$ is the noise transfer function and $e(z)$ is the $Z$-transform of the quantization error.

From (3), (8) and (9), we obtained

$$P_{\nu} \approx \left(\frac{\sigma_{\Delta T}}{T_s}\right)^2$$

$$\times \left(\frac{A^2 \omega_i^2}{2f_s} + \frac{X_{FS}^2}{12(2^B - 1)^2} \frac{1}{\pi} \int_0^\pi \frac{1}{(1 - e^{-j\omega})N_{TF}(1 - e^{-j\omega})^2} d\omega\right),$$

(10)

where $f_s = 1/T_s$ is the sampling frequency.

Depending on the actual modulator topology, the integration in (9) and hence the calculation of the second term in (10) may become too involved. Instead, $E[(\Delta q_n)^2]$ can be calculated analytically by using the state-space formulation shown in the next section. State-space formulation provides a framework to study all types of modulators. Most important, it allows the study of jitter-induced noise in the time domain and extract the noise autocorrelation function [6].

3. State-space formulation

Let us consider the conceptual block diagram in Fig. 1. Using the impulse-invariant transformation [16], the DT equivalent of the loop-filter transfer function can be
written as

\[
G(z) = \frac{n_{L-1}z^{L-1} + \cdots + n_1z + n_0}{d_Lz^L + d_{L-1}z^{L-1} + \cdots + d_1z + d_0},
\]

(11)

where \(n_i\) and \(d_i\) are function of the coefficients of the original CT modulator loop filter, \(G(s)\). Therefore, \(N_{TF}(z)\) can be derived from (11) as

\[
N_{TF}(z) = \frac{1}{1 + G(z)} = \frac{d_Nz^L + d_{N-1}z^{L-1} + \cdots + d_1z + d_0}{d_Lz^L + (d_{L-1} + n_{L-1})z^{L-1} + \cdots + (d_1 + n_1)z + (d_0 + n_0)}
\]

\[
= \frac{d_Lz^L + (d_{L-1} + n_{L-1})z^{L-1} + \cdots + (d_1 + n_1)z + (d_0 + n_0)}{d_L + d_{L-1}z^{-1} + \cdots + d_1z^{-(L-1)} + d_0z^{-L}}
\]

\[
= d_L + (d_{L-1} + n_{L-1})z^{-1} + \cdots + (d_1 + n_1)z^{-(L-1)} + (d_0 + n_0)z^{-L}.
\]

(12)

Fig. 3 shows the transpose of the Direct II implementation of (12) [15]. This block diagram does not have any direct correspondence with the physical implementation of the modulator and is only used to represent the relationship between the input \(e(n)\), output \(q(n)\) and state variables of \(N_{TF}(z)\). The so-called state-space representation of \(N_{TF}(z)\) can be implemented by the block diagram in Fig. 4, which is described by the following finite difference equations [15]:

\[
\begin{align*}
\overline{v}(n+1) &= \overline{F}_0 \cdot \overline{v}(n) + \overline{p}_0 \cdot e(n), \\
n(n) &= \overline{g}_0^T \cdot \overline{v}(n) + e(n),
\end{align*}
\]

(13)

where \(F_0\) is the state matrix, \(\overline{v}(n)\) is the \(L \times 1\) state vector, \(\overline{p}_0\) and \(\overline{g}_0\) are \(L \times 1\) vectors, respectively, given by

\[
\overline{F}_0 = \begin{bmatrix}
0 & 0 & 0 & \cdots & 0 & -n_0/d_L \\
1 & 0 & 0 & \cdots & 0 & -n_1/d_L \\
0 & 1 & 0 & \cdots & 0 & -n_2/d_L \\
\vdots & \vdots & \vdots & \ddots & \vdots & \vdots \\
0 & 0 & \cdots & \cdots & \cdots & \cdots \\
0 & 0 & 0 & \cdots & 1 & -n_{L-1}/d_L
\end{bmatrix},
\]

\[
\overline{p}_0 = \begin{bmatrix}
n_0 \\
n_1 \\
\vdots \\
n_{L-1}
\end{bmatrix}/d_L,
\]

\[
\overline{g}_0 = \begin{bmatrix}
0 \\
0 \\
\vdots \\
1
\end{bmatrix}.
\]

(14)

\[
\begin{align*}
\overline{v}(n+1) &= \overline{F}_0 \cdot \overline{v}(n) + \overline{p}_0 \cdot e(n), \\
n(n) &= \overline{g}_0^T \cdot \overline{v}(n) + e(n),
\end{align*}
\]

(15)

3.1. Expectation value of \((\Delta q_n)^2\)

To compute the power of the jitter error from (2) it is necessary to derive the mathematical expectation of \((\Delta q_n)^2\), given by

\[
E((\Delta q_n)^2) = E[(q(n) - q(n-1))^2] = 2[E(q(n)^2) - E(q(n)q(n-1))],
\]

(16)

where the fact that \(E(q(n)^2) = E(q(n-1)^2)\) has been taken into account.

It is demonstrated in Appendix B that \(E((\Delta q_n)^2)\) is given by

\[
E((\Delta q_n)^2) = 2E(e(n)^2) \left( 1 - \overline{g}_0^T \cdot \overline{p} + \sum_{k=0}^{L} \sum_{j=1}^{L} g_k p_j \bar{\lambda}_k^{j-1} \overline{\lambda}_j^{-1} \frac{\overline{\lambda}_k^{j-1} \overline{\lambda}_j^{-1}}{1 - \overline{\lambda}_k^{j-1} \overline{\lambda}_j^{-1}} \right),
\]

(17)

where \(L\) is the order of \(N_{TF}\), \(\lambda_i\) are the eigenvalues of \(\overline{F}_0\) and \(q_i\) and \(p_i\) are, respectively, the elements of \(g_0^T = \overline{g}_0^T \cdot \bar{T} \) and \(p = \overline{p} \cdot \overline{p}_0\), being \(\bar{T}\) the matrix of the eigenvectors of \(\overline{F}_0\).

Taking into account that

\[
E(e(n)^2) = \frac{X_{\bar{c}}^2}{12(2^R - 1)^2},
\]

(18)
Expression (17) can be rewritten as
\[ E(\Delta q_n^2) = \frac{X_{FS}^2}{6(2^B - 1)} \psi(g, p, \bar{\lambda}, L), \] (19)
where
\[ \psi(g, p, \bar{\lambda}, L) = 1 - g^T \cdot \bar{p} + \sum_{k=1}^{L} \sum_{j=1}^{L} g_k p_i g_j \bar{p}_j \frac{j_{k-1}^j - j_{k-1}^{j-1}}{1 - j_{k-1}^j}. \] (20)

The above expression gives a direct method to calculate \( E(\Delta q_n^2) \), and hence \( P_e \) from the eigenvalues of a \( L \times L \) matrix, which involves the summation of \( L^2 \) terms, normally with \( L < 5 \).

### 3.2. In-band noise power and signal-to-noise ratio

Replacing (9) with (19) in (10), the jitter noise power is given by
\[ P_e = \frac{\sigma_{AT}^2}{T^2} \left[ T^2 A^2 \sigma_v^2 \psi(g, p, \bar{\lambda}, L) \right]. \] (21)

Taking into account that \( \Delta T(n) \) is a Gaussian random process, and that \( \Delta Y_n \equiv [y(n) - y(n - 1)] \) is not correlated with \( \Delta T(n) \), the error power computed using (21) can be assumed to be a white noise source at the input of the modulator. Therefore, the in-band noise power can be written as
\[ P_{\text{in-band}} = (\sigma_{AT})^2 B_w \left[ \frac{A^2 \sigma_v^2}{f_s} + \frac{X_{FS}^2}{6(2^B - 1)} \psi(g, p, \bar{\lambda}, L) \right], \] (22)
where \( B_w \) is the signal bandwidth.

The in-band noise power sets the accuracy which the modulator can attain. This accuracy can be alternatively formulated in terms of SNR,
\[ \text{SNR}_{\text{jitter}} = \frac{A^2}{2P_{\text{in-band}}}. \] (23)

Depending upon whether the in-band noise power is dominated only by the jitter terms or also includes the quantization error noise power one obtains, respectively,
\[ \text{SNR}_{\text{jitter}} = 10 \log \frac{A^2}{2B_w(\sigma_{AT})^2 \left[ \frac{A^2 \sigma_v^2}{f_s} + \frac{X_{FS}^2}{6(2^B - 1)} \psi(g, p, \bar{\lambda}, L) \right]}. \] (24)

\[ \text{SNR} = \frac{A^2}{2B_w(\sigma_{AT})^2 \left[ \frac{A^2 \sigma_v^2}{f_s} + \frac{X_{FS}^2}{6(2^B - 1)} \psi(g, p, \bar{\lambda}, L) \right]}. \] (25)

where \( \text{SNR}_{\text{jitter}} \) corresponds to the case dominated by jitter, and \( \text{SNR} \) corresponds to the more general case where an uncorrelated quantization noise term \( P_{Q,\text{band}} \) is added to the jitter term to obtain the total in-band noise \( P_{\text{in-band}} = P_{\text{jitter}} + P_{Q,\text{band}} \).

Note that in (22) and (25) the primary time uncertainty \( (\sigma_{AT})^2 \) is multiplied by two different factors which added together define the hereinafter called Jitter Amplification Factor, namely:

- the signal-dependent term (SDT), that depends on the input signal parameters \( A \) and \( \omega_n \), and sampling frequency:
\[ \text{SDT} = \frac{A^2 \omega_v^2}{f_s}. \] (26)

- and the modulator-dependent term (MDT), that depends on the modulator topology parameters \( B, X_{FS} \) and \( \psi(g, p, \bar{\lambda}, L) \), and sampling frequency:
\[ \text{MDT} = \frac{X_{FS}^2}{3(2^B - 1)} \psi(g, p, \bar{\lambda}, L). \] (27)

Note also that the latter term increases with \( f_s \) while the former decreases with \( f_s \). This suggests that a value can be found that minimizes the jitter amplification factor.

Consider for illustration the third-order single-loop CT \( \Sigma \Delta \)M depicted at conceptual level in Fig. 5. Several modulators with different numbers of bits in the internal quantizer (2b, 4b and 6b) have been studied. Table 1 shows the values of the loop-filter coefficients as well as the position of the pole and Table 2 shows the values of \( g_n, p_i \) and \( \bar{\lambda}_n \) obtained from the state-space formulation. Fig. 6
plots the jitter amplification factor, together with its two constitutive terms, STD (common to all modulators) and MDT, as a function of $f_s$ for $f_i = B_w = 20$ MHz.

Several conclusions can be drawn:

- For the modulator with a 2 bit internal quantizer, jitter sensitivity is completely dominated by the modulator-dependent term. In this case, lowering the sampling frequency (while keeping constant $B_w$) yields an improvement in the in-band noise power.
- In the case of the modulator with a 4-bit internal quantizer, even though in the higher range of sampling frequency jitter-induced noise is still dominated by the modulator-dependent term, in the lower range the term dependent on the input signal becomes dominant. This means that improvement in the in-band noise power would be possible by lowering the sampling frequency down to a certain value below which noise power starts to raise again. In any case, dependency of jitter-induced noise on sampling frequency is reduced significantly with respect to the previous case.
- In the case of a 6-bit internal quantizer, the jitter amplification factor is dominated by the input signal-dependent term in most of the range under study. Note also that for the cases with 4 and 6 bit internal quantization, there is an optimum value of $f_s$ that minimizes the in-band jitter noise power and hence, maximizes SNR. Generally speaking, whenever jitter is the main limiting factor of a multi-bit CT ΣΔM with NRZ DAC, obtaining the minimum value of the jitter amplification factor provides a convenient criterion for deciding loop-filter parameters, sampling frequency and the number of bits in the internal quantizer for given specifications.

<table>
<thead>
<tr>
<th>Coefficient</th>
<th>Value, 2b mod.</th>
<th>Value, 4b mod.</th>
<th>Value, 6b mod.</th>
</tr>
</thead>
<tbody>
<tr>
<td>$\lambda$</td>
<td>0.031</td>
<td>-0.222</td>
<td>0.183</td>
</tr>
<tr>
<td></td>
<td>0.457+j0.497</td>
<td>0.123+j0.815</td>
<td>-0.635+j0.377</td>
</tr>
<tr>
<td></td>
<td>0.457-j0.497</td>
<td>0.123-j0.815</td>
<td>-0.635-j0.377</td>
</tr>
<tr>
<td>$\beta$</td>
<td>-3.048</td>
<td>-2.807</td>
<td>-1.195</td>
</tr>
<tr>
<td></td>
<td>0.146+j0.64</td>
<td>-0.352+j1.37</td>
<td>-1.883+j7.541</td>
</tr>
<tr>
<td></td>
<td>0.146-j0.64</td>
<td>-0.352-j1.37</td>
<td>-1.883-j7.541</td>
</tr>
<tr>
<td>$\gamma$</td>
<td>0.7</td>
<td>0.811</td>
<td>0.586</td>
</tr>
<tr>
<td></td>
<td>0.82</td>
<td>0.765</td>
<td>0.856</td>
</tr>
<tr>
<td></td>
<td>0.82</td>
<td>0.765</td>
<td>0.856</td>
</tr>
</tbody>
</table>

Fig. 6. Jitter components vs. $f_s$ for the modulator in Fig. 5. Note that the right vertical scale applies to the modulator with 2 bit quantization and the left scale to the rest of the cases.

Fig. 7. Block diagram of a single-bit second-order CT ΣΔM.
4. Comparison with previous approaches

The main interest of the analysis carried out in this paper lies in the availability of simple, yet accurate, analytical expressions for the jitter-induced in-band noise power. These expressions help designers to gain an insight into the operation of multi-bit CT $\Sigma$Ms with NRZ DACs. Among other things, this improved insight helps designers to better understand the impact of the input signal on the jitter error balance. As was shown in Fig. 6, different design regions can be defined based on the relative importance of the terms (26) and (27). It was also illustrated how, under certain conditions, jitter-induced noise could increase with decreasing sampling frequency. This therefore limits the bandwidth that can be effectively achieved in practice.

Table 3
Loop-filter coefficients of CT $\Sigma$Ms in Fig. 9

<table>
<thead>
<tr>
<th></th>
<th>CT $\Sigma$M1</th>
<th>CT $\Sigma$M2</th>
<th>CT $\Sigma$M3</th>
</tr>
</thead>
<tbody>
<tr>
<td>$k_{in}$</td>
<td>1.5</td>
<td>2</td>
<td>1.6</td>
</tr>
<tr>
<td>$k_{fb}$</td>
<td>$-1.5$</td>
<td>$-2$</td>
<td>$-1.6$</td>
</tr>
<tr>
<td>$k_{g1}$</td>
<td>1</td>
<td>1</td>
<td>1.6</td>
</tr>
<tr>
<td>$k_{g2}$</td>
<td>$-0.1$</td>
<td>0.37</td>
<td>$-0.24$</td>
</tr>
<tr>
<td>$k_{g3}$</td>
<td>0.6</td>
<td>1</td>
<td></td>
</tr>
<tr>
<td>$k_{r}$</td>
<td>0.5</td>
<td>1.2</td>
<td></td>
</tr>
<tr>
<td>$k_{ff1}$</td>
<td>1</td>
<td>1</td>
<td>1</td>
</tr>
<tr>
<td>$k_{ff2}$</td>
<td>0.5</td>
<td>1</td>
<td></td>
</tr>
<tr>
<td>$k_{in2}$</td>
<td>–</td>
<td>–</td>
<td></td>
</tr>
<tr>
<td>$k_{fb2}$</td>
<td>–</td>
<td>–</td>
<td></td>
</tr>
<tr>
<td>Poles</td>
<td>$\omega_1 = 0$, $\omega_2 = \sqrt{3/52}B_w$</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

Fig. 8. Comparison of theory and simulations for the modulator of Fig. 7.

Fig. 9. Multi-bit NRZ CT $\Sigma$Ms under study: (a) third-order single-loop and (b) cascade 2-1.
However, in spite of the practical relevance of such a limit, this effect has not been addressed in previous analysis.

Coverage provided by previous analyses, especially those in [3,7], are appropriate whenever the modulator term dominates the jitter amplification factor. This is generally the case with single-bit quantization where $E[(\Delta q_i)^2]$ dominates due to the much greater value of the quantization step $\Delta$. Let us consider for illustration purposes the single-bit second-order CT $\Sigma M$ of Fig. 7 with $f_i = B_m$, an input amplitude of 80% of the reference level, $f_s = 40 MHz$ and an oversampling ratio $M = f_s/(2B_m) = 64$.

In this case, the modulator-dependent term is more than one thousand times higher than the signal-dependent term. In other words, jitter sensitivity in this modulator is completely dominated by $E[(\Delta q_i)^2]$, making jitter-induced noise power practically independent of the input signal.

### Table 4
Values of $F_0^T$, $\pi_0^T$ and $\pi_0^T$ for the CT $\Sigma AM$s in Fig. 9

<table>
<thead>
<tr>
<th>CT $\Sigma AM$ before diagonalization</th>
<th>CT $\Sigma AM$ after diagonalization</th>
</tr>
</thead>
<tbody>
<tr>
<td>$F_0^T$</td>
<td>$\pi_0^T$</td>
</tr>
<tr>
<td>[0 0 $-0.208$]</td>
<td>[0 $-0.328$]</td>
</tr>
<tr>
<td>[1 1 $-0.198$]</td>
<td>[0 0 0.664 $-j0.438$]</td>
</tr>
<tr>
<td>[0 1 1001]</td>
<td>[0 0 0.664 $-j0.438$]</td>
</tr>
</tbody>
</table>

### Table 5
Simulated vs. theoretical predictions of $E[(\Delta q_i)^2]$

<table>
<thead>
<tr>
<th>Modulator</th>
<th>$f_i$ (MHz)</th>
<th>$A$ (V)</th>
<th>Clock jitter (ps)</th>
<th>Simulated ($10^{-2}$ $\Psi^2$)</th>
<th>Theory ($10^{-2}$ $\Psi^2$)</th>
</tr>
</thead>
<tbody>
<tr>
<td>CT $\Sigma AM$1</td>
<td>2.197</td>
<td>0.3</td>
<td>10</td>
<td>12.2</td>
<td>16</td>
</tr>
<tr>
<td>CT $\Sigma AM$1</td>
<td>8.79</td>
<td>0.3</td>
<td>10</td>
<td>12.1</td>
<td>16</td>
</tr>
<tr>
<td>CT $\Sigma AM$1</td>
<td>17.58</td>
<td>0.3</td>
<td>10</td>
<td>12.2</td>
<td>16</td>
</tr>
<tr>
<td>CT $\Sigma AM$1</td>
<td>8.79</td>
<td>0.1</td>
<td>10</td>
<td>11.2</td>
<td>16</td>
</tr>
<tr>
<td>CT $\Sigma AM$1</td>
<td>8.79</td>
<td>0.2</td>
<td>10</td>
<td>14.1</td>
<td>16</td>
</tr>
<tr>
<td>CT $\Sigma AM$1</td>
<td>8.79</td>
<td>0.3</td>
<td>10</td>
<td>12.2</td>
<td>16</td>
</tr>
<tr>
<td>CT $\Sigma AM$1</td>
<td>8.79</td>
<td>0.3</td>
<td>30</td>
<td>12.2</td>
<td>16</td>
</tr>
<tr>
<td>CT $\Sigma AM$2</td>
<td>2.197</td>
<td>0.3</td>
<td>10</td>
<td>1.21</td>
<td>1.2</td>
</tr>
<tr>
<td>CT $\Sigma AM$2</td>
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<td>0.3</td>
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<td>1.23</td>
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First stage CT $\Sigma AM$3: $f_i$ = 4 MHz, $A$ = 0.3 V, $B_m$ = 1 MHz, $f_s$ = 40 MHz, $M = f_s/(2B_m) = 64$.

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First stage CT $\Sigma AM$3: $f_i$ = 4 MHz, $A$ = 0.3 V, $B_m$ = 1 MHz, $f_s$ = 40 MHz, $M = f_s/(2B_m) = 64$.
Under these conditions, the equations derived in this paper provide similar predictions to the expressions reported in [3] for single-bit quantization, which is recalled here for comparison,

\[
\text{SNR}_{\text{jitter}} = 10 \log \left( \frac{1}{16M\sigma^2_{\Delta T}B_w^2} \right) \tag{28}
\]

and the analysis presented in [7]. This is illustrated in Fig. 8. On one hand, the curves at the top right-hand side depict the predictions made by the simplified expressions (24) and (28), respectively, showing good agreement. On the other hand, the bottom curves depict the predictions made by the previously shown Eq. (25) and by the analysis in [7], as well as the estimations made by simulations. The agreement is quite good. Fig. 8 also shows that within the region where the resolution is dominated by jitter the agreement between simplified and complete SNR estimations is reasonable.

As the signal-dependent term becomes first significant and eventually dominant, previous analyses fail to produce proper predictions. In the next section, it will be shown that when the oversampling ratio is reduced and the number of bits increased (as happens in broadband applications where the combination of high input bandwidth and technology limitations imposes a low oversampling ratio) behavior in terms of jitter sensitivity is not well described by previous approaches, while expressions derived in this study closely match modulator performance.

At the limit when the \(\text{SNR}_{\text{jitter}}\) is fully dominated by the signal-dependent term and the modulator-dependent term is negligible, the maximum resolution is calculated from (24) as

\[
\text{SNR}_{\text{MAX}} = 10 \log \left( \frac{f_s}{8\pi^2\sigma^2_{\Delta T}B_w^2} \right)^{\frac{1}{2}} = 10 \log \left( \frac{M}{4\pi^2\sigma^2_{\Delta T}B_w^2} \right)^{\frac{1}{2}}. \tag{29}
\]

where we have assumed that \(f_i = B_w\). This is a limit valid both for single-loop and cascade CT \(\Sigma\Delta\)Ms.\(^7\) This is also valid for any type of loop filter, since (29) is independent of the particular loop filter.

Note that exactly the same expression is obtained for DT \(\Sigma\Delta\)Ms [17]. In these modulators, this limit is established by the input sampler. In CT \(\Sigma\Delta\)Ms it is introduced by the feedback DAC. In fact, (29) reveals a limit that applies to any ADC, not only to those based on \(\Sigma\Delta\) modulation, and that is that no converter, when clocked with an imperfect signal, can perform better than an ideal sampler clocked with the same signal.

In summary, the analysis in this paper provides a more detailed coverage of practical design choices with application in broadband while at the same time serves as an extension to previous studies, covering cases not included in them.

\(^7\)In these cascade architectures, jitter-induced noise introduced in the first stage is not affected by later stages since they process only quantization errors.
5. Validation and application to VDSL

Fig. 9 shows two CT ΣΔMs used as illustrative case studies in this section. Fig. 9(a) is a third-order single-loop and Fig. 9(b) is a cascade 2-1 topology. Both architectures employ feed-forward stabilization and incorporate a feedback coefficient $k_i$ to move one of the poles to an optimum position. In this section the results of the analysis in this paper are compared to those obtained through detailed time-domain behavioral simulation using SIMSIDES, a SIMULINK-based simulator for ΣΔMs [18].

The modulators in Fig. 9 have been synthesized following the methodology described in [12] for VDSL application with $B_w = 20$ MHz. Three different cases are considered:

- CT ΣΔM1: Fig. 9(a) with $f_s = 400$ MHz and $B = 2$;
- CT ΣΔM2: Fig. 9(a) with $f_s = 160$ MHz and $B = 5$;
- CT ΣΔM3: Fig. 9(b) with $f_s = 160$ MHz and $B_1 = B_2 = 5$,

where $B_1$ and $B_2$ are the number of bits in the quantizer in the first and second stage of Fig. 9(b), respectively. Table 3 shows the values of the loop-filter coefficients, $k_i$, and the position of the poles for the three cases mentioned above. An optimum distribution of NTF zeros has been adopted as described in [19]. Table 4 shows the values of $F_0^{-1}$, $g_0^{-1}$ and $p_0^{-1}$ also for these three cases.

Table 5 compares the values of $E[(\Delta q)^3]$ extracted from simulations with those calculated using (19). Note that the simulated $E[(\Delta q)^3]$ are independent of the input signal and clock jitter, as predicted by (19). Fig. 10 shows several simulated output spectra of cases CT ΣΔM1 (Fig. 9(a)) and CT ΣΔM2 (Fig. 9(b)) corresponding to different values of $f_s$ and $\sigma_{jT} = 25$ ps. Note that in Fig. 10(a), the in-band noise power does not depend on $f_s$, in agreement with what is predicted by Hernandez et al. [7]. However, as $B$ increases from 2 to 5, the modulator-dependent term in (22) decreases and hence, the in-band noise becomes dominated by the signal-dependent term as illustrated in Fig. 10(b).

This effect is better shown in Fig. 11, where the SNR-peak of the modulators in Fig. 9 is plotted vs. $\sigma_{jT}$ for several values of $f_s$, showing simulation results and theoretical predictions. For comparison purposes, predictions given by Hernandez et al. [7] are also included. Note that simulated and theoretical data match very well when the combined effect of signal- and modulator-dependent jitter noise is taken into account.

Note that in Fig. 11(a), due to the fact that $f_s$ and $A$ are large, the jitter amplification factor is dominated by the modulator-dependent term, meaning that the SNR is practically independent of the input signal. However, when $B$ is increased and $f_s$ is decreased in order to improve jitter insensitivity, the resolution improves for low input frequencies, whereas for higher input frequencies this improvement is considerably reduced as shown in Fig. 11(b). The same behavior is obtained in Fig. 11(c),

Fig. 11. SNR vs. $\sigma_{jT}$ for different values of $f_s$: (a) CT ΣΔM1, (b) CT ΣΔM2, (c) CT ΣΔM3.
where jitter sensitivity is dominated by the first stage. It is important to note that this dependence on input signal, even though it might not be important in low bandwidth applications, can become dominant in broadband communications where the input frequency is high and designers resort to multi-bit implementations with low oversampling ratios.

6. Conclusions

The effect of clock jitter error on multi-bit CT ΣΔMs with NRZ DAC has been analyzed. Based on the use of state-space formulation, easy-to-compute closed-form expressions have been derived for the in-band noise power and signal-to-noise ratio. This study extends the application range of the derived expressions as compared with previous approaches. It provides mathematical tools to separate the two components of jitter-induced noise. It provides means that allow the designer to quantify how the modulator is going to be affected by jitter and facilitates the design optimization process. This optimization can be performed using (20) as a figure of merit in a iterative method. Furthermore, for low oversampling ratios, this study makes it possible to find out an optimum solution in terms of jitter sensitivity by using (24), where all modulator parameters, including modulator filter, sampling frequency and quantizer number of bits can be used to find a minimum in the in-band noise power. Predictions have been confirmed by time-domain simulations of several CT ΣΔMs for VDSL application.

Acknowledgments

This work has been supported by the Spanish Ministry of Science and Education (with support from the European Regional Development Fund) under contract TEC2004-01752/MIC.

Appendix A. Calculation of $E\{\Delta q(n)q(n)\}$

It is proved herein that a good approximation of $E\{\Delta q(n)q(n)\}$ can be calculated taking into account only quantization error. This approximation simplifies enormously any further analysis but needs justification since it is not necessarily applicable to every feedback system. It is shown that in the particular case of ΣΔ converters, it is a valid approximation and leads to accurate predictions. According to (2), the effect of clock jitter can be modeled as shown in Fig. 12.

For simplicity, the input to the modulator $x(t)$ is approximated by an ideally sampled version $x(n)$. With this assumption $G(s)$ can be replaced by $G(z)$ which is the DT equivalent calculated through the impulse-invariant transformation [16]. The equation governing the modulator is

$$x(z) + \frac{\Delta T(z)}{T_s} \otimes (1 - z^{-1})y(z) - y(z) \times G(z) + e(z) = y(z). \quad (30)$$

Taking into account that $y(z) = x(z) + q(z)$, the following equation is easily derived:

$$q(z) - \left[ \frac{\Delta T(z)}{T_s} \otimes (1 - z^{-1})q(z) \right] \frac{G(z)}{1 + G(z)} = \frac{\left[ (\Delta T(z)/T_s) \otimes (1 - z^{-1})x(z) \right] (1 - z^{-1})G(z)}{1 + G(z)} + \frac{e(z)}{1 + G(z)}. \quad (31)$$

In order to determine $E\{(q(n) - q(n-1))^2\}$, the equation in (31) is multiplied by $z^{-1}$ and subtracted from itself, giving:

$$(1 - z^{-1})q(z) - \left[ \frac{\Delta T(z)}{T_s} \otimes (1 - z^{-1})q(z) \right] \frac{(1 - z^{-1})G(z)}{1 + G(z)} = \frac{\left[ (\Delta T(z)/T_s) \otimes (1 - z^{-1})x(z) (1 - z^{-1})G(z) \right]}{1 + G(z)} - \frac{(1 - z^{-1})x(z) (1 - z^{-1})e(z)}{1 + G(z)}. \quad (32)$$

The expected value of both sides is calculated, starting with the term to the left of the equal sign:

$$E \left\{ Z^{-1} \left[ (1 - z^{-1})q(z) - \left[ \frac{\Delta T(z)}{T_s} \otimes (1 - z^{-1})q(z) \right] \right] \times \left( \frac{(1 - z^{-1})G(z)}{1 + G(z)} \right)^2 \right\} = E\{(q(n) - q(n-1))^2\}$$

$$+ E \left\{ Z^{-1} \left[ \frac{\Delta T(z)}{T_s} \otimes (1 - z^{-1})q(z) \right] \frac{(1 - z^{-1})G(z)}{1 + G(z)} \right\}^2 \right\} - 2E \left\{ (q(n) - q(n-1))Z^{-1} \left[ \frac{\Delta T(z)}{T_s} \otimes (1 - z^{-1})q(z) \right] \right\} \times \left( \frac{(1 - z^{-1})G(z)}{1 + G(z)} \right) \right\}. \quad (33)$$

Since $\Delta T(n)$ is a random signal with zero mean, it can be proven that the last term in (33) is zero. Considering the exact continuous-time signal can be used together with inverse Laplace and Z transforms making the analysis much more complicated. Since it is demonstrated above that input signal has no significant effect on the calculation of $E\{(q(n) - q(n-1))^2\}$, the exact analysis does not contribute anything and the approximation makes the analysis much simpler.

Fig. 12. Clock jitter model used in the mathematical derivations.
that 
\[ |G(z)| \frac{1}{1 + G(z)} = |S_{TF}(z)| \leq 1 \quad (34) \]
an upper bound for the second-last term in (33) can be estimated:
\[
E \left\{ \frac{\Delta T(n)}{T_s} \left[ (1 - z^{-1})q(z) \left( \frac{1 - z^{-1}}{1 + G(z)} \right) \right]^2 \right\} \\
\leq E \left\{ \frac{\Delta T(n)}{T_s} \left[ (1 - z^{-1})q(z) \right] \left( 1 - z^{-1} \right) \right\}^2 \\
= E \left\{ \frac{\Delta T(n)}{T_s} \left[ (1 - z^{-1})q(n) - q(n - 1) \right] \right\}^2 \\
= 2E \left\{ \frac{\Delta T(n)}{T_s} \right\}^2 E \left\{ (q(n) - q(n - 1))^2 \right\} \\
\leq E \left\{ (q(n) - q(n - 1))^2 \right\}. \quad (35) \]

Therefore, the term to the left of the equal sign in (32) can be approximated by
\[
EZ^{-1}(1 - z^{-1})q(z) = \left\{ \left( \frac{\Delta T(z)}{T_s} \right) \otimes (1 - z^{-1})q(z) \right\}^2 \approx E \left\{ (q(n) - q(n - 1))^2 \right\}. \quad (36) \]

The term on the right-hand side of (32) can be approximated following a similar procedure. First, taking into account that \( x(z) \) is restricted to the signal band where \( G(z) \to 0 \), the following approximation can be applied:
\[
\frac{1 - z^{-1}}{1 + G(z)} x(z) \approx 0 \quad (37) \]
leading to the following approximation:
\[
E \left\{ \frac{\Delta T(z)}{T_s} \left[ (1 - z^{-1})\frac{x(z)}{1 + G(z)} \left( 1 - z^{-1} \right)G(z) \right] \right\} \\
\approx E \left\{ \left( \frac{\Delta T(n)}{T_s} \right) \left[ (1 - z^{-1})x(n) - (1 - z^{-1})e(z) \right] \right\}^2 \\
= E \left\{ \frac{\Delta T(n)}{T_s} \left[ x(n) - x(n - 1) \right] \otimes Z^{-1} \left[ \frac{(1 - z^{-1})G(z)}{1 + G(z)} \right]^2 \right\} \\
+ E \left\{ \frac{\Delta T(n)}{T_s} \right\}^2 \left\{ Z^{-1} \left[ \frac{(1 - z^{-1})e(z)}{1 + G(z)} \right]^2 \right\}. \quad (38) \]

where the fact that \( \Delta T(n) \) is a random signal with zero mean has been used to drop one of arising terms. Using the approximation in (34), an upper bound for the second-last term in (38) can be evaluated:
\[
E \left\{ \frac{(x(n) - x(n - 1)) \otimes Z^{-1} \left[ \frac{(1 - z^{-1})G(z)}{1 + G(z)} \right]^2}{\frac{\Delta T(n)}{T_s}} \right\} \\
\leq E \left\{ \frac{(x(n) - x(n - 1)) \otimes Z^{-1} \left[ (1 - z^{-1}) \right]^2}{\frac{\Delta T(n)}{T_s}} \right\} \\
= E \left\{ \frac{(x(n) - x(n - 1))}{\frac{\Delta T(n)}{T_s}} \right\} \\
- \frac{\Delta T(n - 1)}{T_s} \left[ x(n - 1) - x(n - 2) \right]^2 \\
= 2E \left\{ \frac{\Delta T(n)}{T_s} \right\}^2 E \left\{ (x(n) - x(n - 1))^2 \right\} \approx \sigma_{\Delta T}^2 A^2 \omega_m^2, \quad (39) \]

where the same approximation as in (8) has been used.

The last part of this demonstration consists of proving that the last term in (39) satisfies the relation:
\[
\sigma_{\Delta T}^2 A^2 \omega_m^2 \leq E \left\{ \left( Z^{-1} \left[ \frac{(1 - z^{-1})e(z)}{1 + G(z)} \right] \right)^2 \right\}. \quad (40) \]

The proof starts with the definition of \( N_{TF}(z) \):
\[
E \left\{ \left( Z^{-1} \left[ \frac{(1 - z^{-1})e(z)}{1 + G(z)} \right] \right)^2 \right\} \\
= \frac{X_{FS}^2}{12(2^B - 1)^2} \int_0^\pi |1 - e^{-j\omega}|^2 |N_{TF}(e^{-j\omega})|^2 d\omega \\
\geq \frac{X_{FS}^2}{12(2^B - 1)^2} \int_0^\pi |1 - e^{-j\omega}|^2 |N_{TF}(e^{-j\omega})|^2 d\omega. \quad (41) \]

Using the fact that the out of band gain of \( N_{TF}(e^{-j\omega}) \) is greater than one, a lower bound for (41) can be estimated,
\[
E \left\{ \left( Z^{-1} \left[ \frac{(1 - z^{-1})e(z)}{1 + G(z)} \right] \right)^2 \right\} \\
> \frac{X_{FS}^2}{12(2^B - 1)^2} \int_0^\pi |1 - e^{-j\omega}|^2 d\omega \approx \frac{X_{FS}^2}{6(2^B - 1)^2} \\
\geq \frac{2A^2}{3(2^B - 1)^2} \sigma_{\Delta T}^2 A^2, \quad (42) \]

using the fact that the integral in (42) is \( \approx 2\pi \) for \( M \geq 4 \) and that the maximum input amplitude is \( A \leq X_{FS}/2 \). Now the following relation can be easily shown to hold even for extreme values of clock jitter and input signal,
\[
\frac{2A^2}{3(2^B - 1)^2} \geq \sigma_{\Delta T}^2 A^2. \quad (43) \]

\( B = 5, \sigma_{\Delta T} = 30 \text{ ps} \) and \( f_i = 30 \text{ MHz} \), the first term (43) is more than 20 times the second term.
Using Eqs. (39), (42) and (43) in (38), the following conclusion can be drawn:

\[
E[(\Delta q_n)^2] \cong E\{ (z^{-1}[1 - z^{-1}]N_{TF}(z)e(z))^2 \} \\
= \frac{X^2_{FS}}{12\pi(2^B - 1)^2} \int_0^\pi [(1 - e^{-\omega T})N_{TF}(e^{-\omega T})]^2 \, d\omega. \tag{44}
\]

**Appendix B. Mathematical expectation of \(|q(n)|^2\) in stable systems**

In order to derive an expression for \(E[(\Delta q_n)^2]\), it will be assumed in (15) that the initial state, \(\bar{v}(0)\), is zero. A non-zero initial state would lead to expressions of the form \(E[\text{constant} \cdot e(n)]\) which are zero by definition. With this, \(E[(\Delta q_n)^2]\) and \(E[q(n)q(n-1)]\) can be written, respectively, as:

\[
E[q(n)^2] = E\left\{ \left( \sum_{k=0}^{n-1} \bar{y}_0^T \cdot F_0^{n-k-1} \cdot \bar{p}_0 \cdot e(k) + e(n) \right) \right\} \\
\times \left( \sum_{k=0}^{n-1} \bar{y}_0^T \cdot F_0^{n-1-j} \cdot \bar{p}_0 \cdot e(j) + e(n) \right) \\
= \sum_{k=0}^{n-1} \sum_{j=0}^{n-1} \bar{y}_0^T \cdot F_0^{n-k-1-j} \cdot \bar{p}_0 \cdot F_0^{n-1-j} \cdot \bar{p}_0 \cdot E(k)e(j) \\
+ \sum_{k=0}^{n-1} y_0^T \cdot F_0^{n-k-1} \cdot \bar{p}_0 \cdot E(k)e(n) \\
+ \sum_{j=0}^{n-1} y_0^T \cdot F_0^{n-1-j} \cdot \bar{p}_0 \cdot E(j)e(n) + E(e(n)^2), \tag{45}
\]

\[
E[q(n)q(n-1)] = E\left\{ \left( \sum_{k=0}^{n-1} \bar{y}_0^T \cdot F_0^{n-k-1} \cdot \bar{p}_0 \cdot e(k) + e(n) \right) \right\} \\
\times \left( \sum_{k=0}^{n-1} \bar{y}_0^T \cdot F_0^{n-k-1} \cdot \bar{p}_0 \cdot e(k) \right) \\
= \sum_{k=0}^{n-1} \left[ \bar{y}_0^T \cdot F_0^{n-k-1} \cdot \bar{p}_0 \right]^2 \cdot E(k)e(n) \\
+ E(e(n)e(n-1)). \tag{46}
\]

Considering that \(E[e(k)e(j)] = 0\) for \(k \neq j\), (45) and (46) are, respectively, simplified into:

\[
E[q(n)^2] = E(e(n)^2) \left( 1 + \sum_{k=0}^{n-1} \left[ \bar{y}_0^T \cdot F_0^{n-k-1} \cdot \bar{p}_0 \right]^2 \right), \tag{47}
\]

\[
E[q(n)q(n-1)] = E(\bar{v}(n)\bar{v}(n-1)) \\
= E(e(n)^2) \times \left( \bar{y}_0^T \cdot \bar{p}_0 + \sum_{k=0}^{n-1} \bar{y}_0^T \cdot F_0^{n-k-1} \cdot \bar{p}_0 \cdot \bar{y}_0^T \cdot F_0^{n-1-k} \cdot \bar{p}_0 \right). \tag{48}
\]

Note that \(E(q(n)^2)\) and \(E(q(n)q(n-1))\) depend on the time instant, \(n\). However, it is demonstrated next that for a stable modulator, i.e., a system with a \(N_{TF}\) having all poles inside the unit circle, the value of \(E(q(n)^2)\) is independent of time, provided that a reasonable number of samples is used to derive (48). In order to demonstrate this, let us consider the state-space representation of \(N_{TF}(z)\) shown in Fig. 4, which can be described by the finite difference equations in (13).

After diagonalization, the equation system in (13) can be expressed as:

\[
\bar{v}(n+1) = \bar{F} \cdot \bar{v}(n) + \bar{p} \cdot e(n),
\]

\[
q(n) = \bar{g}^T \cdot \bar{v}(n) + e(n), \tag{49}
\]

where \(\bar{v}(n)\) is the state vector of the diagonalized system and \(\bar{F}, \bar{p}\) and \(\bar{g}\) are, respectively, given by:

\[
\bar{F} = T^{-1} \cdot F_0 \cdot \bar{T},
\]

\[
\bar{p} = T^{-1} \cdot \bar{p}_0 = \begin{bmatrix} p_1 \\ p_2 \\ \vdots \\ p_L \end{bmatrix},
\]

\[
\bar{g}^T = \bar{y}_0^T \cdot \bar{T} = \begin{bmatrix} g_1 & g_2 & \cdots & g_L \end{bmatrix}, \tag{50}
\]

where \(\bar{T}\) is the matrix formed by the eigenvectors of \(\bar{F}\), \(\lambda_j\) are the eigenvalues and \(L\) is the order of the modulator.

Once \(F_0\) has been diagonalized, the matrix product \(\bar{g}^T \cdot \bar{F}_0 \cdot \bar{p}_0\) can be written as:

\[
\left[ \bar{y}_0^T \cdot F_0^{n-k-1} \cdot \bar{p}_0 \right]^2 = \left[ \bar{g}^T \cdot \bar{T}^{-1} \cdot F_0^{n-k-1} \cdot \bar{T} \cdot \bar{p} \right]^2 \\
= \left[ \bar{g}^T \cdot \bar{T}^{-1} \cdot F_0 \cdot \bar{T} \right]^{n-k-1} \cdot \bar{p} \]

\[
= \left[ \bar{g}^T \cdot F_0^{n-1-k} \cdot \bar{p} \right] \sum_{i=1}^{L} g_i p_i \sum_{j=1}^{L} \bar{g}_j \lambda_i \bar{\lambda}_{ji}^{n-1-k} \bar{\lambda}_{ji}^{-1-k}. \tag{51}
\]

Taking into account (51), the summation in (47) can now be expressed as:

\[
\sum_{k=0}^{n-1} \left[ \bar{y}_0^T \cdot F_0^{n-k-1} \cdot \bar{p}_0 \right]^2 = \sum_{i=1}^{L} g_i p_i \sum_{j=1}^{L} \bar{g}_j \lambda_i \bar{\lambda}_{ji}^{n-1-k} \bar{\lambda}_{ji}^{-1-k}. \tag{52}
\]
Let us define the partial sums as

$$S_{nj} = \sum_{k=0}^{n-1} \frac{\lambda_i^{n-1-k} \lambda_j^{n-1-k}}{1 - \lambda_i^{n-1} \lambda_j^{-1}}.$$  \hspace{1cm} (53)

Multiplying (53) by \(\lambda_i^{-1} \lambda_j^{-1}\) and subtracting from the original, the following expression is obtained:

$$S_{nj} - \lambda_i^{-1} \lambda_j^{-1} S_{nj} = \lambda_i^{n-1} \lambda_j^{n-1} - \lambda_i^{-1} \lambda_j^{-1} = \frac{\lambda_i^{n-1} \lambda_j^{n-1} - \lambda_i^{-1} \lambda_j^{-1}}{1 - \lambda_i^{-1} \lambda_j^{-1}}.$$  \hspace{1cm} (54)

If the system is stable, \(|\lambda_i| < 1\), and hence \(S_{nj}\) has a finite limit given by

$$\lim_{n \to \infty} S_{ijn} = - \frac{\lambda_i^{-1} \lambda_j^{-1}}{1 - \lambda_i^{-1} \lambda_j^{-1}}.$$  \hspace{1cm} (55)

In practical cases, it has been observed that for \(n \geq 10\), \(S_{ijn}\) is very close to the limit given above. Using (55), the last summation in (52) can be expressed as

$$\sum_{k=0}^{n-1} \lambda_i^{n-1-k} \lambda_j^{n-1-k} = - \frac{\lambda_i^{-1} \lambda_j^{-1}}{1 - \lambda_i^{-1} \lambda_j^{-1}}.$$  \hspace{1cm} (56)

Finally, from (47), (52) and (56), the expected value of \(q(n)^2\) can be expressed as

$$E[q(n)^2] = E[e(n)^2] \left( 1 - \sum_{k=1}^{L} \sum_{j=1}^{L} g_k g_j \frac{\lambda_k^{-1} \lambda_j^{-1}}{1 - \lambda_k^{-1} \lambda_j^{-1}} \right)^2.$$  \hspace{1cm} (57)

which is independent of time.

Following a similar procedure, it can be proved that \(E[q(n)q(n-1)]\) is given by

$$E[q(n)q(n-1)] = E[e(n)^2] \left( g^T \cdot \bar{p} - \sum_{k=1}^{L} \sum_{j=1}^{L} g_k g_j \frac{\lambda_k^{-1} \lambda_j^{-1}}{1 - \lambda_k^{-1} \lambda_j^{-1}} \right).$$  \hspace{1cm} (58)

With this, expressions in (47) and (48) can be re-written as

$$E[q(n)^2] = E[e(n)^2] \left( 1 - \sum_{k=1}^{L} \sum_{j=1}^{L} g_k g_j \frac{\lambda_k^{-1} \lambda_j^{-1}}{1 - \lambda_k^{-1} \lambda_j^{-1}} \right).$$  \hspace{1cm} (59)

$$E[q(n)q(n-1)] = E[e(n)^2] \left( g^T \cdot \bar{p} - \sum_{k=1}^{L} \sum_{j=1}^{L} g_k g_j \frac{\lambda_k^{-1} \lambda_j^{-1}}{1 - \lambda_k^{-1} \lambda_j^{-1}} \right).$$  \hspace{1cm} (60)

Finally, from (16), (59) and (60), the following relation is obtained:

$$E[(\Delta q_n)^2] = 2E[e(n)^2] \times \left( 1 - g^T \cdot \bar{p} + \sum_{k=1}^{L} \sum_{j=1}^{L} g_k g_j \frac{\lambda_k^{-1} \lambda_j^{-1}}{1 - \lambda_k^{-1} \lambda_j^{-1}} \right).$$  \hspace{1cm} (61)

References


PUBLICACIÓN 3

**Título de la Publicación:** Systematic Design of High-Resolution High-Frequency Cascade Continuous-Time Sigma-Delta Modulators

**Autores:** Ramón Tortosa, Rafael Castro-López, José M. de la Rosa, Elisenda Roca, Angel Rodríguez-Vázquez and Francisco V. Fernández

**Tipo de publicación:** Revista internacional indexada con índice de calidad relativo

**Nombre de la revista:** ETRI Journal

**Editorial:** Electronics Telecommunications Research Institute

**ISSN:** 1225-6463

**Indice de impacto:** 1.129

**Referencia completa de la publicación:**


**RESUMEN**

Este artículo presenta una metodología “top-down/bottom-up” para sistematizar el diseño e implementación de moduladores ΣΔ en cascada realizados mediante la técnica de circuito de tiempo continuo. Las características más destacadas de la metodología propuesta son las siguientes:

- a) Modelado de comportamiento flexibles, que pueden ser aplicados en distintas etapas del proceso de síntesis “top-down”.

- b) Síntesis directa en el dominio del tiempo continuo para minimizar la complejidad de la circuitería y la sensibilidad a los errores de tolerancia de sus principales elementos.

- c) Exploración arquitectural basada en la optimización y el conocimiento.

- d) Uso de frentes Pareto-óptimos para reducir las iteraciones de rediseño.

La aplicabilidad de esta metodología se ilustra y valida mediante el diseño de un modulador ΣΔ en cascada de tiempo continuo en una tecnología CMOS de 130nm, con una tensión de alimentación de 1.2V, con resolución efectiva de 12 bits y 20 MHz de ancho de banda.
This paper introduces a systematic top-down and bottom-up design methodology to assist the designer in the implementation of continuous-time (CT) cascade sigma-delta (ΣΔ) modulators. The salient features of this methodology are (a) flexible behavioral modeling for optimum accuracy-efficiency trade-offs at different stages of the top-down synthesis process, (b) direct synthesis in the continuous-time domain for minimum circuit complexity and sensitivity, (c) mixed knowledge-based and optimization-based architectural exploration and specification transmission for enhanced circuit performance, and (d) use of Pareto-optimal fronts of building blocks to reduce re-design iterations. The applicability of this methodology will be illustrated via the design of a 12-bit 20 MHz CT ΣΔ modulator in a 1.2 V 130 nm CMOS technology.

Keywords: ΣΔ modulators, mixed-signal interfaces for wireless/wireline communications, design automation.
In spite of their advantages, CT $\Sigma$Δ modulators are more sensitive than DT modulators to some circuit errors, namely, clock jitter, excess loop delay, and technology parameter variations [2]. The latter are especially critical for the realization of cascaded architectures. This explains the use of single-loop topologies in most reported silicon prototypes [4]-[6]. Although single-loop CT topologies have potentially lower sensitivity to technological process variations than cascade CT topologies, the possibility of avoiding stability problems in the latter make them especially appealing for high-resolution, high signal bandwidth operation.

Most developments in systematic design methods and tools have focused on DT $\Sigma$Δ modulators [7]-[13], probably due to their widespread use, but also due to their easier design. First, developments of methods and tools for CT $\Sigma$Δ modulators have addressed specific problems, such as efficient behavioral simulation [12], [14], [15] or topological synthesis by discrete-time to continuous-time transformation [16], eventually with coefficient scaling using simulation of ideal modulators [17].

This paper introduces a complete design methodology to assist the designer in the implementation of CT cascade $\Sigma$Δ modulators. The main components of this systematic methodology, introduced in section II, are the following:

a) Performance modeling of dominant error sources at the modulator level (described in section III)

b) A High-level topological synthesis method directly in the continuous-time domain (described in section IV)

c) Efficient behavioral simulator with variable levels of modeling accuracy for architectural synthesis, specification transmission, and hierarchical verification (described in section V)

d) Global and local optimization core for topology exploration and specification transmission (described in section II)

e) Specification transmission driven by bottom-up information flow in the form of Pareto-optimal fronts (described in section VI)

The design of a 12-bit 20 MHz CT $\Sigma$Δ modulator in a 1.2 V 130 nm CMOS technology is used in section VII as an illustrative example of each step.

II. Systematic Design Methodology

Synthesis of high-speed CT $\Sigma$Δ modulators is a complex task which requires systematic design methods and customized tools. The objective of the synthesis process is to design a CT $\Sigma$Δ modulator able to meet the performance specifications, with minimum power consumption and minimum occupation of silicon area.

The synthesis procedure is schematically shown in Fig. 2. In the three main stages of this design flow, design space exploration and specification transmission rely on the interaction of some kind of performance evaluator (such as equations and behavioral simulation with models at some level of abstraction) with an optimizer. The cornerstones of this process are an adequate formulation of a cost function, which quantifies the degree of compliance of the design with the targeted performance; a fast yet accurate method to evaluate the cost function; and an efficient technique to generate the next movement over the design space.

The optimization core used has two steps. In the first step, global optimization techniques are applied, whereas deterministic techniques are applied for local optimization in the second step [18]. Our experience is that adaptive simulated annealing algorithms are more efficient for global optimization addressing some specific design constraints, whereas other popular global optimization algorithms, such as evolutionary algorithms, are more powerful to explore trade-offs between performance specifications.

The optimization problem is mathematically stated as

$$\min_{\mathbf{x}} y_{ai}(\mathbf{x}), \quad 1 \leq i \leq P$$

subject to $y_{ij}(\mathbf{x}) \geq Y_{ij}$ or $y_{ij}(\mathbf{x}) \leq Y_{ij}$, $1 \leq j \leq R$,

where $y_{ai}(\mathbf{x})$ stands for the value of the $i$-th design objective.
(that is, to minimize power consumption); \( y_j(x) \) is the value of the \( j \)-th design constraint (that is, an SNR larger than 70 dB); \( Y_j \) is the targeted value of such design specification; and \( x \) is the vector of design variables. Design objectives, constraints, and variables depend on the optimization task at hand. For instance, block non-idealities (such as amplifier gain) are design variables for high-level sizing, but they are design constraints for circuit-level sizing. It is important to highlight the difference between a constraint and a design objective. Constraints define the set of valid designs (also called the feasible design space), whereas design objectives, such as power consumption or area occupation, characterize the optimality of the design and show the trade-off between valid solutions. The sizing engine carries out the optimization by using a single cost function. For those points of the design space that do not satisfy the design constraints, the cost function is defined as

\[
\Psi(x) = \max\left[-w_j \log\left(\frac{y_j}{Y_j}\right)\right],
\]

where \( w_j \) is the weight associated to the \( j \)-th constraint. For those points of the feasible design space, the cost function is defined as

\[
\Psi(x) = \Phi(y_i) = -\sum w_i \log\left|y_i\right|,
\]

where \( w_i \) is the weight associated with the \( i \)-th design objective.

The inputs to the architectural synthesis stage (see Fig. 2) are required performance specifications of the CT \( \Sigma \Delta \) modulator and the technology process information. The methodology starts by an architectural exploration, which basically tries to obtain candidate architectures, defined by the order of the modulator \( L \), the number of bits of the quantizer(s) \( B \), and the oversampling ratio \( M \), which allows a certain SNR specification to be obtained. This architectural exploration is performed by using analytical expressions that model the dominant error sources limiting the achievable SNR, in combination with the optimization core previously outlined. The modeling of these error sources will be discussed in section III. The output of this architectural exploration is a set of candidate architectures that can potentially meet the modulator performance specifications.

The following step is the topological synthesis, that is, the definition of the cascade architecture, the intra- and inter-stage loop filter transfer functions, and the cancellation logic functions. A direct synthesis method in the CT domain is used here instead of the more conventional DT to CT transformation of an equivalent DT topology. The direct topological synthesis method is described in section IV.

The input to the high-level sizing stage is the structural description of the topology being synthesized. The subsequent automated sizing process uses the behavioral simulator (see the non-idealities considered in section V) together with global optimization procedures to find out the maximum values of non-idealities of the different building blocks that can be tolerated while still meeting the modulator performance specifications. At this level, power consumption estimates are much more detailed as relationships with each building block...
specifications can be established [7]. The modulator performance with the transmitted building block specifications is then verified under all operating conditions (process, temperature, and supply variations) by using the behavioral simulator (section V). If this verification shows that some performance specification degrades beyond certain limits, the high-level synthesis and/or the architectural synthesis are performed again under harder constraints.

The last step of the synthesis procedure is the sizing of the building blocks. The inputs to the circuit-level sizing stage are the performance requirements for each building block (for instance, DC gain and bandwidth of amplifiers, or hysteresis and offset for comparators). This sizing is performed by combining an electrical simulator with the global optimization procedure previously outlined [18]. The implementation of the optimization core is flexible enough to incorporate valuable design knowledge of each building block. At the optimization level, design knowledge brings knowledge of the feasibility space. This limits the exploration space and makes the synthesis process more efficient, thereby enhancing the optimization results.

With all blocks sized, a final verification of the complete modulator at the electrical level at a limited number of operating conditions is performed, namely, at the nominal point and a few critical process corners. This verification is complemented by a more exhaustive verification (all process, temperature, and supply variations) at the behavioral level with information extracted at the electrical level. Performance degradations beyond tolerable margins induce redesign iterations at the circuit and/or modulator levels.

III. High-Level Performance Modeling and Architectural Exploration

As shown in section II, design space exploration and specification transmission rely on the iterative interaction between a global optimizer and a fast performance evaluator. At a high level of abstraction, modulator performance is modeled by a set of closed-form equations, which are relatively inaccurate but carry essential information on the design parameters dominating the system behavior. The signal to noise ratio of a ΣΔ modulator is given by

\[ SNR = \frac{A^2/2}{P_e}, \]

where \( A \) represents the magnitude of the input signal, and \( P_e \) represents the in-band error power. Ideally, the in-band error power only contains the quantization noise \( P_{eq} \):

\[ P_{eq} = \frac{X_{FS}^2}{6f_s(2^N-1)^2} \int_0^1 \left| N_{TF}(f) \right|^2 df. \]

Here, \( X_{FS} \) is the full-scale of the quantizer, \( N \) is the number of bits of the quantizer, \( f_s \) is the sampling frequency, \( N_{TF}(.) \) is the noise transfer function, and \( B_s \) is the signal bandwidth. However, in practice, the error power contains terms due to quantization error power enlargement, digital-to-analog converter (DAC) non-linearities, capacitor mismatching, thermal noise, clock jitter, finite amplifier gain, incomplete amplifier settling, and so on. Therefore, the in-band error power becomes

\[ P_e = P_{eq} + \Delta P_{eq} + P_{e\text{thermal}} + P_{e\text{jitter}} + P_{e\text{DAC}} + P_{e\text{settling}} + \ldots \]

Unlike other types of ΣΔ modulators, a dominant error source in high-speed CT modulators is the error power due to clock jitter. For this reason, closed-form modeling of the influence of jitter is of paramount importance. The error power due to clock jitter in CT ΣΔ modulators with non-return-to-zero (NRZ) DACs can be expressed as in [19] as

\[ P_{e\text{jitter}} = B_w\left(\frac{A^2}{2f_s}\right)\left(\frac{X_{FS}^2}{6(2^N-1)}\right)^2\Psi\left(\frac{g}{p}, \frac{\bar{\lambda}}{L}, \frac{1}{f_s}\right), \]

where \( A \) and \( a \) are the amplitude and frequency of the input signal, and \( \Psi\left(\frac{g}{p}, \frac{\bar{\lambda}}{L}, \frac{1}{f_s}\right) \) is a function arising from the state-space representation of the noise transfer function of the modulator and depends on the modulator order. It can be seen that it has two terms. The first term depends on the modulator input and decreases with the sampling frequency, and the other depends on the modulator architecture and increases with sampling frequency.

For illustration’s sake, Fig. 3 represents the two terms in brackets in (4) for a 5-bit third-order modulator with a 20 MHz input frequency as a function of the sampling frequency. Notice that there is a frequency range dominated by the signal-dependent term and another range dominated by the modulator-dependent term. Therefore, there is an optimum sampling frequency which minimizes the in-band jitter noise power and, hence, maximizes the SNR.

The use of the dominant error power terms in (3) (shown in (2) and (4)) in combination with the optimization core allows candidate architectures to be extracted (each represented by a triad of values of order, number of bits, and oversampling ratio \{\( L, B, M \} \) with better performance in terms of distribution of the noise transfer function (NTF) zeroes and insensitivity to clock jitter.

Usually, several triads are considered for later stages for several reasons. First, the modeling equations are very approximate and, therefore, there is no guarantee that the selected architecture will continue to meet the performance specifications when more accurate models containing the
non-idealities of the particular physical implementation are used. The optimal architecture is the one that, meeting the performance constraints, minimizes objectives like power consumption or area occupation. Exploration criteria at the architectural level include considerations like order minimization, minimization of oversampling ratio to avoid infeasible sampling frequencies in terms of power consumption, and minimization of the number of bits in the quantizer to avoid the use of linearization techniques [4], [19]. Therefore, the power or area minimization criteria that can be considered at this level are of qualitative nature; therefore, any ranking of candidate architectures may suffer significant changes when progressing through the synthesis process. However, this is not very critical at this stage because the desired result is just a set of candidate topologies which will be pruned when more detailed models are considered in subsequent design steps.

IV. Topological Synthesis

Cascade CT ΣΔ modulator architectures are usually synthesized by first synthesizing a ΣΔ modulator with the same performance specifications in the DT domain and then applying a DT to CT transformation that keeps the same digital cancellation logic [16]. However, obtaining a functional CT modulator from this transformation and keeping the cancellation logic requires every state variable and DAC output to be connected to the integrator input of subsequent stages as Fig. 4 shows for a 2-1-1 architecture. This means a larger number of analog components (transconductors and amplifiers), which translates into larger area, higher power consumption, and higher sensitivity to circuit tolerances.

To avoid this, we have developed a synthesis method directly in the continuous-time domain which we will present in this section. Let us consider the general case of a cascaded CT ΣΔ modulator with $m$ stages as shown in Fig. 1. Let us denote the transfer function from $y_i(s)$ to the input of $j$-th quantizer as

$$F_{ij} = F_j(s) = \frac{q_j(s)}{y_i(s)}. \quad (5)$$

The synthesis method starts by optimally placing the poles of the single-loop transfer functions $F_j(s)$ at the positions which minimize the NTF in the signal bandwidth [21]. Their numerators are obtained by combining behavioral simulation with the optimization core. Starting from the nominal values required to place the zeros of the corresponding NTF, the modulator performance is optimized in terms of dynamic range and stability. For this purpose, these coefficients are varied in a range around their nominal values in order to maximize the SNR while maintaining stability. Then, transfer functions $F_j(s)$ are automatically determined by the inter-stage integrating paths.

If the modulator input, $x(t)$, is set to zero, it can be shown that the output of each stage $y_j(z)$ can be written as

$$y_j(z) = \frac{E_j(z) + \sum_{k=1}^{m-1} Z^{j-k} [H_{DAC} F_k]_{mT}}{1 - Z^{j} [H_{DAC} F_k]_{mT}}, \quad (6)$$

where $Z$ stands for the Z-transform, and $L^{mT}$ is the inverse Laplace transform.

The output $y_0$ of the modulator can be written as

$$y_0 = \sum_{k=1}^{m} y_k C_{L_k} = \sum_{k=1}^{m} \frac{E_k(z) + \sum_{j=1}^{m} Z^{j-k} [H_{DAC} F_k]_{mT}}{1 - Z^{j} [H_{DAC} F_k]_{mT}} C_{L_k}. \quad (7)$$
where $CL_d(z)$ represents the partial cancellation logic transfer function of the $k$-th stage.

The partial cancellation logic transfer functions can be calculated by imposing the cancellation of the transfer function of the first $m-1$ quantization errors $E_d(z)$ in (7). This gives

$$CL_k(z) = \frac{-Z\{L^{-1}(H_{DAC}F_{km})\}_{nT}}{1 - Z\{L^{-1}(H_{DAC}F_{mm})\}_{nT}}$$

where the partial cancellation logic transfer function of the last stage, $CL_m(z)$ can be chosen to be the simplest form that preserves the required noise shaping. By using this method, the 2-1-1 architecture in Fig. 5 is synthesized. The circuitry is significantly less complex than that shown in Fig. 4. Another positive consequence is better sensitivity to parameter tolerances.

![Diagram of a 2-1-1 CT \Sigma\Delta modulator using direct synthesis.](image)

Table 1. Basic building blocks and non-idealities modeled in the behavioral simulator.

<table>
<thead>
<tr>
<th>Block</th>
<th>Non-idealities</th>
</tr>
</thead>
<tbody>
<tr>
<td>Integrators</td>
<td>Finite and non-linear gain, dynamic limitations (parasitic capacitors, one- and two-pole transconductor model), thermal noise, finite output swing, linear input range, offset.</td>
</tr>
<tr>
<td>Resonators</td>
<td>Non-idealities associated to the integrators</td>
</tr>
<tr>
<td>Comparators</td>
<td>Offset, hysteresis, signal-dependent delay</td>
</tr>
<tr>
<td>Quantizers/DACs</td>
<td>Integral non-linearity, gain error, offset, jitter, excess loop delay</td>
</tr>
</tbody>
</table>

VI. High-Level Sizing Using POFs

As stated in section II, the combination of the behavioral simulator in section V with the optimization tool allows the high-level sizing of the \Sigma\Delta modulator to be efficiently performed, that is, getting the maximum non-idealities of the building blocks which can be tolerated while meeting the modulator specifications.

This high-level specification transmission has some drawbacks. First, there is no information a priori about the realizability of the building blocks with the transmitted specifications, and this may induce redesign iterations. Secondly, even if the specifications are realizable, the results
Fig. 6. (a) Gain/GB/power Pareto-optimal hypersurface for a cascode operational amplifier and (b) gain/GB projection.

Fig. 7. Front-end operational amplifier.

may be suboptimal in terms of area or power consumption due to an inappropriate balance among the specifications demanded for different building blocks.

Specification transmission can be made more efficient if Pareto-optimal fronts of candidate architectures are available. These fronts represent trade-off hypersurfaces between the different types of circuit performance [24]-[26]. For illustration’s sake, Fig. 6(a) shows the trade-offs between dc-gain, gain-bandwidth (GB) product, and power for the folded-cascode operational amplifier shown in Fig. 7 in a 130 nm CMOS technology. This Pareto-optimal front was generated by combining a genetic algorithm [27] with an electrical simulator. Projection on the XY plane in Fig. 6(b) makes it easy to visualize the best trade-off between dc gain and GB that the circuit at hand can achieve. Pareto fronts usually have higher dimensionality including all specifications of interest of the building block, which allows exploration of the trade-off among them, including the power and area budget.

Although Pareto fronts can also be used to directly provide the sizes of the building blocks (each point in the Pareto front represents a design point), in our case, we have used them only to guarantee the feasibility of specifications and to provide estimates of area and power for higher hierarchical levels. The reason is that Pareto fronts are usually generated by using evolutionary algorithms, where a population of individuals evolves towards the best performance trade-offs. Therefore, the number of points of the Pareto fronts is necessarily limited [26]. Restricting the search space to those points would lead to suboptimal solutions; therefore, better results are obtained if circuit sizing using the statistical optimization techniques discussed in section II is applied with the circuit specifications obtained in the high-level sizing.

VII. Case Study

The objective specifications for the CT ΣΔ modulator are 12 bits with 20 MHz signal bandwidth for a wireline communication application, to be implemented in a 130 nm CMOS technology. As a result of the different steps of the architectural exploration process, several fifth-order (L=5) cascade ΣΔ modulators were selected: 2-1-1-1, 2-2-1, and 3-2 topologies. Only the topology which is retained for the final synthesis steps is conceptually shown in Fig. 8 (a). It consists of a 2-2-1 topology and is clocked at \( f_c = 240 \) MHz (\( M=6 \)) with B=4 and NRZ DACs in all stages in order to minimize the effect of jitter.

The intra- and inter-stage transfer functions \( F_y \) can be written as:

\[
\begin{align*}
F_{11}(s) = & \frac{b_{11}s + b_0}{s^2 + \omega_{p1}^2}, \\
F_{22}(s) = & \frac{b_{31}s + b_{30}}{s^2 + \omega_{p2}^2}, \\
F_{33}(s) = & \frac{b_{30}}{s}, \\
F_{23}(s) = & \frac{b_{20}b_{30}}{s(s^2 + \omega_{p2}^2)}, \\
F_{13}(s) = & \frac{b_{10}b_{20}b_{30}}{s(s^2 + \omega_{p1}^2)(s^2 + \omega_{p2}^2)},
\end{align*}
\]

where \( \omega_{p1,2} \) denotes the optimal placement of the pole frequencies. Coefficients \( b_{ij} \) in (9) are found through a
maintaining stability. The nominal values in order to achieve the maximum SNR while the zeroes of the corresponding dynamic range, starting the simulation-based optimization process that optimizes the building blocks, and behavioral simulation for evaluation. The result of this sizing process is summarized in Table 3, showing the maximum (minimum) values of the non-idealities (at the building block level) that can be tolerated to fulfill the required modulator performance. Notice that not all non-idealities that were presented in Table 1 are listed in Table 3. In this table, only specifications for those non-idealities that have a significant impact on the modulator performance are collected. Thermal noise of amplifiers, for instance, is not critical for the design at hand (it is usually less critical than the integrator’s thermal noise from the $RC$ elements, whose in-band noise power, in this case, is around 85 dB). The building blocks, including a front-end opamp, loop filter transconductors, quantizers, and DACs are designed by applying a cell-level sizing tool [18]. Due to space limitations, only the synthesis results of the front-end opamp sizing are shown here.

The schematic of the front-end operational amplifier used together with its common-mode feedback circuit is shown in Fig. 7. It is a fully differential folded-cascode topology with gain

\[
C_L(z) = z^{-1}(n_{i4} + n_{i5}z^{-1} + n_{i6}z^{-2} + n_{i7}z^{-3} + n_{i8}z^{-4}),
\]

\[
C_{L2}(z) = z^{-1}(n_{i2} + n_{i3}z^{-1} + n_{i4}z^{-2} - (1 - 2\cos(T_i\omega_{po})z^{-1} + z^{-2}),
\]

\[
C_{L3}(z) = (1 - 2\cos(T_i\omega_{po})z^{-1} + z^{-2})(1 - 2\cos(T_i\omega_{po})z^{-1} + z^{-2}),
\]

\[
n_{i0} = n_{i4} = -\frac{h_i h_{i2} h_{i0}}{\alpha_{po}^2 \alpha_{po}^2 (\alpha_{po}^2 - \alpha_{po}^2)},
\]

\[
n_{i1} = n_{i1} = -\frac{2h_i h_{i2} h_{i0}}{\alpha_{po}^2 \alpha_{po}^2 (\alpha_{po}^2 - \alpha_{po}^2)}
\cdot \{T_i (\alpha_{po}^3 \alpha_{po}^3 - \alpha_{po}^3 \alpha_{po}^3 + \alpha_{po}^3 \alpha_{po}^2 \alpha_{po}^2 - \alpha_{po}^3 \alpha_{po}^3 + \alpha_{po}^3 \alpha_{po}^3 + \alpha_{po}^3 \alpha_{po}^2 \alpha_{po}^2 - \alpha_{po}^3 \alpha_{po}^3 + \alpha_{po}^3 \alpha_{po}^3),
\]

\[
n_{i2} = n_{i2} = -\frac{h_i h_{i2} h_{i0}}{\alpha_{po}^2} [T_i \alpha_{po}^2 \alpha_{po}^2 - \sin(T_i \omega_{po}^2)],
\]

\[
n_{i3} = n_{i3} = -\frac{h_i h_{i2} h_{i0}}{\alpha_{po}^2} [\sin(T_i \omega_{po}^2) - T_i \omega_{po}^2 \cos(T_i \omega_{po}^2)],
\]

where $T_i = 1/f_s$ is the sampling period.

Figure 8 (b) shows the conceptual circuit implementation of the modulator. The results of the optimization process are summarized in Table 2, which includes the values of loop filter coefficients, $k_i$ (implemented as transconductances) and the capacitances, $C_n$ used in the modulator.

The modulator was high-level sized. That is, the system-level specifications (12-bit at 20 MHz) were mapped onto building-block specifications using global optimization for design parameter selection, Pareto-optimal fronts of the sub-blocks and behavioral simulation for evaluation. The results of this sizing process is summarized in Table 3, showing the maximum (minimum) values of the non-idealities (at the building block level) that can be tolerated to fulfill the required modulator performance. Notice that not all non-idealities that were presented in Table 1 are listed in Table 3. In this table, only specifications for those non-idealities that have a significant impact on the modulator performance are collected. Thermal noise of amplifiers, for instance, is not critical for the design at hand (it is usually less critical than the integrator’s thermal noise from the $RC$ elements, whose in-band noise power, in this case, is around 85 dB). The building blocks, including a front-end opamp, loop filter transconductors, quantizers, and DACs are designed by applying a cell-level sizing tool [18]. Due to space limitations, only the synthesis results of the front-end opamp sizing are shown here.

The schematic of the front-end operational amplifier used together with its common-mode feedback circuit is shown in Fig. 7. It is a fully differential folded-cascode topology with gain

![Fig. 8. (a) Conceptual diagram of the 2-2-1 modulator and (b) circuit implementation.](image-url)
Table 2. Loop filter coefficients of the ΣΔ modulator.

<table>
<thead>
<tr>
<th>Coefficient</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>$R_i$</td>
<td>5 kΩ</td>
</tr>
<tr>
<td>$C_i$</td>
<td>6 pF</td>
</tr>
<tr>
<td>$k_1=k_2=k_3=k_4=200$ µA/V</td>
<td></td>
</tr>
<tr>
<td>$k_5=100$ µA/V</td>
<td></td>
</tr>
<tr>
<td>$k_6=158$ µA/V</td>
<td></td>
</tr>
</tbody>
</table>

Table 3. High-level sizing of the ΣΔ modulator.

<table>
<thead>
<tr>
<th>Section</th>
<th>Specification</th>
</tr>
</thead>
<tbody>
<tr>
<td>Front-end opamp</td>
<td>DC gain &gt; 68 dB, GB &gt; 580 MHz, Phase margin &gt; 60°, Differential output swing &gt; 0.5 V</td>
</tr>
<tr>
<td>Flash quantizers</td>
<td>Comparator offset &lt; 20 mV, Comparator hysteresis &lt; 20 mV, Comparator resolution time &lt; 1 ns, Ladder unit resistance = 220 Ω</td>
</tr>
<tr>
<td>Loop transconductors</td>
<td>DC gain &gt; 50 dB, Differential input amplitude &gt; 0.3 V, Differential output amplitude &gt; 0.3 V, Third-order non-linearity &lt; -56 dB</td>
</tr>
<tr>
<td>Current-steering DACs</td>
<td>Current standard deviation &lt; 0.15% LSB, Finite output impedance &gt; 12 MΩ, Settling time &lt; 500 ps</td>
</tr>
</tbody>
</table>

Table 4. Electrical performance of the front-end opamp.

<table>
<thead>
<tr>
<th>Specification</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>GB</td>
<td>600 MHz</td>
</tr>
<tr>
<td>DC gain</td>
<td>71 dB</td>
</tr>
<tr>
<td>Phase margin</td>
<td>80°</td>
</tr>
<tr>
<td>Parasitic input capacitance</td>
<td>0.36 pF</td>
</tr>
<tr>
<td>Parasitic output capacitance</td>
<td>0.4 pF</td>
</tr>
<tr>
<td>Differential output swing</td>
<td>0.7 V</td>
</tr>
<tr>
<td>Power consumption</td>
<td>20 mW</td>
</tr>
</tbody>
</table>

After a simulator-in-the-loop optimization process, the resulting sized circuit achieves the electrical performance shown in Table 4. A similar sizing is applied for the other building blocks.

The modulator performance before and after layout generation has been extensively verified. Figure 9 shows the layout of the modulator. The total occupied area is 2.33 mm$^2$ (pads included) with a power dissipation of 70 mW from a single 1.2 V supply voltage. As an illustration, Fig. 10 shows the output spectrum for an input sine-wave with -6.5 dBV amplitude and 1.76 MHz frequency. The maximum signal-to-(noise+distortion) ratio (SNDR) is 80 dB (about 13 bits). These results correspond to a full electrical-level post-layout simulation (thermal noise is included in the simulation). Due to the long simulation time, this type of verification is only feasible for a limited set of simulation conditions. A more exhaustive verification (including process, supply, and temperature variations) is performed by using the behavioral simulator with data obtained from the electrical simulation of the building blocks. This allows, for instance, the application of Monte Carlo simulation to evaluate the influence of mismatch on performance deviations. In the present case,
even in the worst-case mismatch, a maximum SNDR larger than 74 dB is obtained.

Finally, Fig. 11 shows the results from a two-tone input signal test. The performance degradation due to the third-order intermodulation distortion (IM3) is well below the required resolution.

VIII. Conclusion

This paper has presented a complete design methodology supporting the design of CT ΣΔ modulators. An appropriate combination of design knowledge, behavioral simulation, synthesis methods, and optimization tools eases the complex design of these high-performance modulators.

References

[27] K. Deb et al., “A Fast and Elitist Multiobjective Genetic Algorithm:
Dr. Castro is also currently teaching at the University of Seville, Spain, where his main research area was high speed continuous-time sigma delta modulators. In 2007, he joined Analog Devices in Ireland, where he is currently working as a team leader and main designer in the development of low-voltage and low-power temperature sensors. His research interests include low-power data converters and sensors.

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PUBLICACIÓN 4

Título de la Publicación: Design of a 1.2-V Cascade Continuous-Time ΣΔ Modulator for Broadband Telecommunications

Autores: Ramón Tortosa, José M. de la Rosa, Angel Rodríguez-Vázquez and Francisco V. Fernández

Tipo de publicación: Artículo en congreso internacional con proceso de revisión por pares

Nombre del congreso: IEEE International Symposium on Circuits and Systems (ISCAS)

Editorial: IEEE


Referencia completa de la publicación:


RESUMEN

Este artículo presenta el diseño de un modulador ΣΔ de tiempo continuo en cascada con cuantización multi-bit para sistemas de telecomunicación de banda ancha. La arquitectura del modulador ha sido sintetizada directamente en el dominio del tiempo continuo en lugar de utilizando una transformación discreta-continua a un modulador de tiempo discreto equivalente. Este método resulta en una arquitectura más eficiente en términos de conformado de ruido, consumo de potencia y sensibilidad a las tolerancias de los elementos de circuito analógicos.

El diseño del circuito, realizado en una tecnología CMOS de 130nm, se fundamenta en una metodología CAD “top-down/bottom-up” que combina simulación con optimización estadística en diferentes niveles de abstracción de la jerarquía del sistema. El consumo de potencia estimado es de 60mW, considerando una única tensión de alimentación de 1.2V y una frecuencia de muestreo de 240MHz. Los resultados de simulación demuestran que el modulador puede alcanzar una resolución efectiva de 80dB (13-bit) en un ancho de banda de 20MHz.
Design of a 1.2-V Cascade Continuous-Time $\Sigma \Delta$ Modulator for Broadband Telecommunications

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Abstract – This paper presents the design of a continuous-time multibit cascade 2-2-1 $\Sigma \Delta$ modulator for broadband telecom systems. The modulator architecture has been synthesized directly in the continuous-time domain instead of using a discrete-to-continuous time transformation. This method results in a more efficient modulator in terms of noise shaping, power consumption and sensitivity to circuit element tolerances. The design of the circuit, realized in a 0.13µm CMOS technology, is based upon a top-down CAD methodology which combines simulation and statistical optimization at different levels of the modulator hierarchy. The estimated power consumption is 60mW from a 1.2-V supply voltage when clocked at 240MHz. Simulation results show 80-dB effective resolution within a 20-MHz signal bandwidth.  

I. INTRODUCTION

Modern broadband telecommunication applications, like Very high-rate Digital Subscriber Line (VDSL) and Power Line Communication (PLC), demand Analog-to-Digital Converters (ADCs) targeting 12-14bit resolution at conversion rates of 40-80 MSamples/second (MS/s). Traditionally, these specifications have been achieved with Nyquist-rate ADCs, using pipeline or folding/interpolation topologies, because of the prohibitive sampling frequencies required by $\Sigma \Delta$ Modulators ($\Sigma \Delta$Ms) [1]. However, in the last few years, the use of Continuous-Time (CT) instead of Discrete-Time (DT) circuit techniques are making possible for $\Sigma \Delta$Ms to digitize (1-15 MHz) signals with 11-14 bit resolution [2]-[4].

In spite of achieving potentially faster operation with lower power consumption, CT $\Sigma \Delta$Ms are more sensitive than DT $\Sigma \Delta$Ms to some circuit errors, namely: clock jitter and technology parameter variations [5]. The latter are specially critical for the realization of cascode architectures what explains the very few Integrated Circuits (ICs) reported up to now [4].

Recent studies demonstrate that more efficient cascode CT $\Sigma \Delta$Ms can be synthesized by using a direct synthesis method [6]. This method allows to reduce the number of analog components and to efficiently place the zeros/poles of the noise transfer function, thus yielding to more robust architectures than using a DT-to-CT transformation [7].

This paper reports the design and electrical implementation of a cascode CT $\Sigma \Delta$M. The modulator architecture comprises three stages. The first two stages are a second-order topology whereas the last stage uses a first-order loop filter. All stages include 4-bit internal quantization and Non-Return-to-Zero (NRZ) Digital-to-Analog Converter DAC in order to attenuate the clock jitter [8]. The modulator has been synthesized directly in the continuous-time domain and no calibration is used to compensate for mismatch and element tolerances. Circuit design, realized in a 0.13µm CMOS technology and nominal 1.2-V supply voltage, has been optimized from system-level to building-block level in order to achieve the required specifications with minimum power dissipation. Simulation results demonstrate that the presented circuit can digitize 20-MHz signals with 13-bit resolution when clocking at 240MHz.

II. DESIGN CONSIDERATIONS

The modulator in this paper was designed to cope with an effective resolution over 12bit within a 20-MHz signal bandwidth. Ideally, these specifications can be achieved by different combinations of modulator order, $L$, number of bits of the internal quantizer(s), $B$, and oversampling ratio, $M$. However, in practice, there are some important limiting factors precluding from using some of $\{L, B, M\}$ triads. These limitations impose the following design constraints:

- High-order single-loop topologies may not be feasible for the mentioned specifications because of stability issues. For that reason, only cascade architectures made up of second-order and first-order stages were considered.
- High values of $B$ force to use linearization techniques [3] or digital calibration [2] in order to control the nonlinearity of the DAC used in the modulator feedback loop.
- Large values of $M$ lead to unfeasible sampling frequencies in terms of power consumption.
- Last but not least, clock jitter is an ultimate limiting error that has to be addressed from the very beginning of the design process. In fact, as demonstrated in [8], the in-band noise power caused by jitter error can be minimized by proper selection of $B$, the sampling frequency, $f_s$ and the modulator loop filter.

Taking into account the considerations mentioned above, an exhaustive exploration of different $\Sigma \Delta$M loop filters was done using SIMSIDES [10] in order to find out the optimum $\{L, B, M\}$ triad in terms of power consumption, distribution of the Noise Transfer Function (NTF) zeroes and insensitivity to clock jitter. As a result, the fifth-order ($L = 5$) cascode $\Sigma \Delta$M, conceptually shown in Fig.1, was selected. It consists of a 2-2-1 topology, clocked at $f_s = 240$MHz ($M = 6$), with $B = 4$ and NRZ DAC in all stages in order to minimize the...
effect of jitter, that according to [8], must be below 3ps rms.

The modulator in Fig. 1 can be synthesized from an equivalent DT \( \Sigma \Delta M \) However, in order to get a functional CT \( \Sigma \Delta M \) while keeping the Cancellation Logic (CL) of the original DT \( \Sigma \Delta M \), every state variable and DAC output must be connected to every integrator input of later stages [7]. The number of integrating paths, and hence of analog components, can be reduced if the whole cascaded \( \Sigma \Delta M \) is directly synthesized in the CT domain as proposed in [6]. In this paper we have selected the latter methodology, which does not only take into account the single-stage loop filter transfer functions (\( F_{i,j} \)), but also the inter-stage loop filter transfer functions (\( F_{j,j} \)). The latter, defined as the transfer function from \( y_j \) to the \( j \)-th quantizer (see Fig. 1), are continuous-time integrating paths appearing only when the modulator stages are connected to form the cascaded \( \Sigma \Delta M \) and must be included in the synthesis methodology to obtain a functional modulator with minimum number of inter-stage paths.

For the modulator in this paper, the following \( F_{ij} \) were synthesized:

\[
F_{11}(s) = \frac{b_{11}s + b_{10}}{(s^2 + \omega_{p1}^2)} \quad F_{22}(s) = \frac{b_{21}s + b_{20}}{(s^2 + \omega_{p2}^2)} \quad F_{33}(s) = \frac{b_{30}s}{s^2 + \omega_{p2}^2} \\
\]

\[
F_{13}(s) = \frac{b_{20}b_{30}}{(s^2 + \omega_{p1}^2)(s^2 + \omega_{p2}^2)} \quad F_{23}(s) = \frac{b_{20}b_{30}}{s^2 + \omega_{p2}^2} 
\]

where \( T_s = 1/f_s \) is the sampling period and \( \omega_{p1,2} \) are the pole frequencies. Coefficients \( b_{ij} \) in (1) are found through an iterative simulation-based process that – starting from nominal values required to place the zeroes of the corresponding NTF – optimizes the modulator performance in terms of dynamic range and stability. For this purpose, these coefficients are varied in a range of up to ±20% around their nominal values in order to achieve the maximum Signal-to-Noise Ratio (SNR) while keeping stability. The partial CL transfer functions can be calculated from (1) [6]:

\[
CL_1 = z^{-1}(n_{11} + n_{12}z^{-1} + n_{13}z^{-2} + n_{14}z^{-3}) \\
CL_2 = z^{-1}(n_{21} + n_{22}z^{-1} + n_{23}z^{-2}) \cdot (1 - 2\cos(T_{s}\omega_{p1})z^{-1} + z^{-2}) \\
CL_3 = (1 - 2\cos(T_{s}\omega_{p2})z^{-1} + z^{-2}) \cdot (1 - 2\cos(T_{s}\omega_{p2})z^{-1} + z^{-2})
\]

where coefficients \( n_{ij} \) are given by:

\[
n_{10} = n_{11} = -\frac{b_{10}b_{20}b_{30}}{\omega_{p1}\omega_{p2}2(\omega_{p1}^2 - \omega_{p2}^2)} \quad [T(s) = \omega_{p1}\omega_{p2}2(\omega_{p1}^2 - \omega_{p2}^2)] \\
n_{11} = -\frac{2b_{10}b_{20}b_{30}}{\omega_{p1}\omega_{p2}^22(\omega_{p1}^2 - \omega_{p2}^2)} \quad ([T(s) = \omega_{p1}\omega_{p2}^22(\omega_{p1}^2 - \omega_{p2}^2) + \omega_{p2}^2\sin(T_{s}\omega_{p2}) - \omega_{p1}^2\sin(T_{s}\omega_{p1}) + \omega_{p1}^2\sin(T_{s}\omega_{p1}) - \omega_{p2}^2\sin(T_{s}\omega_{p2})]) \\
n_{12} = -\frac{b_{10}b_{20}b_{30}}{\omega_{p1}\omega_{p2}2(\omega_{p1}^2 - \omega_{p2}^2)} \quad [T(s) = \omega_{p1}\omega_{p2}^22(\omega_{p1}^2 - \omega_{p2}^2) + \omega_{p2}^2\sin(T_{s}\omega_{p2}) + \omega_{p1}^2\sin(T_{s}\omega_{p1}) + \omega_{p2}^2\sin(T_{s}\omega_{p2})] \\
n_{20} = b_{20} = \frac{-b_{20}b_{30}}{\omega_{p2}^2} \quad [T(s) = \omega_{p2}^2(\omega_{p1}^2 - \omega_{p2}^2) + \omega_{p2}^2\sin(T_{s}\omega_{p2})] \\
n_{21} = -\frac{b_{20}b_{30}}{\omega_{p2}^2} \quad [T(s) = \omega_{p2}^2(\omega_{p1}^2 - \omega_{p2}^2) + \omega_{p2}^2\sin(T_{s}\omega_{p2}) - \omega_{p2}^2\cos(T_{s}\omega_{p2})]
\]

III. MODULATOR IMPLEMENTATION

Fig. 2 shows the conceptual circuit implementation of the modulator. An RC-active front-end integrator is chosen for its better linearity whereas the rest of integrators are Gm-C [2][3]. The 4-bit quantizers were implemented using a flash ADC made up of a resistive ladder and 15 regenerative comparators. DACs were implemented by current-steering topologies. An extra feedback branch between the output and the input to the quantizer (DAC2 in Fig.2) and two D-latches is

![Figure 1. Conceptual diagram of the 2-2-1 modulator.](image1)

- **Figure 1.** Conceptual diagram of the 2-2-1 modulator.

![Figure 2. Modulator implementation.](image2)

- **Figure 2.** Modulator implementation.

t2. Although the modulator has been implemented using fully-differential circuitry, a single-ended schematic is shown here for the sake of simplicity.
employed in the first two stages in order to compensate for the effect of excess loop delay [2]. The first two stages are formed by a resonator which has its poles placed at an optimum position, minimizing NTF in the signal bandwidth, \( B_n \) [9]. Resistor variations can be tuned out using a combination of a discrete rough tuning of the resistors \((R_{1a} \text{ and } R_{1b})\) and a continuous fine tuning of the transconductors \(k_{g1}\) and \(k_{g2}\). This tuning can be also used to cancel the effect of finite Gain-Bandwidth product \((GB)\) of the front-end opamp, due to the fact that all this error can be modelled as an integrator gain error [3]. All the other transconductors can be tuned in order to keep the time constant \(C/g_m\) unchanged over \(C\) variations.

Table I. sums up the outcome of the optimization process – entirely done in the CT domain as described in previous section. This table includes the values of loop filter coefficients, \(k_i\) (implemented as transconductances) as well as the capacitances, \(C_i\), and resistances, \(R_i\), used in the modulator.

The modulator was high-level sized, i.e., the system-level specifications (12-bit@20-MHz) were mapped onto building-block specifications using statistical optimization for design parameter selection and behavioral simulation for evaluation [10]. The result of this sizing process is summarized in Table II, showing the maximum (minimum) values of the circuit error mechanisms that can be tolerated in order to fulfill the required modulator performance. The data in this table are the starting point of the electrical design described in next section.

IV. DESIGN OF THE MAIN BUILDING BLOCKS

The modulator has been designed in a 0.13\(\mu\)m 1-poly 8-metal logic CMOS process. Metal-insulator-Metal capacitors were used because of their good matching and linearity properties. The estimated power dissipation is 60mW from a single 1.2-V supply voltage. The \(\Sigma A\) building blocks were conveniently selected and sized according to the system-level specifications. Among the others, the most critical subcircuits are the opamps and the transconductors, described below.

A. Front-end operational amplifier

Fig.3 shows the schematic of the front-end operational amplifier together with its common-mode feedback circuit. It is a fully differential telescopic cascode topology with gain boosting. Note that p-type input scheme has been considered in order to cancel the body effect in PMOS devices – one of the mechanisms for substrate noise coupling. One of the major limitations of this topology is the output swing. However, this is not a problem in this modulator where proper system-level design reduces the front-end integrator output signal range to 0.3V. Table III sums up the simulated performance of the circuit.

B. Transconductors

One of the main limitations in open-loop Gm-C integrators is their poor linearity. In order to tackle this problem, the transconductor shown in Fig.4, based on a quadratic term cancellation, is proposed. High-speed operation is achieved by using only feed-forward paths and by adding capacitors \(C_{gf}\) which introduces a high frequency zero that extends the frequency range of operation. This transconductor can be turned through the bias current, \(I_{b1c}.\) In order for the tuning to be effective, each transconductor in the modulator is formed by a parallel connection of unitary transconductors of 100\(\mu\)A/V each. Multiple MonteCarlo simulations have been done during the design process in order to take into account the impact of mismatch on the linearity of this circuit. Table IV shows a summary of the electrical performance.

| TABLE I. LOOP FILTER COEFFICIENTS OF THE \(\Sigma A\) |
| --- | --- |
| \(R_{1a} - R_{1b} = 1 \text{k}\Omega\) ; \(R_{1c} = 5 \text{k}\Omega\), | |
| \(C_1 = C_3 = 6 \text{ pF}\) | |
| \(k_{g1} = 500 \text{ \mu A/V}\) | \(k_{g2} = 800 \text{ \mu A/V}\) |
| \(k_{g3} = k_{g3} = k_{g4} = k_{g5} = k_{g6} = 200 \text{ \mu A/V}\) | |
| \(k_{g7} = 158 \text{ \mu A/V}\) | |

| TABLE II. HIGH-LEVEL SIZING OF THE \(\Sigma A\) |
| --- | --- |
| **Front-end opamp** | **GB** 600 MHz |
| DC Gain | \(>580\) MHz |
| Phase Margin | \(>60^\circ\) |
| Parasitic Input Capacitance | \(<0.4 \text{ pF}\) |
| Parasitic Output Capacitance | \(<0.5 \text{ pF}\) |
| Diff. Output Swing | \(>0.5 \text{ V}\) |
| **Transconductors** | **DC Gain** 71 dB |
| Diff. Input Amplitude | 0.3 V |
| Diff. Output Amplitude | 0.3 V |
| Third-order non-linearity | \(<36 \text{ dBV}\) |

| TABLE III. ELECTRICAL PERFORMANCE OF THE FRONT-END OPAMP |
| --- | --- |
| **GB** | **600 MHz** |
| DC Gain | 71 dB |
| Phase Margin | 80\(^\circ\) |
| Parasitic input capacitance | 0.36 \text{ pF} |
| Parasitic output capacitance | 0.4 \text{ pF} |
| Differential output swing | 0.7 V |
| Power consumption | 20mW |
V. SIMULATION RESULTS

The modulator was simulated considering the electrical performance described above. As an illustration, Fig.5 shows the output spectrum for an input sinewave of -6.5-dBV amplitude and 1.76-MHz frequency. The maximum Signal-to-(Noise+Distortion) Ratio (SNDR) is 80 dB (≈ 13 bits).

In addition to the design issues discussed in previous sections, the effect of circuit tolerances and component mismatch, especially critical in cascade CT-ΣΔMs, has been taken into account. The first one can be controlled in this circuit by using tuning of time constants. However mismatch error still remains. In order to evaluate the impact of this error on the performance of the modulator, maximum values of mismatch were estimated for a 0.13μm CMOS technology. The results of this analysis are shown in Fig.6 where the SNR is represented as a function of the standard deviation of the transconductances (σgm) and capacitances (σC). For each point of these surfaces, a Monte Carlo analysis of 150 simulations was carried out. The value of the SNR represented in the vertical axis of Fig.6 is obtained by 90% of the simulations for each case of σgm and σC. Note that even in the worst-case mismatch, the resolution is above the specified (74-dB).

CONCLUSIONS

The design of a 1.2-V, 0.13μm CMOS 13-bit@20-MHz cascade CT-ΣΔM has been presented. The modulator architecture has been directly synthesized in the continuous-time domain, thus optimizing their performance in terms of circuit complexity, power consumption and sensitivity with respect to mismatch. In the time of writing this paper, the circuit is being laid out for fabrication and it is expected that measured results will be available at the symposium.

REFERENCES

PUBLICACIÓN 5

Título de la Publicación: A 12-bit@40MS/s Gm-C Cascade 3-2 Continuous-Time Sigma-Delta Modulator

Autores: Ramón Tortosa, Antonio Aceituno, José M. de la Rosa, Angel Rodríguez-Vázquez and Francisco V. Fernández

Tipo de publicación: Artículo en congreso internacional con proceso de revisión por pares

Nombre del congreso: IEEE International Symposium on Circuits and Systems (ISCAS)

Editorial: IEEE


Referencia completa de la publicación:


RESUMEN

Este artículo presenta el diseño a nivel de transistor en una tecnología CMOS de 130nm de un modulador ΣΔ de tiempo continuo en cascada. La topología del modulador se ha sintetizado directamente en el dominio del tiempo continuo, y consiste en una etapa de tercer orden conectada en cascada con una etapa de segundo orden. Ambas etapas se han implementado mediante integradores Gm-C y utilizan un cuantizador de 4 bits. El efecto de la no linealidad del DAC se compensa mediante la implementación de un algoritmo DEM (de “Dynamic Element Matching”).

El consumo estimado de potencia del circuito es de 70mW considerando una única fuente de alimentación de 1.2V y una señal de reloj de 240MHz. Se presentan simulaciones eléctricas realizadas en Cadence-SPECTRE que validan el funcionamiento del modulador a nivel de transistor, mostrando una resolución efectiva de 12 bits en un ancho de banda de 20MHz.
A 12-bit@40MS/s Gm-C Cascade 3-2 Continuous-Time Sigma-Delta Modulator

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Abstract – This paper reports the transistor-level design of a 130-nm CMOS continuous-time cascade ΣΔ modulator. The modulator topology, directly synthesized in the continuous-time domain, consists of a third-order stage followed by a second-order stage, both realized using Gm-C integrators and a 4-bit internal quantizer. Dynamic element matching is included to compensate for the non-linearity of the feedback digital-to-analog converters. The estimated power consumption is 70 mW from a 1.2-V supply voltage when it is clocked at 240MHz. CADENCE-SPECTRE simulations show 12-bit effective resolution within a 20-MHz signal bandwidth.11

I. INTRODUCTION

The in-coming generation of mobile terminals will incorporate WLAN-based connection to the Internet. These systems will require broadband Analog-to-Digital Converters (ADCs) capable of digitizing 20-MHz wideband signals with effective resolutions over 12-bit with the minimum power consumption [1]. Recently, a number of Continuous-Time (CT) Sigma-Delta Modulators (ΣΔMs) have been reported featuring 9-11 bit effective resolution within 15-20 MHz signal bandwidth [2]-[5], which make them very appropriate for broadband telecom systems.

Most of reported CT ΣΔMs Integrated Circuits (ICs) use single-loop topologies because of their potentially lower sensitivity to technology parameter variations – a critical error in CT ΣΔMs [6]. However, as demonstrated in [7], more efficient cascade CT ΣΔMs can be obtained by using a direct synthesis method.

Based on this method, this paper presents the design and electrical implementation of a cascade 3-2 CT ΣΔM, that includes 4-bit internal quantization and Non-Return-to-Zero (NRZ) Digital-to-Analog Converter (DAC) in all stages. Dynamic Element Matching (DEM) is used to reduce the effect of mismatch on the linearity of the circuit. The feedback loop filter is implemented using Gm-C integrators whereas current steering DACs are employed in the feedback loop. The design of these blocks, realized in a 130-nm CMOS technology and using a single 1.2-V supply voltage, is based upon a top-down CAD methodology that combines simulation and statistical optimization at different levels of the system hierarchy. CADENCE-SPECTRE transistor-level simulation results demonstrate that the presented circuit can digitize 20-MHz signals with 12-bit resolution when is clocked at 240MHz.

II. MODULATOR ARCHITECTURE

The modulator has been designed to fulfill the following requirements: 12-bit within a 20-MHz signal bandwidth. In order to cope with these specifications in an optimal way in terms of power consumption, distribution of the Noise Transfer Function (NTF) zeroes and insensitivity to clock jitter [8], an exhaustive exploration of different CT ΣΔM topologies was done using SIMSIDES [9]. As a result, a fifth-order cascade ΣΔM, shown in Fig.112, was selected. It consists of a 3-2 topology, clocked at $f_c = 240$MHz, with an internal 4-bit (flash) quantizer and NRZ (current-steering) DAC in all stages in order to minimize the effect of jitter, that according to [8], must be below 3ps rms. An extra feedback branch between the output and the input to the quantizer (DAC2 in Fig.1) and two D-latches are employed in both stages in order to compensate for the effect of excess loop delay [10].

The modulator has been synthesized in the CT domain as proposed in [7] and implemented using Gm-C integrators. The front-end transconductor uses a different topology than the rest of transconductors in the chain because of the very demanding linearity requirements at the input node.

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11. This work has been supported by the Spanish Ministry of Science and Education (with support from the European Regional Development Fund) under contract TEC2004-01752/MIC.

12. Although the modulator has been implemented using fully-differential circuitry, a single-ended schematic is shown here for the sake of simplicity.
The first stage of the modulator is formed by an integrator and a resonator and the second stage is formed by a resonator. Both resonators have their poles placed at an optimum position, minimizing NTF in the signal bandwidth, $B_w$ [11]. Transconductors can be tuned in order to keep the time constant $C/g_m$ unchanged over $C$ variations. Loop filter coefficients are found through an iterative simulation-based process that – starting from nominal values required to place the NTF zeroes – optimizes the modulator performance in terms of dynamic range and stability within the full-scale range. Table I sums up the outcome of the optimization process – entirely done in the CT domain. This table includes the values of coefficients, $k_j$ (implemented as transconductances) as well as the capacitances, $C_j$, used in the modulator.

The modulator specifications were mapped onto building-block specifications using statistical optimization for design parameter selection and behavioral simulation for evaluation [9]. The result of this sizing process is summarized in Table II, showing the maximum (minimum) values of the circuit error mechanisms that can be tolerated in order to fulfill the required modulator performance. The data in Table II are the starting point of the electrical design described in next section.

III. CIRCUIT DESIGN

The ΣΔM building blocks, namely, transconductors, current-steering DACs and comparators (used in 4-bit flash quantizers) have been conveniently selected and sized according to the requirements given in Section II[3]. Design considerations on each of these blocks as well as their transistor-level performance are detailed in this section.

A. Transconductors

One of the main limitations in open-loop Gm-C integrators is their poor linearity. This is specially critical at the input node of the modulator because harmonic distortion caused by the front-end transconductor is directly translated to the digital domain without any attenuation. For this reason, two different transconductors were used in the modulator: one at the front-end and another one for the rest of the loop filter. Fig.2 shows the front-end transconductor, which is based on resistive source degenerated transconductances. Amplifiers are used to improve the linearity of the transconductor. As a triple-well option is available, NMOS transistors are used at the input because body modulation effect can be avoided by connecting the source terminal to the substrate terminal. This circuit was designed considering technology corners and mismatch deviations. Table III shows a summary of the electrical performance.

---

**TABLE I. LOOP FILTER COEFFICIENTS OF THE ΣΔM**

<p>| | |</p>
<table>
<thead>
<tr>
<th></th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td>$C_u = 3.65 \text{ pF}$</td>
<td>$k_u = 190 \mu\text{A/V}$</td>
</tr>
<tr>
<td>$C_1 = C_2 = C_3 = C_u$</td>
<td>$C_4 = C_5 = 2C_u$</td>
</tr>
<tr>
<td>$k_{in1} = 852 \mu\text{A/V}$</td>
<td>$k_{f01} = 730 \mu\text{A/V}$</td>
</tr>
<tr>
<td>$k_{f0} = 2k_u$</td>
<td>$k_{f1} = 4k_u$</td>
</tr>
<tr>
<td>$k_{g1} = k_{g5} = 3k_u$</td>
<td>$k_{g2} = 5k_u$</td>
</tr>
<tr>
<td>$k_{g4} = 7k_u$</td>
<td></td>
</tr>
<tr>
<td>$k_{in2} = 5k_u$</td>
<td>$k_{f02} = 6k_u$</td>
</tr>
<tr>
<td>$k_{r1} = k_{r2} = k_u$</td>
<td></td>
</tr>
</tbody>
</table>

---

**TABLE II. BUILDING-BLOCK SPECIFICATIONS**

<p>| | |</p>
<table>
<thead>
<tr>
<th></th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Modulator specs: 12-bit @ 20MHz</strong></td>
<td></td>
</tr>
<tr>
<td>Full-scale Reference Voltage</td>
<td>0.5V</td>
</tr>
</tbody>
</table>

**Front-End Transconductor**

<p>| | |</p>
<table>
<thead>
<tr>
<th></th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td>DC Gain</td>
<td>70 dB</td>
</tr>
<tr>
<td>Diff. Input Amplitude</td>
<td>0.3V</td>
</tr>
<tr>
<td>Diff. Output Amplitude</td>
<td>0.3V</td>
</tr>
<tr>
<td>Third-order non-linearity</td>
<td>−86dB</td>
</tr>
</tbody>
</table>

**Loop Filter Transconductors**

<p>| | |</p>
<table>
<thead>
<tr>
<th></th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td>DC Gain</td>
<td>50dB</td>
</tr>
<tr>
<td>Diff. Input Amplitude</td>
<td>0.3V</td>
</tr>
<tr>
<td>Diff. Output Amplitude</td>
<td>0.3V</td>
</tr>
<tr>
<td>Third-order non-linearity</td>
<td>−56dB</td>
</tr>
</tbody>
</table>

**Flash Quantizers**

<p>| | |</p>
<table>
<thead>
<tr>
<th></th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td>Comparator Offset</td>
<td>20mV</td>
</tr>
<tr>
<td>Comparator Hysteresis</td>
<td>20mV</td>
</tr>
<tr>
<td>Comp. Resolution Time</td>
<td>1ns</td>
</tr>
<tr>
<td>Ladder Unit Resistance</td>
<td>220Ω</td>
</tr>
</tbody>
</table>

**Current-steering DACs**

<p>| | |</p>
<table>
<thead>
<tr>
<th></th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td>Current std. deviation</td>
<td>0.15% LSB</td>
</tr>
<tr>
<td>Finite output impedance</td>
<td>12MΩ</td>
</tr>
<tr>
<td>Settling Time</td>
<td>500ps</td>
</tr>
</tbody>
</table>

---

**TABLE III. TRANSISTOR-LEVEL PERFORMANCE OF THE FRONT-END TRANSCONDUCTOR**

<p>| | |</p>
<table>
<thead>
<tr>
<th></th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td>DC Gain</td>
<td>78.3 dB</td>
</tr>
<tr>
<td>Max. Diff. Input Amplitude</td>
<td>0.3V</td>
</tr>
<tr>
<td>Max. Diff. Output Amplitude</td>
<td>0.3V</td>
</tr>
<tr>
<td>HD3</td>
<td>−89dB</td>
</tr>
<tr>
<td>Power consumption</td>
<td>8.8mW</td>
</tr>
</tbody>
</table>

---

**Figure 2. Front-end transconductor schematic.**
Fig. 3 shows the transconductor used for the rest of integrators in the modulator, which is based on a quadratic term cancellation. High-speed operation is achieved by using only feed-forward paths which introduce a high frequency zero that extends the frequency range of operation. This transconductor can be tuned through the bias current, $I_{\text{bias}}$. In order for the tuning to be effective, each transconductance is formed by a parallel connection of unitary transconductors of $100\mu$A/V each. Multiple Monte Carlo simulations have been done during the design process in order to take into account the impact of mismatch on the linearity of this circuit. Table IV shows a summary of the electrical performance of the transconductors showing their main features.

**B. Flash quantizers**

Embedded quantizers are realized by 4-bit flash ADCs made up of a resistor string for the division of the reference voltage combined with 15 comparators. Non-salicided polysilicon 220-$\Omega$ unit resistors were selected according to mismatch and non-linearity requirements.

As far as the comparators is concerned, the circuit shown in Fig. 4, based on a regenerative latch including a preamplifying stage, was selected. The role played by the preamplifier is to improve the resolution of the comparator, which can be severely degraded in practice due to dissimilarities between the latch parameters. For that reason, a large number of Monte-Carlo simulations have been done for characterizing the comparator performance after its full sizing. Table V summarizes the comparator features, showing the worst-cases for hysteresis and resolution time, together with the power dissipation.

![Figure 3. Loop-filter transconductor schematic.](image)

**TABLE IV. TRANSISTOR-LEVEL PERFORMANCE OF LOOP-FILTER TRANSCONDUCTORS**

<table>
<thead>
<tr>
<th>Parameter</th>
<th>DC Gain</th>
<th>Max. Diff. Input Amplitude</th>
<th>Max. Diff. Output Amplitude</th>
<th>HD3</th>
<th>Power consumption</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>52dB</td>
<td>0.3V</td>
<td>0.3V</td>
<td>–60dB</td>
<td>622μW</td>
</tr>
</tbody>
</table>

![Figure 4. Comparator schematic.](image)

**TABLE V. ELECTRICAL PERFORMANCE OF THE COMPARATORS**

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Typical</th>
<th>Worst-case</th>
</tr>
</thead>
<tbody>
<tr>
<td>Offset (mV)</td>
<td>0.7</td>
<td>-3.2</td>
</tr>
<tr>
<td>Hysteresis (mV)</td>
<td>12.1</td>
<td>12.7</td>
</tr>
<tr>
<td>Resol. time, $T_{RHL}$ (ns)</td>
<td>0.8</td>
<td>0.9</td>
</tr>
<tr>
<td>Resol. time, $T_{RHI}$ (ns)</td>
<td>0.75</td>
<td>0.8</td>
</tr>
<tr>
<td>Power Cons. (mW)</td>
<td>0.12</td>
<td></td>
</tr>
</tbody>
</table>

**C. Current-steering DACs**

Feedback DACs are implemented as current steering DACs because of their potential for high-speed operation and the convenience to interface with Gm-C loop filter [10]. Fig.5(a) shows the block diagram of the circuit. It consists of two 360-$\mu$A P-type (Fig.5(b)) gain-boosted current sources and 15 N-type (Fig.5(c)) regulated-cascode current cells which are controlled, through NMOS switches, by a thermometer-code input data ($D_i$ in Fig. 6(a)). The ideal operation of the current cells is affected by random errors (due to device mismatches), systematic errors (finite output impedance, thermal gradients, edge effects, CMOS technology-related errors) and dynamic limitations. Among the others, there is a strong trade-off.
between required mismatch (0.15% LSB) and settling time (500 ps). In order to relax this trade-off, DEM techniques are used to relax mismatch requirements down to 0.6% LSB, with LSB being \( I_{LSB} = 48 \mu A \), without penalizing the linearity of the modulator. The current cells were sized using FRIDGE [12] and verified by CADENCE-SPECTRE simulations. Table VI sums up the electrical performance\(^4\), which agrees with specifications given in Table II.

IV. LAYOUT AND TRANSISTOR-LEVEL SIMULATIONS

The modulator has been designed in a 130-nm 1-poly 8-metal logic CMOS process. Metal-insulator-Metal capacitors were used because of their good matching and linearity properties. Fig. 6 shows the layout of the chip highlighting the main parts. The layout has been carefully designed to maximize the modulator performance in terms of robustness with respect to switching activity, including separate analog, mixed and digital supplies, guard-rings surrounding each section of the circuit, etc. In addition, centroid layout techniques with unitary transistors have been employed, especially in most critical matched parts of the circuit. The complete modulator occupies an area of 2.33 mm\(^2\) (pads included) and the estimated power dissipation is 70 mW from a single 1.2-V supply voltage.

The modulator has been verified at the transistor-level using CADENCE-SPECTRE. As an illustration, Fig. 7 shows the output spectrum for an input sinewave of -10.5-dBV amplitude and 1.348-MHz frequency. The 3rd-order harmonic distortion limits the maximum signal-to-(noise+distortion) Ratio (SNDR) to 75.3 dB (12.2 bit) within a 20-MHz band.

<table>
<thead>
<tr>
<th>TABLE VI. WORST-CASE PERFORMANCE OF CURRENT CELLS</th>
</tr>
</thead>
<tbody>
<tr>
<td>Parameter</td>
</tr>
<tr>
<td>-----------</td>
</tr>
<tr>
<td>Output Impedance</td>
</tr>
<tr>
<td>Unitary current</td>
</tr>
<tr>
<td>Current Std Deviation</td>
</tr>
<tr>
<td>Settling Time</td>
</tr>
<tr>
<td>Power Cons. (mW)</td>
</tr>
</tbody>
</table>

CONCLUSIONS

A 1.2-V, 130-nm CMOS 12-bit@20-MHz cascade 3-2 CT-ΣΔM has been presented. The modulator architecture has been directly synthesized in the continuous-time domain and implemented using Gm-C integrators, 4-bit flash quantizers and NRZ current steering DACs in all stages. The chip has been sent for fabrication and measurements results will be available at the conference. If experimental results agree with CADENCE-SPECTRE simulations, the presented modulator will be at the cutting edge of state-of-the-art on ΣΔMs.

REFERENCES


\(^4\) Note that the P-type current cell is not switched and therefore, the circuit does not need to settle within a given period.
ANEXO 3: OTRAS PUBLICACIONES SOBRE LOS TRABAJOS RECOGIDOS EN LA TESIS DOCTORAL

RESUMEN

Este anexo incluye una serie de artículos publicados por el doctorando en conferencias internacionales, todas ellas vinculadas al trabajo de investigación desarrollado en esta tesis doctoral y publicadas por entidades de reconocido prestigio internacional como son IEEE, IEE (hoy IET) y SPIE, sometidas al proceso de revisión por pares.

Las publicaciones incluidas son las siguientes:


The 5th IEE International Conference on

ADDA 2005
Advanced A/D and D/A Conversion Techniques and their Applications

25 - 27 July 2005
Organised by The IEE Measurement, Sensors, Instrumentation and NDT Professional Network

University of Limerick, Limerick, Ireland
CONTENTS

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233 Cascade Continuous-Time Sigma-Delta Modulators with Reduced Number of Analog Components – Application to VDSL
R Tortosa, J M de la Rosa, A Rodriguez-Vázquez and F V Fernández
IMSE (CNM-CSIC)
Spain

239 High-Speed Continuous-Time Bandpass Delta-Sigma AD Modulator Architecture Employing Subsampling Technique with RF DAC
M Uemori and H Kobayashi
Gunma University
Japan

243 A CMOS Bandpass Sigma-Delta Modulator Employing SAW Resonator
R Yu and Y P Xu
National University of Singapore
Singapore

249 Fitting-Based Analysis and Debugging Tools for A/D Converters
T Rahkonen
University of Oulu
Finland

255 Measurements of ADCs Effective Resolution
J Holub, J Neškudla and J Vedral
Czech Technical University
Czech Republic

259 A Statistical Evaluation of ADC Histogram Tests with Arbitrary Stimuli Signal
N Björssel
University of Gävle
P Händel
Royal Institute of Technology
Sweden

Introduction to Poster Session 2

265 Efficient Technique for Improving the Frequency Response of CIC Decimation Filter
G J Dolecek
Institute INAOE
Mexico
CASCADE CONTINUOUS-TIME $\Sigma\Delta$ MODULATORS WITH REDUCED NUMBER OF ANALOG COMPONENTS – APPLICATION TO VDSL

R. Tortosa, J.M. de la Rosa, A. Rodríguez-Vázquez and F.V. Fernández

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Abstract

This paper describes new cascaded continuous-time $\Sigma\Delta$ modulators intended to cope with VDSL specifications. These modulators have been synthesized using a new methodology that is based on the direct synthesis of the whole cascaded architecture in the continuous-time domain instead of using a discrete-to-continuous time transformation as has been done in previous approaches. This method allows to efficiently place the zeroes/poles of the loop-filter transfer function and to reduce the number of analog components, thus leading to more efficient topologies in terms of circuitry complexity, power consumption and robustness with respect to circuit parasitics.

1. Introduction

Although most reported Sigma-Delta Modulators ($\Sigma\Delta$Ms) have been implemented using Discrete-Time (DT) circuits, the increasing demand for broadband data communication systems has motivated the use of Continuous-Time (CT) circuit techniques. In addition to show an intrinsic antialiasing filtering, CT $\Sigma\Delta$Ms provide potentially faster operation with lower power consumption than their DT counterparts [1][2]. However, CT $\Sigma\Delta$Ms are more sensitive than DT $\Sigma\Delta$Ms to certain circuit errors, namely: clock jitter, excess loop delay and technology parameter variations [1][2]. The latter are specially critical for the realization of cascade architectures. This has forced the use of single-loop topologies in most reported silicon prototypes even thought low oversampling ratios ($<12$) are needed [3][4], whereas very few cascaded CT $\Sigma\Delta$M Integrated Circuits (ICs) have been reported [5].

The need to achieve medium-high resolutions ($>12$bits) within high signal bandwidths ($\geq$20MHz) while guaranteeing stability, has prompted the interest in proper methods for the synthesis of high-order cascade CT $\Sigma\Delta$Ms [6]-[8]. These methods are based on applying a DT-to-CT transformation to an equivalent DT topology that fulfills the required specifications. In most cases, the use of such a transformation is normally translated into an increase of the analog circuit complexity with the subsequent penalty in silicon area, power consumption and sensitivity to parameter tolerances.

This paper presents a direct synthesis method of cascaded CT $\Sigma\Delta$Ms which, dispensing with the DT-to-CT equivalence, makes it possible to reduce the analog circuitry complexity and place the zeroes/poles of the quantization noise transfer function in an optimal way, thus yielding to more robust architectures than using a DT-to-CT transformation. As an application, the proposed methodology is used to find optimum CT $\Sigma\Delta$Ms for Very high-rate Digital Subscriber Line (VDSL). Three fifth-order cascade topologies are synthesized: 2-1-1-1, 2-2 and 3-2. These $\Sigma\Delta$Ms are designed for 12-bit@20-MHz specifications and their performances are compared in terms of time-domain simulations that take into account critical error mechanisms like mismatch and clock jitter error.

2. Direct synthesis of cascade CT $\Sigma\Delta$Ms

Fig.1 shows the conceptual block diagram of a $m$-stage cascaded CT $\Sigma\Delta$M. Each stage, consisting of a single-quantizer CT $\Sigma\Delta$M, re-modulates a signal containing the quantization error generated in the previous stage. Once in the digital domain, the outputs, $y_i$, of the stages are properly processed and combined (by the cancellation logic) in order to cancel out the quantization errors of all the stages, but the last one in the cascade. This latter error appears at the overall modulator output shaped by a function of order equal to the summation of the orders of all the stages.

Cascade CT $\Sigma\Delta$Ms are normally synthesized from equivalent (well-known) DT systems and use the same digital cancellation logic [7]. This DT/CT equivalence can be guaranteed because the overall open loop transfer function of each stage in Fig.1 is in fact a DT system [1]. However, in order to get a

![Figure 1. Conceptual block diagram of a cascaded CT $\Sigma\Delta$.](image-url)
functional CT ΣΔM while keeping the cancellation logic of the original DT ΣΔM, every state variable and DAC output must be connected to the integrator input of later stages [7]. This increases the number of analog components, i.e. transconductors, amplifiers and DACs. As an illustration, Fig.2(a) shows a cascaded 2-1-1 CT ΣΔM obtained from an existing DT ΣΔM [9]. Note that at least eight scaling coefficients (\( k_{2-9} \)) and their corresponding signal paths are needed to connect the different stages of the modulator. The number of integrating paths can be reduced – as illustrated in Fig.2(b) – if the whole cascaded ΣΔM is directly synthesized in the CT domain.

For that purpose, let us consider the more general case of the \( m \)-stage cascaded CT ΣΔM shown in Fig.1. The overall output, \( y_o \), is given by:

\[
y_o(z) = \sum_{k=1}^{m} y_k(z)CL_k(z)
\]

(1)

where \( y_k(z) \) and \( CL_k(z) \) represent respectively the output and partial cancellation logic transfer function of the \( k \)-th stage.

If the modulator input, \( x(t) \), is set to zero, the output of each stage can be written as:

\[
y_k(z) = \frac{E_k(z)}{1-Z_{kk}} + \sum_{i=1}^{k-1} \frac{Z_{ik}y_i(z)}{1-Z_{kk}}
\]

(5)

The partial cancellation logic transfer functions (\( CL_k \)) can be calculated by imposing the cancellation of the transfer function of the first \( m-1 \) quantization errors \( E_k(z) \) in (6). This gives:

\[
CL_k(z) = \frac{-Z_{km}CL_m}{1-Z_{mm}} = \frac{-Z\left[L^{-1}\left[H_DF_{km}\right]_{nTs}\right]CL_m(z)}{1-Z\left[L^{-1}\left[H_DF_{mm}\right]_{nTs}\right]}
\]

(7)

where the partial cancellation logic transfer function of the last stage, \( CL_m(z) \), can be chosen to be the simplest form that preserves the required noise shaping.

Note that the design equations (1)-(7) do not only take into account the single-stage loop filter transfer functions (\( F_{ii} \)), but also the inter-stage loop filter transfer functions (\( F_{ij}, i \neq j \)). The latter are continuous-time integrating paths appearing only when the modulator stages are connected to form the cascaded ΣΔM and must be included in the synthesis methodology to obtain a functional modulator with minimum number of inter-stage paths.

Therefore, the following procedure can be used in a systematic methodology for the synthesis of cascaded CT ΣΔMs:

- First, the poles of single-stage transfer functions (\( F_{ii}(s) \)) are optimally placed in the signal bandwidth for given
specifications. This process is carried out entirely in the CT domain and no equivalence to an existing DT modulator needs to be imposed.

- Second, once the individual stages are designed and optimized, cancellation logics are calculated using (7).

For illustrative purposes, the 2-1-1 CT ΣΔM of Fig.2(b) was synthesized using (1)-(7) to achieve 16-bit resolution in a 750-kHz bandwidth, with a sampling frequency of 48MHz (oversampling ratio, M = 32) [9]. For simplicity, in order to facilitate the comparison of the performance of both modulators in Fig.2, the coefficients of the first stage \(k_{i1}, k_{g1}, k_{fb1}, k_{fb2}\) are taken to be equal in both systems and are obtained from a DT-to-CT transformation of the first stage of a DT ΣΔM in [9]. The rest of coefficients in Fig.2(b) are taken such that the time constant of the integrators is the inverse of the sampling frequency \(T_s = 1/f_s\):

\[
\begin{align*}
k_{i1} &= -k_{fb1} = 1/4; \\
k_{fb2} &= -3/8 \\
k_{g1} &= k_{i1} = -k_{fb3} = k_{i2} = -k_{fb4} = 1 \\
\end{align*}
\]

Hence, the single-loop and inter-stage transfer functions are given by:

\[
\begin{align*}
F_{11} &= \frac{-3T_s}{(sT_s)^2} + \frac{1}{4} \\
F_{22} &= F_{33} = \frac{-1}{sT_s} \\
F_{13} &= \frac{-3T_s}{(sT_s)^2} + \frac{1}{4} \\
F_{23} &= \frac{-1}{(sT_s)^2} \\
\end{align*}
\]

and the partial cancellation logic transfer functions can be calculated using (7)-(9). Considering a Non-Return-to-Zero (NRZ) DAC, the following cancellation logics are derived:

\[
\begin{align*}
CL_1 &= \frac{-1}{48}(7 + 29z^{-1} - 7z^{-2} - 5z^{-3}) \\
CL_2 &= z^{-1}(1 + z^{-1})(1 - z^{-1})^2 \\
CL_3 &= 2(1 - z^{-1})^3 \\
\end{align*}
\]

where \(CL_3\) is chosen to have three zeroes at DC, corresponding to the zeroes contributed by the first three integrators.

In order to compare the robustness of both modulators in Fig.2, the effect of mismatch on the Signal-to-Noise Ratio (SNR) was also simulated using SIMSIDES, a SIMULINK-based time-domain behavioural simulator for ΣΔMs [10]. For this purpose, maximum values of mismatch were estimated for a 0.13 μm CMOS technology and both modulators in Fig.2 were simulated considering a Gm-C implementation. The results are shown in Fig.3 where the SNR loss is represented as a function of the standard deviation of the transconductances \(\sigma_{gm}\) and capacitances \(\sigma_C\). For each point of these surfaces, 150 simulations were carried out using random variations with the standard deviation given in the diagrams. The value of SNR loss represented in Fig.3 stands for the difference between the ideal SNR, i.e. with no parameter variation, and the SNR with 90% of the 150 simulations above it. It is shown that the lower analog component count in Fig.2(b) is reflected in a lower variance of the modulator coefficients, leading to a better behaviour in terms of sensitivity to mismatch.

3. Application to VDSL

As an application of the synthesis methodology proposed in previous section, three 5th-order cascaded CT ΣΔMs, shown in Fig.4, were synthesized to cope with VDSL specifications: 12-bit resolution within a 20-MHz signal bandwidth. In order to fulfill these specifications without being limited by the clock jitter error, the sampling frequency, \(f_s\), and the number of bits of the internal quantizers (and DACs), \(B\), must be properly chosen. In the case of 5th-order modulators like those shown in Fig.4, the in-band jitter noise power is minimized for \(f_s = 240\text{MHz}\) and \(B = 4\) [11].

Another critical source of error in CT ΣΔMs is the excess loop delay. As shown in [12] this error can be compensated by adding an extra feedback branch between the output and the input to the quantizer (DAC2 in Fig.4) and two D-latches. By adding this extra branch with the appropriate gain, the loop impulse response is exactly the same as that of the original. This extra feedback term can be easily included in the calculation of the cancellation logic. In a practical implementation it could be advantageous to make DAC2 programmable [4].

Considering the factors above, the CT ΣΔMs in Fig.4 were synthesized using the methodology described in Section 3, taking into account the following considerations:

- The first stage of the 2-1-1-1 architecture (Fig.4(a)) is formed by a resonator which has its poles placed at
Simulation-based procedure that explicitely shown in Table 1 for simplicity integration described in previous section. Coefficients of the modulators in Fig. 4, obtained using the formula:

$$
\begin{align*}
\sum C_{ij} &= \text{Table 1 shows the transforms of } F_{ij}(s) \text{ and cancellation logics } C_{ij} \text{ of the modulators in Fig.4, obtained using the formulation described in previous section. Coefficients } r_{ij} - \text{not explicitly shown in Table 1 for simplicity} - \text{are function of the loop filter coefficients. These coefficients are obtained from a simulation-based procedure that} \text{starting from nominal values required to place the zeroes of the corresponding NTF} \text{optimize the modulator performance in terms of dynamic range and stability. For this purpose, loop filter coefficients are varied in a range of up to ±20% around their nominal values in order to achieve the maximum Signal-to-Noise Ratio (SNR) while keeping stability.}

The outcome of the optimization process – entirely done in the CT domain – is summarized in Table 2. This table includes the values of loop filter coefficients, $k_i$, (implemented as transconductances) as well as the capacitances, $C_i$, and resistances, $R_i$ obtained from the optimization process.

4. Simulation results

The modulators in Fig. 4 were simulated using SIMSIDES [10]. Fig. 5 shows the ideal output spectra of the modulators when clocked at $f_c = 240$ MHz. It can be observed the effect of the resonators poles distributed within the signal bandwidth.

In addition to the ideal performance described above, the effect of most critical limiting factors has been taken into account in the high-level design. Two critical limiting factors in cascaded ΣΔMs, and particularly in their CT implementation, are circuit tolerances and component mismatch. The first one can be controlled by using tuning of time constants [3][4] or digital calibration [5]. However mismatch error still remains. In order to evaluate the impact of this error on the performance of the modulators in Fig. 4, maximum values of mismatch were estimated for a 0.13 μm CMOS technology considering a Gm-C implementation. The results of this analysis are shown.
in Fig.6 where the SNR is represented as a function of the stan-
dard deviation of the transconductances ($\sigma_{gm}$) and capaci-
tances ($\sigma_c$). For each point of these surfaces, a MonteCarlo
analysis of 150 simulations was carried out. The value of the
SNR represented in the vertical axis of Fig.6 is obtained by
90% of the simulations for each case of $\sigma_{gm}$ and $\sigma_c$. Note
that even in the worst-case mismatch, the resolution is above the
specified (72-dB).

Finally, the modulators in Fig.4(b)-(c) were high-level sized,
i.e., the system-level specifications (12-bit@20-MHz) were
mapped onto building-block specification using statistical opti-
mitization for design parameter selection, and behavioural
simulation for evaluation. The results of this sizing process are
summarized in Table 3, showing the maximum (minimum)
values of the circuit error mechanisms that can be tolerated in
order to fulfill the required modulator performance. As an illu-
sration, Fig.7 shows the output spectra of the modulators
being designed using the proposed method.

<table>
<thead>
<tr>
<th>Modulator</th>
<th>Function Transforms</th>
<th>Cancellation logics</th>
</tr>
</thead>
<tbody>
<tr>
<td>2-1-1-1</td>
<td>$Z^{-1}(H_{2-1-1}) = \frac{n_1 z^2 + n_2 z + n_3}{(z-1)^2 + 2 \cos(T \omega_p) z + 1}$</td>
<td>$C_L = -z^{-1}(n_{14} + n_{13} z^{-1} + n_{12} z^{-2} + n_{11} z^{-3} + n_{09} z^{-4})$</td>
</tr>
<tr>
<td></td>
<td></td>
<td>$C_L = -z^{-1}(n_{14} + n_{13} z^{-1} + n_{12} z^{-2} + n_{11} z^{-3} + n_{09} z^{-4})$</td>
</tr>
<tr>
<td></td>
<td></td>
<td>$C_L = -z^{-1}(n_{12} + n_{21} z^{-1} + n_{22} z^{-2})$</td>
</tr>
<tr>
<td></td>
<td></td>
<td>$(1 - 2 \cos(T \omega_p) z^{-1} + z^{-2})$</td>
</tr>
<tr>
<td></td>
<td></td>
<td>$(1 - 2 \cos(T \omega_p) z^{-1} + z^{-2})$</td>
</tr>
<tr>
<td>2-2-1</td>
<td>$Z^{-1}(H_{2-2-1}) = \frac{n_1 z^2 + n_2 z + n_3}{(z-1)^2 + 2 \cos(T \omega_p) z + 1}$</td>
<td>$C_L = -z^{-1}(n_{14} + n_{13} z^{-1} + n_{12} z^{-2} + n_{11} z^{-3} + n_{09} z^{-4})$</td>
</tr>
<tr>
<td></td>
<td></td>
<td>$C_L = -z^{-1}(n_{12} + n_{21} z^{-1} + n_{22} z^{-2})$</td>
</tr>
<tr>
<td></td>
<td></td>
<td>$(1 - 2 \cos(T \omega_p) z^{-1} + z^{-2})$</td>
</tr>
<tr>
<td></td>
<td></td>
<td>$(1 - 2 \cos(T \omega_p) z^{-1} + z^{-2})$</td>
</tr>
<tr>
<td>3-2</td>
<td>$Z^{-1}(H_{3-2}) = \frac{n_1 z^2 + n_2 z + n_3}{(z-1)^2 + 2 \cos(T \omega_p) z + 1}$</td>
<td>$C_L = -z^{-1}(n_{14} + n_{13} z^{-1} + n_{12} z^{-2} + n_{11} z^{-3} + n_{09} z^{-4})$</td>
</tr>
<tr>
<td></td>
<td></td>
<td>$C_L = -z^{-1}(n_{12} + n_{21} z^{-1} + n_{22} z^{-2})$</td>
</tr>
<tr>
<td></td>
<td></td>
<td>$(1 - 2 \cos(T \omega_p) z^{-1} + z^{-2})$</td>
</tr>
<tr>
<td></td>
<td></td>
<td>$(1 - 2 \cos(T \omega_p) z^{-1} + z^{-2})$</td>
</tr>
</tbody>
</table>

Table 1: Summary of the characteristics of the cascaded CT $\Sigma$AMs designed using the proposed method.

<table>
<thead>
<tr>
<th>Modulator</th>
<th>2-1-1-1 Modulator</th>
<th>2-2-1 Modulator</th>
<th>3-2 Modulator</th>
</tr>
</thead>
<tbody>
<tr>
<td>$R_\mu$</td>
<td>$= 3.7 k\Omega$</td>
<td>$= 3.7 k\Omega$</td>
<td>$= 3.7 k\Omega$</td>
</tr>
<tr>
<td>$C_1$</td>
<td>$= 1.757 \mu F$</td>
<td>$= 1.757 \mu F$</td>
<td>$= 1.757 \mu F$</td>
</tr>
<tr>
<td>$k_{s1}$</td>
<td>$= 10 \mu S$</td>
<td>$= 10 \mu S$</td>
<td>$= 10 \mu S$</td>
</tr>
<tr>
<td>$k_{s2}$</td>
<td>$= 20 \mu S$</td>
<td>$= 20 \mu S$</td>
<td>$= 20 \mu S$</td>
</tr>
<tr>
<td>$k_{s3}$</td>
<td>$= 30 \mu S$</td>
<td>$= 30 \mu S$</td>
<td>$= 30 \mu S$</td>
</tr>
<tr>
<td>$k_{s4}$</td>
<td>$= 40 \mu S$</td>
<td>$= 40 \mu S$</td>
<td>$= 40 \mu S$</td>
</tr>
</tbody>
</table>

Table 2: Loop filter coefficients of the modulators in Fig.4.
References

Table 3: High-level sizing of the modulators in Fig.4(b) and Fig.4(c).

<table>
<thead>
<tr>
<th>Front-end opamp</th>
<th>Fig. 4(b)</th>
<th>Fig. 4(c)</th>
</tr>
</thead>
<tbody>
<tr>
<td>DC G</td>
<td>&gt;70 dB</td>
<td>&gt;60 dB</td>
</tr>
<tr>
<td>Phase Margin</td>
<td>60º</td>
<td>60º</td>
</tr>
<tr>
<td>Parasitic Input Capacitance</td>
<td>&lt;0.2 pF</td>
<td>&lt;0.2 pF</td>
</tr>
<tr>
<td>Parasitic Output Capacitance</td>
<td>&lt;0.2 pF</td>
<td>&lt;0.2 pF</td>
</tr>
<tr>
<td>Diff. Output Swing</td>
<td>&gt;0.5 V</td>
<td>&gt;0.5 V</td>
</tr>
<tr>
<td>Transconductors</td>
<td></td>
<td></td>
</tr>
<tr>
<td>DC G</td>
<td>&gt;50 dB</td>
<td>&gt;60 dB</td>
</tr>
<tr>
<td>Diff. Input Amplitude</td>
<td>0.3 V</td>
<td>0.4 V</td>
</tr>
<tr>
<td>Diff. Output Amplitude</td>
<td>0.3 V</td>
<td>0.4 V</td>
</tr>
<tr>
<td>Third-order non-linearity</td>
<td>&gt;56 dBV</td>
<td>&gt;53 dBV</td>
</tr>
</tbody>
</table>

Figure 5. Ideal output spectra of the cascaded CT ΣΔMs in Fig.4: (a) 2-1-1-1. (b) 2-2-1. (c) 3-2.

Figure 6. SNR loss vs. mismatch for: (a) 2-2-1 CT ΣΔM. (b) 3-2 CT ΣΔM.

Figure 7. Output Spectra for: (a) 2-2-1 CT ΣΔM. (b) 3-2 CT ΣΔM.
ANALYSIS OF CLOCK JITTER ERROR IN MULTIBIT CONTINUOUS-TIME
ΣΔ MODULATORS WITH NRZ FEEDBACK WAVEFORM
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ABSTRACT
This paper presents a detailed study of the clock jitter error in multibit continuous-time ΣΔ modulators with non-return-to-zero feedback waveform. Closed-form expressions are derived for the in-band error power and the signal-to-noise ratio showing that the jitter-induced noise can be separated into two main components: one depending on the modulator loop filter and the other one due to the input signal. The latter, not considered in previous approaches, allows us to accurately predict the signal-to-noise ratio degradation and to optimize the modulator performance in terms of jitter insensitivity. Moreover, the use of state-space formulation makes the analysis quite general and applicable to either cascaded or single-loop architectures. Time-domain simulations of several modulators are shown to validate the presented approach.1

1. INTRODUCTION
Nowadays, the increasing demand for ever faster Analog-to-Digital Converters (ADCs) in broadband communication systems has boosted the interest in Continuous-Time (CT) Sigma-Delta Modulators (ΣΔMs). These modulators offer an intrinsic anti-aliasing filtering and provide potentially higher sampling rates with lower power consumption than their Discrete-Time (DT) counterparts [1][2]. However, CT ΣΔMs are more sensitive than DT ΣΔMs to several circuit non idealities. One of their major degrading factors, especially in high-speed applications, is due to uncertainties in the clock signal edges, commonly referred to as clock jitter [1].

Clock jitter in CT ΣΔMs has been object of several studies reported in open literature [1][3]-[7]. Most of them were carried out considering ΣΔM architectures with an internal single-bit quantizer and a Return-to-Zero (RZ) Digital-to-Analog Converter (DAC). However, multibit quantization has been used in most silicon prototypes achieving medium-high resolutions (11-14 bit) within high signal bandwidths (1-15 MHz) [8]-[10]. The combined use of high-order (3rd-4th order) single-loop architectures with multibit (3-6 bit) quantization allows to reduce the oversampling ratio (normally < 12) while guaranteeing stability and robustness with respect to circuit parameter tolerances – the latter being a very critical error in CT ΣΔMs [1][2]. In addition to improve resolution, multibit quantization can reduce the sensitivity of CT ΣΔMs to clock jitter if a Non-Return-to-Zero (NRZ) feedback waveform is used in the DAC [9]. Therefore, their study is needed in order to optimize the modulator performance in terms of sensitivity to jitter error. The analysis of clock jitter in CT ΣΔMs considering a NRZ feedback waveform is mathematically more complex than using a RZ pulse shaping. In most cases, designers resort to semi-empirical estimations based on simulation results and consider a white-noise model for the jitter error [1][5][9]. To the best of the authors’ knowledge, only the work in [7] takes into account the effect of the modulator loop filter transfer function on the in-band jitter noise power of CT ΣΔMs with NRZ DAC. However, the analysis in [7] does not consider the effect of input signal for the sake of simplicity.

This paper analyzes the effect of signal-dependent clock jitter in multibit CT ΣΔMs with NRZ DAC. State-space formulation [11] is used to derive closed-form relations among jitter error, modulator specifications, loop filter transfer function and input signal parameters. The results of this study – applicable to any modulator topology – show effects not considered in previous approaches which become critical in high frequency applications. As an illustration several modulators using either single-loop or cascaded topologies are simulated to demonstrate the theoretical predictions.

2. CLOCK JITTER IN CT ΣΔMS WITH NRZ DACs
Fig.1 shows the conceptual block diagram of a single-loop CT ΣΔM. The loop filter is CT and the sampling operation is realized before quantization instead of at the modulator input as done in the case of DT ΣΔMs. Thus, the output signal, y(n), is DT, the input signal, x(t), is CT and a DT-to-CT transformation is implemented by the DAC to create the CT feedback signal, y(t). Therefore, there are two clocked building blocks subject to jitter error: the sampler and the DAC. The error introduced through the sampling process is reduced by the loop gain and shaped in the same way as the quantization noise and hence, its effect can be neglected. On the contrary, the jitter error associated to the DAC directly adds with the input signal, thus increasing the in-band noise power and degrading the modulator performance.

In the case of a NRZ DAC, the error sequence can be related to the output signal using the following relationship [1]:

\[ \epsilon(n) = (y(n) - y(n-1)) \frac{\Delta T(n)}{T_s} \]

where \( T_s \) is the sampling period and \( \Delta T(n) \) is the time uncertainty.

\[ x(t) \sum \text{Loop Filter} G(s) \]

\[ y(t) \]

\[ \text{DAC} \]

\[ y(n) \]

\[ \frac{\Delta T(n)}{T_s} \]

\[ \text{Figure 1. Conceptual block diagram of a single-loop CT ΣΔM.} \]

\[^1\] In order to simplify the notation, \( y(nT_s) \) is written as \( y(n) \) with \( T_s \) being the sampling period.

\[^2\] This work has been supported by the Spanish Ministry of Science and Education (with support from the European Regional Development Fund) under contract TEC2004-01752/MIC.
Assuming that the input signal and the quantization error are uncorrelated and that $\Delta T(n)$ is a Gaussian random process with zero mean and standard deviation $\sigma_\Delta T$, the power of the jitter error signal can be written as:

$$
P_e = E\{e(n)^2\} = \frac{\sigma_{\Delta T}^2}{T_s} E\{|y(n) - y(n-1)|^2\} = \sigma_{\Delta T}^2 T_s$$

where $E\{\cdot\}$ stands for the mathematical expectation [12] and $q(n)$ is the shaped quantization noise, given by:

$$q(z) = N_{TF}(z)e(z)$$

where $N_{TF}(z)$ represents the quantization Noise Transfer Function and $e(z)$ is the quantization error assumed to be a white noise source.

Considering a sinusoidal input signal of amplitude $A$ and angular frequency $\omega = \omega_n/T_s$, $\Delta x_n = [x(n) - x(n-1)]$ can be simplified as:

$$\Delta x_n \equiv \frac{d}{dt} x(t) \mid _{-T_s} = A\omega \cos(\omega_n(T_s - nT_s))$$

and hence,

$$E\{\Delta x_n^2\} = \frac{T_s^2 A^2 \omega^2}{2} E\{(\cos(\omega_n(T_s - nT_s)))^2\} = \frac{T_s^2 A^2 \omega^2}{2} \pi$$

The expectation value of $\Delta q_n = [q(n) - q(n-1)]$ can be derived from (3) giving:

$$E\{\Delta q_n^2\} = E\{Z^{-1}(1 - z^{-1})N_{TF}(z)e(z))^2\} = \frac{X_{ FS}^2 \pi}{12\pi(2^B - 1)} \left\| 1 - e^{-j\omega_0}N_{TF}(e^{j\omega_0}) \right\|^2 d\omega_0$$

where $X_{ FS}$ and $B$ are the full-scale and the internal number of bits of the quantizer, respectively.

From (2), (5) and (6), we obtain:

$$P_e \leq \left( \frac{\sigma_{\Delta T}}{T_s} \right)^2 \frac{X_{ FS}^2 \pi}{12\pi(2^B - 1)} \left\| 1 - e^{-j\omega_0}N_{TF}(e^{j\omega_0}) \right\|^2 d\omega_0$$

where $f_s = 1/T_s$ is the sampling frequency.

In some modulator topologies, the integration in (7) may become mathematically too complex, thus requiring the use of numerical solving methods. This can be simplified if the state-space formulation is used to derive $E\{\Delta q_n^2\}$ as shown in next section.

3. STATE-SPACE FORMULATION

Fig. 2 shows the state-space representation of $N_{TF}(z)$, which can be described by the following finite difference equations [12]:

$$\overline{y(n+1)}_0 = \overline{F}_0 \cdot \overline{y(n)}_0 + \overline{p}_0 \cdot e(n)$$

$$q(n) = \overline{g}_0 \cdot \overline{y(n)}_0 + e(n)$$

where $\overline{F}_0$ is the state matrix, $\overline{y(n)}_0$ is the $L \times 1$ state vector, $\overline{p}_0$ and $\overline{g}_0$ are $L \times 1$ vectors and $L$ is the order of $N_{TF}$.

Figure 2. State-space representation of $N_{TF}(z)$.

Equation system (8) can be solved recursively to find the relation between the initial state ($\overline{y(n)}_0$), previous input ($e(k)$), present input ($e(n)$) and output ($q(n)$) of the system [12]. This gives:

$$q(n) = \sum_{k=0}^{n-1} \overline{g}_0 \cdot \overline{F}_0^{-n-k} \cdot \overline{p}_0 \cdot e(k) + e(n)$$

Assuming that the initial state, $\overline{y(0)}_0$, is zero and considering that $E\{e(k)e(j)\} = 0$ for $k \neq j$, it can be shown from (9) that:

$$E\{q^2(n)\} = E\{e^2(n)\} + \sum_{k=0}^{n-1} \left[ \overline{g}_0 \cdot \overline{F}_0^{-n-k} \cdot \overline{p}_0 \right]^2$$

Diagonalizing $\overline{F}_0$ and considering that the system in Fig. 2 is stable, the expression in (10) can be re-written as:

$$E\{q^2(n)\} = E\{e^2(n)\} + \sum_{k=1}^{n-1} \frac{g_k \rho_k \rho_k^{-1} \lambda_j^{-1} \lambda_j}{1 - \lambda_k^{-1} \lambda_j}$$

where $\lambda_j$ are the eigenvalues of $\overline{F}_0$ and $g_k$ and $\rho_k$ are respectively the elements of $\overline{G} = \overline{g}_0 \overline{T}$ and $\overline{P} = \overline{T}^{-1} \overline{p}_0$, with $\overline{T}$ being the matrix of the eigenvectors of $\overline{F}_0$.

Using a similar procedure, it can be demonstrated that:

$$E\{q(n)q(n-1)\}$$

$$= E\{e(n)^2\} - \sum_{k=1}^{n-1} g_k \rho_k \rho_k^{-1} \lambda_j^{-1} \lambda_j$$

Taking into account that $E\{e(n)^2\} = \frac{X_{ FS}^2}{12\pi(2^B - 1)}$, and $E\{q(n)^2\} = E\{q(n-1)^2\}$, the value of $E\{\Delta q_n^2\}$ can be derived from (11) and (12) as:

$$E\{\Delta q_n^2\} = 2\left(E\{q(n)^2\} - E\{q(n)q(n-1)\}\right) = \frac{X_{ FS}^2}{6(2^B - 1)} \psi(\gamma, \beta, L)$$

where

$$\psi(\gamma, \beta, L) = 1 - \frac{\gamma^T \gamma - \sum_{k=1}^{n-1} g_k \rho_k \rho_k^{-1} \lambda_j^{-1} \lambda_j}{1 - \lambda_k^{-1} \lambda_j}$$

Replacing (6) with (13) in (7) and assuming that the jitter noise is an additive noise source at the input of the modulator, the Signal-to-Noise Ratio (SNR) dominated by jitter can be written as:

$$SNR = \frac{A^2}{B_w \cdot \sigma_{\Delta T}^2 \left[ \frac{X_{ FS}^2}{12\pi(2^B - 1)} \psi(\gamma, \beta, L) \right]}$$
where $B_w$ is the signal bandwidth.

Note that in the denominator of (15), $(\sigma_{AT})^2$ is multiplied by a factor that is the sum of two terms: one depending on the input signal parameters ($A$ and $\theta_0$) and the other one which is a function of the modulator topology parameters $(B, N_{FS}, \psi(g, p, \lambda, L))$. The first term decreases with $f_s$ while the second term increases with $f_s$. This is illustrated in Fig.3 where the two terms in brackets in the denominator of (15) are plotted versus $f_s$ for a 5-bit 3rd-order single-loop CT $\Sigma M$ with $f_s = B_w = 20MHz$. Note that there is an optimum value of $f_s$, $f_{op} = 170MHz$, that minimizes the in-band jitter noise power and hence, maximizes $SNR^*$. Thus, using (15) as a figure of merit in multibit CT $\Sigma M$s with NRZ DAC in which jitter is the main limiting factor, the modulator performance can be optimized for given specifications in terms of loop filter parameters, sampling frequency and the number of bits of the internal quantizer.

It is important to mention that the effect of $N_{FS}$ on the in-band jitter noise of multibit NRZ CT $\Sigma M$s was previously studied in [7]. However, it did not take into account the impact of signal-dependent jitter term, which can be very critical in broadband applications as illustrated in next section.

### 4. SIMULATION RESULTS

The presented study has been validated through time-domain behavioural simulation using SIMSIDES, a SIMULINK-based simulator for $\Sigma M$s [13]. Fig.4 shows the multibit NRZ CT $\Sigma M$s under study. Fig.4(a) is a 3rd-order single-loop and Fig.4(b) is a cascaded 2-1 topology. In both architectures, feed-forward stabilization is used and a feedback coefficient $k$ is used to move one of the poles to an optimum position [14]. The modulators were synthesized to handle signals within $B_w = 20MHz$ for VDSL application.

Three different cases are considered:

- **CT $\Sigma M$1**: Fig.4(a) with $f_s = 400MHz$ and $B = 2$
- **CT $\Sigma M$2**: Fig.4(a) with $f_s = 160MHz$ and $B = 5$
- **CT $\Sigma M$3**: Fig.4(b) with $f_s = 160MHz$ and $B_1 = B_2 = 5$

where $B_1$ and $B_2$ are respectively the number of bits of the quantizer in the first- and second- stage in Fig.4(b).

Table 1 shows the values of the loop-filter coefficients ($k_i$) as well as the position of the poles and Table 2 shows the values of $g_r$, $p_i$ and $\lambda_i$ for the three cases mentioned above.

![Figure 3. Jitter components vs. $f_s$ for a 5-bit 3rd order CT $\Sigma M$.](image)

†3. The values of $g_r$, $p_i$ and $\lambda_i$ for $f_s = f_{op} = 170MHz$ are shown in Fig.3.

![Figure 4. Multibit NRZ CT $\Sigma M$s under study. (a) 3rd-order single-loop architecture. (b) Cascaded 2-1 architecture.](image)

Fig.5 shows several simulated output spectra of cases CT $\Sigma M$1 (Fig.5(a)) and CT $\Sigma M$2 (Fig.5(b)) corresponding to different values of $f_s$ and $\sigma_{AT} = 25 ps$. Note that in Fig.5(a), the in-band noise power does not depend on $f_s$ as predicted by [7]. However, as $B$ increases from $B = 2$ to $B = 5$, the modulator-dependent term in (15) decreases and hence, the in-band noise is dominated by the signal-dependent term as illustrated in Fig.5(b). This effect is better shown in Fig.6, where the $SNR$-peak of the modulators in Fig.4 is plotted vs. $\sigma_{AT}$ for several values of $f_s$, showing simulation results and theoretical predictions†4. For comparison pur-

### Table 1: Loop-filter coefficients of CT $\Sigma M$s in Fig.4

<table>
<thead>
<tr>
<th>CT $\Sigma M$1</th>
<th>CT $\Sigma M$2</th>
<th>CT $\Sigma M$3</th>
</tr>
</thead>
<tbody>
<tr>
<td>$k_{i1}$</td>
<td>1.5</td>
<td>2</td>
</tr>
<tr>
<td>$k_{i2}$</td>
<td>-1.5</td>
<td>-2</td>
</tr>
<tr>
<td>$k_{i3}$</td>
<td>1</td>
<td>1</td>
</tr>
<tr>
<td>$b_{i1}$</td>
<td>0.1</td>
<td>0.137</td>
</tr>
<tr>
<td>$b_{i2}$</td>
<td>0.6</td>
<td>1</td>
</tr>
<tr>
<td>$b_{i3}$</td>
<td>0.5</td>
<td>1</td>
</tr>
<tr>
<td>$\lambda_{i1}$</td>
<td>1</td>
<td>1</td>
</tr>
<tr>
<td>$\lambda_{i2}$</td>
<td>0.5</td>
<td>1</td>
</tr>
<tr>
<td>$\lambda_{i3}$</td>
<td>-</td>
<td>-</td>
</tr>
<tr>
<td>Poles</td>
<td>$\omega_1 = 0$</td>
<td>$\omega_2 = \sqrt{3}/2 \pi B_w$</td>
</tr>
</tbody>
</table>

### Table 2: Values of $g_r$, $p_i$ and $\lambda_i$ for the CT $\Sigma M$s in Fig.4

<table>
<thead>
<tr>
<th>CT $\Sigma M$1</th>
<th>CT $\Sigma M$2</th>
<th>CT $\Sigma M$3</th>
</tr>
</thead>
<tbody>
<tr>
<td>$\tau$</td>
<td>$[0.528, 0.664, 0.664]$</td>
<td>$[0.122, 0.122, 0.122]$</td>
</tr>
<tr>
<td>$\sigma$</td>
<td>$[0.56, 0.853, 0.853]$</td>
<td>$[0.81, 0.81, 0.81]$</td>
</tr>
<tr>
<td>$\rho$</td>
<td>$[3.503, 0.016, 0.016]$</td>
<td>$[1.476, 1.476, 1.476]$</td>
</tr>
<tr>
<td>$\lambda$</td>
<td>$[-5.69, -5.69, -5.69]$</td>
<td>$[-5.69, -5.69, -5.69]$</td>
</tr>
</tbody>
</table>
poses, predictions given by [7] are also included. Note that, simulated and theoretical data matched very well when the combined effect of signal- and modulator-dependent jitter noise is taken into account as shown in this work.

CONCLUSIONS
The effect of clock jitter error on multibit CT ΣΔMs with NRZ DAC has been analyzed. Based on the use of state-space formulation, easy-to-compute closed-form expressions have been derived for the noise power and signal-to-noise ratio. It has been demonstrated that the jitter-induced noise has two components: one depending on signal parameters and the other one depending on the modulator loop filter. Their combined effect, not predicted by previous approaches, has been confirmed by time-domain simulations of several CT ΣΔMs intended for VDSL application.

REFERENCES

†4. Expression (15) is replaced in Fig.6 with the ideal value of \( SNR \) for \( \sigma_{\Delta T} = 1 \).
A DIRECT SYNTHESIS METHOD OF CASCADED CONTINUOUS-TIME SIGMA-DELTA MODULATORS

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ABSTRACT

This paper presents an efficient method to synthesize cascaded sigma-delta modulators implemented with continuous-time circuits. It is based on the direct synthesis of the whole cascaded architecture in the continuous-time domain instead of using a discrete-to-continuous time transformation as has been done in previous approaches. In addition to place the zeroes of the loop filter in an optimum way, the proposed methodology leads to more efficient architectures in terms of circuitry complexity, power consumption and robustness with respect to circuit non-idealities.1

1. INTRODUCTION

Continuous-Time (CT) Sigma-Delta Modulators (ΣΔMs) have demonstrated to be an attractive solution for the implementation of Analog-to-Digital (A/D) interfaces in systems-on-chip integrated in deep-submicron standard CMOS technologies [1]. Although most reported ΣΔMs have been implemented using Discrete-Time (DT) circuits, the increasing demand for broadband data communication systems has motivated the use of CT techniques. In addition to show an intrinsic antialiasing filtering, CT ΣΔMs provide potentially faster operation with lower power consumption than their DT counterparts [2][3]. The latter are specially critical for the realization of cascaded architectures. This has forced the use of single-loop topologies in most reported silicon prototypes even though low oversampling ratios (< 12) are needed [4][5], whereas very few cascaded CT ΣΔM Integrated Circuits (ICs) have been reported [6].

However, the need to achieve medium-high resolutions (> 12bits) within high signal bandwidths (> 20MHz) while guaranteeing stability, has prompted the interest in proper methods for the synthesis of high-order cascaded CT ΣΔMs [7]-[9]. These methods are based on applying a DT-to-CT transformation to an equivalent DT topology that fulfills the required specifications. In most cases, the use of such a transformation is normally translated into an increase of the analog circuit complexity with the subsequent penalty in silicon area, power consumption and sensitivity to parameter tolerances.

This paper presents a direct synthesis method of cascaded CT ΣΔMs which, dispensing with the DT-to-CT equivalence, allows to reduce the number of analog components and to efficiently place the zeroes/poles of the noise transfer function, thus yielding to more robust architectures than using a DT-to-CT transformation.

2. CASCADED CT ΣΔ MODULATORS

Fig.1 shows the conceptual block diagram of a m-stage cascaded CT ΣΔM. Each stage, consisting of a single-quantizer CT ΣΔM, re-modulates a signal containing the quantization error generated in the previous stage. Once in the digital domain, the outputs, $y_i$, of the stages are properly processed and combined (by the cancellation logic) in order to cancel out the quantization errors of all the stages, but the last one in the cascade. This latter error appears at the overall modulator output shaped by a function of order equal to the summation of the order of all the stages.

Cascaded CT ΣΔMs are normally synthesized from equivalent (well-known) DT systems and use the same digital cancellation logic [8]. This DT/CT equivalence can be guaranteed because the overall open loop transfer function of each stage in Fig.1 is in fact a DT system [2]. Thus, in the case of a rectangular impulsive response of the Digital-to-Analog Converter (DAC), it can be shown that the equivalent DT loop filter

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1. This work has been supported by the Spanish Ministry of Science and Education (with support from the European Regional Development Fund) under contract TEC2004-01752/MIC.
The transfer function is given by [10][11]:

\[
F(z) = \sum_{p_i} \text{Re} \left( \frac{F(s)}{s} \cdot \frac{e^{m_1 T_s s}}{z - e^{m_1 T_s s}} \right) \sum_{p_i} \text{Re} \left( \frac{F(s)}{s} \cdot \frac{e^{m_2 T_s s}}{z - e^{m_2 T_s s}} \right)
\]

where \( f_s = 1/T_s \) is the sampling frequency; \( m_1 = 1 - T_x/T_s \); \( m_2 = 1 - (T_x + \tau)/T_s \); \( T_x \) and \( \tau \) are respectively the time delay and pulse width of the DAC waveform; \( p_i \) are the poles of \( F(s)/s \) and \( \text{Re}(x) \) stands for the residue of \( x \).

However, in order to get a functional CT \( \Sigma \Delta \) while keeping the cancellation logic of the original DT \( \Sigma \Delta \), every state variable and DAC output must be connected to the integrator input of later stages [8], thus increasing the number of analog components, i.e. transconductors, amplifiers, and DACs. As an illustration, Fig.2(a) shows a cascaded 2-1-1 CT \( \Sigma \Delta \) obtained from an existing DT \( \Sigma \Delta \) [12]. Note that at least eight scaling coefficients \( (k_{g2-g5}) \) and their corresponding signal paths are needed to connect the different stages of the modulator. The number of integrating paths can be reduced – as illustrated in Fig.2(b) – if the whole cascaded \( \Sigma \Delta \) is directly synthesized in the CT domain as proposed in the next section.

3. PROPOSED METHODOLOGY

The idea of dispensing with the DT-to-CT transformation was previously reported in [3] for single-loop architectures. However, in the case of cascaded architectures, the cancellation logic functions (not present in single-loop \( \Sigma \Delta \)'s) must be included in the synthesis procedure in order to get an optimum architecture.

Let's consider the more general case of the \( m \)-stage cascaded CT \( \Sigma \Delta \) shown in Fig.1. The overall output, \( y_o \), is given by:

\[
y_o(z) = \sum_{k=1}^{m} y_k(z)CL_k(z)
\]

where \( y_k(z) \) and \( CL_k(z) \) represent respectively the output and partial cancellation logic transfer function of the \( k \)-th stage.

If the modulator input, \( x(t) \), is set to zero, it can be shown that the output of each stage can be written as:

\[
y_k(z) = \frac{E_k(z) + \sum_{i=1}^{k-1} Z \left( L^{-1} [H_D F_{ik}] \right) y_i(z)}{1 - Z \left( L^{-1} [H_D F_{kk}] \right) y_k(z)}
\]

where \( Z \) stands for the \( Z \)-transform, \( L^{-1} \) is the inverse Laplace transform, \( H_D = H_{DAC}(s) \) is the transfer function of the DAC, and

\[
F_{ij} = F_{ij}(s) = \frac{\text{Input Quantizer} j}{y_j(x)}
\]

represents the transfer function from \( y_j(x) \) to the input of \( j \)-th quantizer.

Using the notation \( Z \left( L^{-1} [H_D F_{km}] \right) y_k(z) \), the output of each stage is given by:

\[
y_k(z) = \frac{E_k(z) + \sum_{i=1}^{k-1} Z_{ik} y_i(z)}{1 - Z_{kk} y_k(z)}
\]

and the output of the modulator can be written as:

\[
y_o = \sum_{k=1}^{m} y_k CL_k = \sum_{k=1}^{m} \left[ \frac{E_k}{1 - Z_{kk}} + \frac{1}{1 - Z_{kk}} \sum_{i=1}^{k-1} Z_{ik} y_i \right] CL_k
\]

The partial cancellation logic transfer functions can be calculated by imposing the cancellation of the transfer function of the first \( m - 1 \) quantization errors \( E_k(z) \) in (6). This gives:

\[
CL_k(z) = \frac{-Z_{km} CL_k}{1 - Z_{mm}} = \frac{-Z \left( L^{-1} [H_D F_{km}] \right) CL_m(z)}{1 - Z \left( L^{-1} [H_D F_{mm}] \right) y_m(z)}
\]

Figure 2. Cascaded 2-1-1 CT \( \Sigma \Delta \) architecture obtained (a) from an equivalent DT \( \Sigma \Delta \) (b) using the proposed method.
where the partial cancellation logic transfer function of the last stage, \( CL_3(z) \), can be chosen to be the simplest form that preserves the required noise shaping.

It is important to mention that the design equations (2)-(7) do not only take into account the single-stage loop filter transfer functions \( F_{ij}(s) \), but also the inter-stage loop filter transfer functions \( F_{ij} \neq j \). The latter are continuous-time integrating paths appearing only when the modulator stages are connected to form the cascaded \( \Sigma\Delta \)M and must be included in the synthesis methodology to obtain a functional modulator with minimum number of inter-stage paths.

Therefore, the following procedure can be used in a systematic methodology for the synthesis of cascaded CT \( \Sigma\Delta \)Ms \(^{52}\):

- First, the poles of different transfer functions \( F_{ij}(s) \) are optimally placed in the signal bandwidth for given specifications. Scaling is needed in order to optimize the dynamic range of each integrator. This process is carried out entirely in the CT domain and no equivalence to an existing DT modulator needs to be imposed.
- Second, once the individual stages are designed and optimized, cancellation logic are calculated using (7).

### 4. SYNTHESIS EXAMPLE

For illustrative purposes, the 2-1-1 CT \( \Sigma\Delta \)M of Fig.2(b) is synthesized using (2)-(7) to achieve 16-bit resolution in a 750 kHz bandwidth, with a sampling frequency of 48MHz (oversampling ratio, \( M = 32 \)) \(^{12}\). Although in the proposed methodology the modulator in Fig.2(b) would be entirely designed in the CT domain, a slightly different approach will be used in this particular case in order to facilitate the comparison of the performance of both modulators in Fig.2. The coefficients of the first stage \( (k_{i1}, k_g, k_{b1}, k_{b2}) \) are taken to be equal in both systems and are obtained from a DT-to-CT transformation of the first stage of a DT \( \Sigma\Delta \)M in \(^{12}\). The rest of coefficients in Fig.2(b) are taken such that the time constant of the integrators is the inverse of the sampling frequency:

\[
\begin{align*}
  k_{i1} & = k_g = 1/4; \quad k_{b1} = -3/8; \\
  k_{b2} & = k_{i2} = -k_{b3} = k_{i3} = -k_{b4} = 1
\end{align*}
\]

Hence, the single-loop and inter-stage transfer functions are given by:

\[
\begin{align*}
  F_{13} & = \frac{(sT_i k_{b2} + k_{b1})k_{i2}k_{i3}}{(sT_i)^3} \\
  F_{23} & = \frac{k_{b3}k_{i3}}{(sT_i)^2} \\
  F_{33} & = \frac{k_{b4}}{sT_i}
\end{align*}
\]

and the partial cancellation logic transfer functions can be calculated using (7). This gives:

\[
\begin{align*}
  CL_1 & = \frac{-Z\left\{L^{-1}[H_D F_{13}]|_{n T_i}\right\}}{1 - Z\left\{L^{-1}[H_D F_{33}]|_{n T_i}\right\}} \\
  CL_2 & = \frac{-Z\left\{L^{-1}[H_D F_{23}]|_{n T_i}\right\}}{1 - Z\left\{L^{-1}[H_D F_{33}]|_{n T_i}\right\}} \\
  CL_3 & = \frac{-Z\left\{L^{-1}[H_D F_{23}]|_{n T_i}\right\}}{1 - Z\left\{L^{-1}[H_D F_{33}]|_{n T_i}\right\}}
\end{align*}
\]

From (8)-(10) and using a Non-Return-to-Zero (NRZ) DAC, the following cancellation logics are derived:

\[
\begin{align*}
  CL_1 & = \frac{z^{-1}}{48}(7 + 29z^{-1} - 7z^{-2} - 5z^{-3}) \\
  CL_2 & = \frac{z^{-1}(1 + z^{-1})(1 - z^{-1})^2}{2} \\
  CL_3 & = \frac{2(1 - z^{-1})^3}{2}
\end{align*}
\]

where \( CL_3 \) is chosen to have three zeroes at DC, corresponding to the zeroes contributed by the first three integrators.

In order to verify the proposed methodology, both modulators in Fig.2 were simulated using SIMSIDES, a SIM-ULINK-based time-domain behavioral simulator for \( \Sigma\Delta \)Ms \(^{13}\). Fig.3 shows two ideal output spectra of the modulators

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\(^{52}\) In this procedure, the modulator order, oversampling ratio and number of bits of internal quantizers are assumed to be determined for given specifications from well-known expressions \(^{1}\).
showing a similar performance. The effect of mismatch on the Signal-to-Noise Ratio (SNR) was also simulated. For this purpose, maximum values of mismatch were estimated for a 0.18 μm CMOS technology and both modulators in Fig.2 were simulated considering a gm-C implementation. The results are shown in Fig.4, where the SNR loss is represented as a function of the standard deviation of the transconductances (σ_m) and capacitances (σ_C). For each point of these surfaces, 150 simulations were carried out using random variations with the standard deviation given in the diagrams. The value of SNR loss represented in Fig.4 stands for the difference between the ideal SNR, i.e. with no parameter variation, and the SNR with 90% of the 150 simulations above it. It is shown that the lower analog component count in Fig.2(b) is reflected in a lower variance of the modulator coefficients, leading to a better behaviour in terms of sensitivity to mismatch.

The same reasoning can be applied to the requirements in terms of DC gain of the individual transconductors. Since the number of transconductors connected to the same node is higher in the previous method, the equivalent impedance associated with these nodes tends to be lower and the requirements in terms of the individual transconductor output impedance is higher. Therefore, a higher DC gain is needed. Fig.5 illustrates this point. Note that the SNR-peaks starts dropping at a DC gain ≡ 8dB higher in the case of the system designed following the previous method.

![Image](image_url)

**Figure 4.** Effect of mismatch on the SNR of a cascaded 2→1→1 CT ΣΔM obtained from: (a) an equivalent DT ΣΔM; (b) proposed method.

![Image](image_url)

**Figure 5.** Effect of DC gain on the SNR-peak.

## CONCLUSIONS

In this paper a new methodology of synthesizing cascaded continuous-time ΣΔ modulators has been presented. It has demonstrated that more efficient topologies in terms of circuit complexity can be generated if the design is directly done in the continuous-time domain and the cancellation logic transfer function is taken into account in the synthesis procedure. Behavioral simulations considering critical error mechanisms validate the presented approach.

## REFERENCES

Continuous-Time Cascaded $\Sigma\Delta$ Modulators for VDSL:
A Comparative Study

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Instituto de Microelectrónica de Sevilla, IMSE-CNM (CSIC)
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ABSTRACT

This paper describes new cascaded continuous-time $\Sigma\Delta$ modulators intended to cope with very high-rate digital subscriber line specifications, i.e. 12-bit resolution within a 20-MHz signal bandwidth. These modulators have been synthesized using a new methodology that is based on the direct synthesis of the whole cascaded architecture in the continuous-time domain instead of using a discrete-to-continuous time transformation as has been done in previous approaches. This method allows to place the zeros/poles of the loop-filter transfer function in an optimal way and to reduce the number of analog components, namely: transconductors and/or amplifiers, resistors, capacitors and digital-to-analog converters. This leads to more efficient topologies in terms of circuitry complexity, power consumption and robustness with respect to circuit non-idealities. A comparison study of the synthesized architectures is done considering their sensitivity to most critical circuit error mechanisms. Time-domain behavioral simulations are shown to validate the presented approach.

Keywords: Analog-to-digital converters, sigma-delta modulators, continuous-time circuits.

1. INTRODUCTION

Continuous-Time (CT) Sigma-Delta Modulators ($\Sigma\Delta$s) have demonstrated to be an attractive solution for the implementation of Analog-to-Digital (A/D) interfaces in systems-on-chip integrated in deep-submicron standard CMOS technologies. Although most reported $\Sigma\Delta$s have been implemented using Discrete-Time (DT) circuits, the increasing demand for broadband data communication systems has motivated the use of CT circuit techniques. In addition to show an intrinsic anti-aliasing filtering, CT $\Sigma\Delta$s provide potentially faster operation with lower power consumption than their DT counterparts.

In spite of their mentioned advantages, CT $\Sigma\Delta$s are more sensitive than DT $\Sigma\Delta$s to some circuit errors, namely: clock jitter, excess loop delay and technology parameter variations. The latter are specially critical for the realization of cascaded architectures. This has forced the use of single-loop topologies in most reported silicon prototypes even though low oversampling ratios ($<12$) are needed, whereas very few cascaded CT $\Sigma\Delta$ Integrated Circuits (ICs) have been reported.

However, the need to achieve medium-high resolutions (>12 bits) within high signal bandwidths (>20MHz) while guaranteeing stability, has prompted the interest in proper methods for the synthesis of high-order cascaded CT $\Sigma\Delta$s. These methods are based on applying a DT-to-CT transformation to an equivalent DT topology that fulfills the required specifications. In most cases, the use of such a transformation is normally translated into an increase of the analog circuit complexity with the subsequent penalty in silicon area, power consumption and sensitivity to parameter tolerances.

This paper presents a direct synthesis method of cascaded CT $\Sigma\Delta$s which, dispensing with the DT-to-CT equivalence, make it possible to reduce the analog circuitry complexity and place the zeros/poles of the quantization noise transfer function in an optimal way, thus yielding to more robust architectures than using a DT-to-CT transformation. As an application, the proposed methodology is used to find optimum CT $\Sigma\Delta$s for Very high-rate Digital Subscriber Line (VDSL). Three fifth-order cascaded topologies are synthesized: 2-1-1-1, 2-2 and 3-2. These modulators are designed for 12-bit@20-MHz specifications and their performances are compared in terms of time-domain simulations that take into account critical error mechanisms like mismatch and clock jitter error.

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2. CASCaded CONTINUOUS-TIME $\Sigma\Delta$ MODULATORS

Fig.1 shows the conceptual block diagram of a $m$-stage cascaded CT $\Sigma\Delta$ M. Each stage, consisting of a single-quantizer CT $\Sigma\Delta$, re-modulates a signal containing the quantization error generated in the previous stage. Once in the digital domain, the outputs, $y_i$, of the stages are properly processed and combined (by the cancellation logic) in order to cancel out the quantization errors of all the stages, but the last one in the cascade. This latter error appears at the overall modulator output shaped by a function of order equal to the summation of the orders of all the stages.

Cascaded CT $\Sigma\Delta$s are normally synthesized from equivalent (well-known) DT systems and use the same digital cancellation logic. This DT/CT equivalence can be guaranteed because the overall open loop transfer function of each stage in Fig.1 is in fact a DT system. Thus, in the case of a rectangular impulsive response of the Digital-to-Analog Converter (DAC), it can be shown that the equivalent DT loop filter transfer function is given by:

$$F(z) = \sum_{p_i} \text{Re} \left( \frac{F(s)}{s} \cdot \frac{e^{m_1 T \cdot s}}{z - e^{T \cdot s}} \right) \cdot \sum_{p_i} \text{Re} \left( \frac{F(s)}{s} \cdot \frac{e^{m_2 T \cdot s}}{z - e^{T \cdot s}} \right)$$

(1)

where $f_s = 1/T_s$ is the sampling frequency; $m_1 = 1 - t_d/T_s$; $m_2 = 1 - (t_d + \tau)/T_s$; $t_d$ and $\tau$ are respectively the time delay and pulse width of the DAC waveform; $p_i$ are the poles of $F(s)/s$ and $\text{Re}(x)$ stands for the residue of $x$.

In order to get a functional CT $\Sigma\Delta$ while keeping the cancellation logic of the original DT $\Sigma\Delta$, every state variable and DAC output must be connected to the integrator input of later stages. This increases the number of analog components, i.e. transconductors, amplifiers and DACs. As an illustration, Fig.2(a) shows a cascaded 2-1-1 CT $\Sigma\Delta$ obtained from an existing DT $\Sigma\Delta$. Note that at least eight scaling coefficients $(k_{g2-g})$ and their corresponding signal paths are needed to connect the different stages of the modulator. The number of integrating paths can be reduced — as shown in Fig.2(b) – if the whole cascaded $\Sigma\Delta$ is directly synthesized in the CT domain as proposed in the next section.

3. PROPOSED SYNTHESIS METHODOLOGY

The idea of dispensing with the DT-to-CT transformation was previously reported in for single-loop architectures. However, in the case of cascaded architectures, the cancellation logic functions (not present in single-loop $\Sigma\Delta$s) must be included in the synthesis procedure to get an optimum architecture.

Let us consider the more general case of the $m$-stage cascaded CT $\Sigma\Delta$ shown in Fig.1. The overall output, $y_o$, is given by:

$$y_o(z) = \sum_{k=1}^{m} y_k(z)CL_k(z)$$

(2)

![Figure 1. Conceptual block diagram of a cascaded CT $\Sigma\Delta$.](image-url)
where \( y_k(z) \) and \( CL_k(z) \) represent respectively the output and partial cancellation logic transfer function of the \( k \)-th stage.

If the modulator input, \( x(t) \), is set to zero, the output of each stage can be written as:

\[
y_k(z) = \frac{E_k(z) + \sum_{i=1}^{k-1} Z \left( L^{-1} \left[ H_D F_{ik} \right] \right) y_i(z)}{1 - Z \left( L^{-1} \left[ H_D F_{kk} \right] \right)}
\]  

(3)

where \( Z \) stands for the Z-transform, \( L^{-1} \) is the inverse Laplace transform, \( H_D = H_{DAC}(s) \) is the transfer function of the DAC, and

\[
F_{ij} = \frac{\text{Input Quantizer } j}{y_i(s)}
\]  

(4)

represents the transfer function from \( y_i(s) \) to the input of \( j \)-th quantizer.

Using the following notation

\[
Z_{km} = Z \left( L^{-1} \left[ H_D F_{km} \right] \right)
\]  

(5)

the output of each stage is given by:

\[
y_k(z) = \frac{E_k(z)}{1 - Z_{kk}} + \sum_{i=1}^{k-1} \frac{Z_{ik} y_i(z)}{1 - Z_{kk}}
\]  

(6)

and the output of the modulator can be written as:

\[
y_o = \sum_{k=1}^{m} y_k CL_k = \sum_{k=1}^{m} \left( \frac{E_k}{1 - Z_{kk}} + \frac{1}{1 - Z_{kk}} \sum_{i=1}^{k-1} Z_{ik} y_i \right) CL_k
\]  

(7)
The partial cancellation logic transfer functions (\( CL_k \)) can be calculated by imposing the cancellation of the transfer function of the first \( m - 1 \) quantization errors \( E_i(z) \) in (7). This gives:

\[
\hat{L}_k(z) = \frac{-Z_{km}CL_m}{1-Z_{mm}} = \frac{-Z \left[ L^{-1}[H_0F_{km}]_{nT_s} \right] \left[ CL_m(z) \right]}{1-Z \left[ L^{-1}[H_0F_{mm}]_{nT_s} \right]}
\]  

(8)

where the partial cancellation logic transfer function of the last stage, \( CL_m(z) \), can be chosen to be the simplest form that preserves the required noise shaping.

Note that the design equations (2)-(8) do not only take into account the single-stage loop filter transfer functions \( (F_{ji}) \), but also the inter-stage loop filter transfer functions \( (F_{ij} \neq j) \). The latter are continuous-time integrating paths appearing only when the modulator stages are connected to form the cascaded \( \Sigma \Delta M \) and must be included in the synthesis methodology to obtain a functional modulator with minimum number of inter-stage paths.

Therefore, the following procedure can be used in a systematic methodology for the synthesis of cascaded CT \( \Sigma \Delta Ms \):\(^{11}\)

- First, the poles of single-stage transfer functions \( (F_{ij}(s)) \) are optimally placed in the signal bandwidth for given specifications. This process is carried out entirely in the CT domain and no equivalence to an existing DT modulator needs to be imposed.
- Second, once the individual stages are designed and optimized, cancellation logics are calculated using (8).

For illustrative purposes, the 2-1-1 CT \( \Sigma \Delta M \) of Fig.2(b) was synthesized using (2)-(8) to achieve 16-bit resolution in a 750-kHz bandwidth, with a sampling frequency of 48MHz (oversampling ratio, \( M = 32 \)). For simplicity, in order to facilitate the comparison of the performance of both modulators in Fig.2, the coefficients of the first stage \( (k_{n1}, k_{f1}, k_{f3}, k_{f4}) \) are taken to be equal in both systems and are obtained from a DT-to-CT transformation of the first stage of a DT \( \Sigma \Delta M \) in.\(^{12}\) The rest of coefficients in Fig.2(b) are taken such that the time constant of the integrators is the inverse of the sampling frequency \( (T_s = 1/f_s) \):

\[
k_{n1} = -k_{f3} = 1/4; \quad k_{f2} = -3/8; \quad k_{f1} = k_{n2} = -k_{f3} = k_{n3} = -k_{f4} = 1
\]  

(9)

Hence, the single-loop and inter-stage transfer functions are given by:

\[
F_{11} = \frac{\frac{3T_s}{8}s^2 + 1}{(sT_s)^2} \quad F_{22} = F_{33} = \frac{-1}{sT_s}
\]  

\[
F_{13} = \frac{\frac{3T_s}{8}s^2 + 1}{(sT_s)^4} \quad F_{23} = \frac{-1}{(sT_s)^3}
\]  

(10)

and the partial cancellation logic transfer functions can be calculated using (8)-(10). Considering a Non-Return-to-Zero (NRZ) DAC, the following cancellation logics are derived:

\[
CL_1 = \frac{z^{-1}}{48}(7 + 29z^{-1} - 7z^{-2} - 5z^{-3})
\]  

\[
CL_2 = z^{-1}(1 + z^{-1})(1 - z^{-1})^2
\]  

\[
CL_3 = 2(1 - z^{-1})^3
\]  

(11)

\(^{11}\) In this procedure, the modulator order, oversampling ratio and number of bits of internal quantizers is assumed to be determined for given specifications from well-known expressions.\(^{1}\)
where $CL_1$ is chosen to have three zeroes at DC, corresponding to the zeroes contributed by the first three integrators.

In order to compare the robustness of both modulators in Fig.2, the effect of mismatch on the Signal-to-Noise Ratio (SNR) was also simulated using SIMSIDES, a SIMULINK-based time-domain behavioral simulator for ΣΔMs. For this purpose, maximum values of mismatch were estimated for a 0.13 μm CMOS technology and both modulators in Fig.2 were simulated considering a Gm-C implementation. The results are shown in Fig.3, where the SNR loss is represented as a function of the standard deviation of the transconductances ($\sigma_{gm}$) and capacitances ($\sigma_C$). For each point of these surfaces, 150 simulations were carried out using random variations with the standard deviation given in the diagrams. The value of SNR lost represented in Fig.3 stands for the difference between the ideal SNR, i.e. with no parameter variation, and the SNR with 90% of the 150 simulations above it. It is shown that the lower analog component count in Fig.2(b) is reflected in a lower variance of the modulator coefficients, leading to a better behavior in terms of sensitivity to mismatch.

4. APPLICATION TO VDSL

As an application of the proposed methodology, three 5th-order cascaded CT ΣΔMs, shown in Fig.4, were synthesized to cope with VDSL specifications: 12-bit resolution within a 20-MHz signal bandwidth. In order to fulfill these specifications without being limited by the clock jitter error, the sampling frequency, $f_s$, and the number of bits of the internal quantizers (and DACs), $B$, must be properly chosen. In the case of a 5th-order modulators like those shown in Fig.4, the in-band jitter noise power is minimized for $f_s = 240$ MHz and $B = 4$.

Another critical source of error in CT ΣΔMs is the excess loop delay. As shown in this error can be compensated by adding an extra feedback branch between the output and the input to the quantizer (DAC2 in Fig.4) and two D-latches. By adding this extra branch with the appropriate gain, the loop impulse response is exactly the same as that of the original. This extra feedback term can be easily included in the calculation of the cancellation logic. In a practical implementation it could be advantageous to make DAC2 programmable.

Considering the factors above, the CT ΣΔMs in Fig.4 were synthesized using the methodology described in Section 3, taking into account the following considerations:

- The first stage of the 2-1-1-1 architecture (Fig.4(a)) is formed by a resonator which has its poles placed at $\omega_p = 2\pi \sqrt{7/9} f_s$, in order to minimize the quantization Noise Transfer Function (NTF) in the signal bandwidth, $B_w$. Resistor variations can be tuned out using a combination of a discrete rough tuning of the resistors ($R_{in}, R_{fb}$ and $R_c$) and a continuous fine tuning of the transconductors $k_{ff}$ and $k_{f1}$. This tuning can be also used to cancel the effect of finite Gain-Bandwidth product (GB) of the front-end opamp, due to the fact that this error can be modelled as an integrator gain error. All the other transconductors could be tuned in order to keep the time constant $C/g_m$ unchanged over $C$ variations.

- An additional resonator has been used in the 2-2-1 architecture (Fig.4(b)), in order to optimally distribute the poles of NTF.

![Figure 3](image-url)  

Figure 3. Effect of mismatch on the SNR of a cascaded 2-1-1 CT ΣΔM obtained from: (a) an equivalent DT ΣΔM; (b) proposed method.
Figure 4. Cascaded CT $\Sigma$Ms synthesized for VDSL: (a) 2-1-1-1; (b) 2-2-1; (c) 3-2.
• The 3-2 modulator shown in Fig. 4(c) includes a first stage which consists of an integrator and a resonator. This topology allows the same optimum pole positioning as in the 2-2-1 modulator with one less stage. However, stability problems might arise that compromise the modulator performance.

Table 1 shows the single-loop and inter-stage transfer functions \( F_{ij} \) for the different architectures in Fig. 4 as a function of the loop filter coefficients \( b_{ij} \). The expressions of \( CL_i \), obtained from (8) and (11), are also shown. It is important to note that \( b_{ij} \) are found from an iterative simulation-based process that optimizes the first stage of the modulator in order to maximize \( SNR \) while keeping stability.

The outcome of the optimization process – entirely done in the CT domain – is summarized in Table 2. This table includes the values of loop filter coefficients, \( k_i \) (implemented as transconductances) as well as the capacitances, \( C_i \), and resistances, \( R_i \) obtained from the optimization process.

The modulators in Fig. 4 were simulated using SIMSIDES. Fig. 5 shows the ideal output spectra of the modulators when clocked at \( f_s = 240 \) MHz. It can be observed the effect of the resonators poles distributed within the signal bandwidth. The impact on the in-band noise power is better appreciated in Fig. 6 that represents the Signal-to-(Noise+Distortion) Ratio (SNDR) vs input amplitude. Note that, although both the 2-2-1 and 3-2 architectures have the same location of the zeroes of the NTF, the 3-2 modulator achieves a worse resolution. This is due to the fact that the optimization process applied to that architecture was more conservative as a consequence of the stability constrains imposed by the 3rd-order stage.

In addition to the ideal performance described above, the effect of most critical limiting factors has been taken into account in the high-level design. Fig. 7 shows the SNR loss caused by clock jitter error. Note that the 2-1-1-1 architecture seems to be less sensitive to this error than the other architectures. However, it is important to note that the ideal SNR of this modulator is lower than the others. Therefore, there is a higher component of quantization noise masking the effect of clock jitter.

Two critical limiting factors in cascaded \( \Sigma \Delta \)Ms, and particularly in their CT implementation, are circuit tolerances and component mismatch. The first one can be controlled by using tuning of time constants or digital calibration. However, mismatch error still remains. In order to evaluate the impact of this error on the performance of the modulators in Fig. 4, maximum values of mismatch were estimated for a 0.13 \( \mu \)m CMOS technology considering a Gm-C implementation.

![Figure 5](image.png)

**Figure 5.** Ideal output spectra of the cascaded CT \( \Sigma \Delta \)Ms in Fig. 4: (a) 2-1-1-1, (b) 2-2-1, (c) 3-2.
### Table 1: Transfer functions and cancellation logic functions of the modulators in Fig.4

<table>
<thead>
<tr>
<th>Modulator</th>
<th>Transfer functions</th>
<th>Cancellation Logic</th>
</tr>
</thead>
<tbody>
<tr>
<td>2-1-1-1</td>
<td>$F_{14} = \frac{b_{10}}{s^2(s^2+\omega_p^2)}$</td>
<td>$CL_{1} = z^{-1}(n_{14}+n_{13}z^{-1}+n_{12}z^{-2}+n_{11}z^{-3}+n_{10}z^{-4})$</td>
</tr>
<tr>
<td></td>
<td>$F_{24} = -\frac{1}{T_s^3s^3}$</td>
<td>$CL_{2} = \frac{1}{6}z^{-1}(1+4z^{-1}+z^{-2})(1-2\cos(T_s\omega_p)z^{-1}+z^{-2})$</td>
</tr>
<tr>
<td></td>
<td>$F_{34} = -\frac{1}{T_s^2s^2}$</td>
<td>$CL_{3} = \frac{1}{2}z^{-1}(1+z^{-1})(1-z^{-1})(1-2\cos(T_s\omega_p)z^{-1}+z^{-2})$</td>
</tr>
<tr>
<td></td>
<td>$F_{44} = -\frac{1}{T_s}z$</td>
<td>$CL_{4} = (1-z^{-1})(1-2\cos(T_s\omega_p)z^{-1}+z^{-2})$</td>
</tr>
<tr>
<td>2-2-1</td>
<td>$F_{13} = \frac{b_{10}}{s(s^2+\omega_p^2)(s^2+\omega_{p2}^2)}$</td>
<td>$CL_{1} = z^{-1}(n_{14}+n_{13}z^{-1}+n_{12}z^{-2}+n_{11}z^{-3}+n_{10}z^{-4})$</td>
</tr>
<tr>
<td></td>
<td>$F_{23} = \frac{b_{20}}{s(s^2+\omega_{p2}^2)}$</td>
<td>$CL_{2} = z^{-1}(n_{22}+n_{21}z^{-1}+n_{20}z^{-2})(1-2\cos(T_s\omega_p)z^{-1}+z^{-2})$</td>
</tr>
<tr>
<td></td>
<td>$F_{44} = -\frac{1}{T_s}z$</td>
<td>$CL_{3} = (1-2\cos(T_s\omega_p)z^{-1}+z^{-2})(1-2\cos(T_s\omega_{p2})z^{-1}+z^{-2})$</td>
</tr>
<tr>
<td>3-2</td>
<td>$F_{12} = \frac{b_{11}+b_{10}}{s(s^2+\omega_p^2)(s^2+\omega_{p2}^2)}$</td>
<td>$CL_{1} = z^{-2}(n_{14}+n_{13}z^{-1}+n_{12}z^{-2}+n_{11}z^{-3}+n_{10}z^{-4})$</td>
</tr>
<tr>
<td></td>
<td>$F_{22} = \frac{b_{21}+b_{20}-T_{s}z}{s^2+\omega_{p2}^2}e^{-\frac{T_s}{2}}$</td>
<td>$CL_{2} = (1-2\cos(T_s\omega_p)z^{-1}+z^{-2})(1-z^{-1})$</td>
</tr>
</tbody>
</table>

#### Cancellation Logic Coefficients

<table>
<thead>
<tr>
<th>Modulator</th>
<th>Cancellation Logic Coefficients</th>
</tr>
</thead>
<tbody>
<tr>
<td>2-1-1-1</td>
<td>$10 = n_{14} = -\frac{b_{10}}{T_s^3\omega_p^3}\left[\sin(T_s\omega_p) - T_s\omega_p + \frac{1}{6}(T_s\omega_p)^3\right]$</td>
</tr>
<tr>
<td></td>
<td>$n_{11} = -\frac{b_{10}}{T_s^3\omega_p^3}\left[(T_s\omega_p)^2 - 2\cos(T_s\omega_p) - 4\sin(T_s\omega_p) + 2T_s\omega_p(\cos(T_s\omega_p) + 1)\right]$</td>
</tr>
<tr>
<td></td>
<td>$n_{12} = -\frac{b_{10}}{T_s^3\omega_p^3}\left[(T_s\omega_p)^3 - 4\cos(T_s\omega_p) + 6\sin(T_s\omega_p) - 2T_s\omega_p(1 + 2\cos(T_s\omega_p))\right]$</td>
</tr>
<tr>
<td>2-2-1</td>
<td>$10 = n_{14} = -\frac{b_{10}}{\omega_{p1}^3\omega_{p2}^3}\left[T_s(\omega_{p1}\omega_{p2}^3 - \omega_{p1}^3\omega_{p2}^3) + \omega_{p1}^3\sin(T_s\omega_{p1}) - \omega_{p2}^3\sin(T_s\omega_{p2})\right]$</td>
</tr>
<tr>
<td></td>
<td>$n_{11} = -\frac{b_{10}}{\omega_{p1}^3\omega_{p2}^3}\left[(T_s(\omega_{p2}^3\omega_{p1} - \omega_{p1}^3\omega_{p2}^3))(\cos(T_s\omega_{p1}) + \cos(T_s\omega_{p2}))\right] + \omega_{p2}^3\sin(T_s\omega_{p2})(1 + \cos(T_s\omega_{p2}))(1 + \cos(T_s\omega_{p2}))$</td>
</tr>
<tr>
<td></td>
<td>$n_{12} = -\frac{b_{10}}{\omega_{p1}^3\omega_{p2}^3}\left[-T_s(\omega_{p1}\omega_{p2}^3 - \omega_{p1}^3\omega_{p2}^3)(1 + 2\cos(T_s\omega_{p1})\cos(T_s\omega_{p2})) + \omega_{p1}^3\sin(T_s\omega_{p2})(1 + 2\cos(T_s\omega_{p1}))(1 + 2\cos(T_s\omega_{p2}))\right]$</td>
</tr>
<tr>
<td></td>
<td>$20 = n_{22} = -\frac{b_{20}}{\omega_{p2}^3}\left[T_s\omega_{p2}^3 - \sin(T_s\omega_{p2})\right]$</td>
</tr>
</tbody>
</table>
Table 1: Transfer functions and cancellation logic functions of the modulators in Fig.4.(Cont.)

<table>
<thead>
<tr>
<th>Mod.</th>
<th>Cancellation Logic Coefficients</th>
</tr>
</thead>
<tbody>
<tr>
<td>3-2</td>
<td>[-b_{10}(T_s \omega_{p1}\omega_{p2}(\omega_{p2}^2 - \omega_{p1}^2) + \omega_{p1}^3 \sin(T_s \omega_{p2}) - \omega_{p2}^3 \sin(T_s \omega_{p1})) + \frac{\omega_{p1}^3 \omega_{p2}^3(\omega_{p2}^2 - \omega_{p1})}{\omega_{p1}} \right] + \frac{b_{11}(1 - \cos(T_s \omega_{p2})) - \omega_{p2}^2(1 - \cos(T_s \omega_{p1}))}{\omega_{p1}^2 \omega_{p2}^2(\omega_{p2}^2 - \omega_{p1})} + \frac{b_{10}(T_s \omega_{p1}\omega_{p2}(\omega_{p1}^2 - \omega_{p2}^2)\cos(T_s \omega_{p1}) + \omega_{p2}^3 \sin(T_s \omega_{p2}) )\cos(T_s \omega_{p2}))}{\omega_{p1}^3 \omega_{p2}^3(\omega_{p1}^2 - \omega_{p2}^2)} + \frac{b_{10}(T_s \omega_{p1}\omega_{p2}(\omega_{p1}^2 - \omega_{p2}^2)\cos(T_s \omega_{p1}) + \omega_{p2}^3 \sin(T_s \omega_{p2}) )\cos(T_s \omega_{p2}))}{\omega_{p1}^3 \omega_{p2}^3(\omega_{p1}^2 - \omega_{p2}^2)}</td>
</tr>
<tr>
<td>11</td>
<td>[-2b_{10}(T_s \omega_{p1}\omega_{p2}(\omega_{p1}^2 - \omega_{p2}^2)\cos(T_s \omega_{p1}) + \omega_{p2}^3 \sin(T_s \omega_{p2}) )\cos(T_s \omega_{p2})) + \frac{b_{11}(1 - \cos(T_s \omega_{p2})) - \omega_{p2}^2(1 - \cos(T_s \omega_{p1}))}{\omega_{p1}^2 \omega_{p2}^2(\omega_{p2}^2 - \omega_{p1})} + \frac{b_{10}(T_s \omega_{p1}\omega_{p2}(\omega_{p1}^2 - \omega_{p2}^2)\cos(T_s \omega_{p1}) + \omega_{p2}^3 \sin(T_s \omega_{p2}) )\cos(T_s \omega_{p2}))}{\omega_{p1}^3 \omega_{p2}^3(\omega_{p1}^2 - \omega_{p2}^2)}</td>
</tr>
<tr>
<td>12</td>
<td>[-b_{10}(T_s \omega_{p1}\omega_{p2}(\omega_{p1}^2 - \omega_{p2}^2)\cos(T_s \omega_{p1}) + \omega_{p2}^3 \sin(T_s \omega_{p2}) )\cos(T_s \omega_{p2})) + \frac{b_{11}(1 - \cos(T_s \omega_{p2})) - \omega_{p2}^2(1 - \cos(T_s \omega_{p1}))}{\omega_{p1}^2 \omega_{p2}^2(\omega_{p2}^2 - \omega_{p1})} + \frac{b_{10}(T_s \omega_{p1}\omega_{p2}(\omega_{p1}^2 - \omega_{p2}^2)\cos(T_s \omega_{p1}) + \omega_{p2}^3 \sin(T_s \omega_{p2}) )\cos(T_s \omega_{p2}))}{\omega_{p1}^3 \omega_{p2}^3(\omega_{p1}^2 - \omega_{p2}^2)}</td>
</tr>
<tr>
<td>13</td>
<td>[-b_{10}(T_s \omega_{p1}\omega_{p2}(\omega_{p1}^2 - \omega_{p2}^2)\cos(T_s \omega_{p1}) + \omega_{p2}^3 \sin(T_s \omega_{p2}) )\cos(T_s \omega_{p2})) + \frac{b_{11}(1 - \cos(T_s \omega_{p2})) - \omega_{p2}^2(1 - \cos(T_s \omega_{p1}))}{\omega_{p1}^2 \omega_{p2}^2(\omega_{p2}^2 - \omega_{p1})} + \frac{b_{10}(T_s \omega_{p1}\omega_{p2}(\omega_{p1}^2 - \omega_{p2}^2)\cos(T_s \omega_{p1}) + \omega_{p2}^3 \sin(T_s \omega_{p2}) )\cos(T_s \omega_{p2}))}{\omega_{p1}^3 \omega_{p2}^3(\omega_{p1}^2 - \omega_{p2}^2)}</td>
</tr>
<tr>
<td>14</td>
<td>[-b_{10}(T_s \omega_{p1}\omega_{p2}(\omega_{p1}^2 - \omega_{p2}^2)\cos(T_s \omega_{p1}) + \omega_{p2}^3 \sin(T_s \omega_{p2}) )\cos(T_s \omega_{p2})) + \frac{b_{11}(1 - \cos(T_s \omega_{p2})) - \omega_{p2}^2(1 - \cos(T_s \omega_{p1}))}{\omega_{p1}^2 \omega_{p2}^2(\omega_{p2}^2 - \omega_{p1})} + \frac{b_{10}(T_s \omega_{p1}\omega_{p2}(\omega_{p1}^2 - \omega_{p2}^2)\cos(T_s \omega_{p1}) + \omega_{p2}^3 \sin(T_s \omega_{p2}) )\cos(T_s \omega_{p2}))}{\omega_{p1}^3 \omega_{p2}^3(\omega_{p1}^2 - \omega_{p2}^2)}</td>
</tr>
<tr>
<td>15</td>
<td>[-b_{11}(1 - \cos(T_s \omega_{p2})) - \omega_{p2}^2(1 - \cos(T_s \omega_{p1})) + \omega_{p2}^3 \sin(T_s \omega_{p2}) )\cos(T_s \omega_{p2})) + \frac{b_{11}(1 - \cos(T_s \omega_{p2})) - \omega_{p2}^2(1 - \cos(T_s \omega_{p1}))}{\omega_{p1}^2 \omega_{p2}^2(\omega_{p2}^2 - \omega_{p1})} + \frac{b_{10}(T_s \omega_{p1}\omega_{p2}(\omega_{p1}^2 - \omega_{p2}^2)\cos(T_s \omega_{p1}) + \omega_{p2}^3 \sin(T_s \omega_{p2}) )\cos(T_s \omega_{p2}))}{\omega_{p1}^3 \omega_{p2}^3(\omega_{p1}^2 - \omega_{p2}^2)}</td>
</tr>
<tr>
<td>20</td>
<td>[-b_{21}(T_s \omega_{p2}) - b_{20}(1 - \cos(T_s \omega_{p2})) + \omega_{p2}^3 \sin(T_s \omega_{p2}) )\cos(T_s \omega_{p2})) + \frac{b_{21}(T_s \omega_{p2}) - b_{20}(1 - \cos(T_s \omega_{p2}))}{\omega_{p2}^2} + \frac{b_{20}(1 - \cos(T_s \omega_{p2}))}{\omega_{p2}^2}</td>
</tr>
</tbody>
</table>

The results of this analysis are shown in Fig.8 where the SNR is represented as a function of the standard deviation of the transconductances ($\sigma_{gm}$) and capacitances ($\sigma_c$). For each point of these surfaces, a Monte Carlo analysis of 150 simulations was carried out. The value of the SNR represented in the vertical axis of Fig.8 is obtained by 90% of the simulations for each case of $\sigma_{gm}$ and $\sigma_c$. Note that even in the worst-case mismatch, the resolution is above the specified (72-db). Finally, the modulators in Fig.4 were high-level sized, i.e., the system-level specifications (12-bit/20-MHz) were mapped onto building-block specification using statistical optimization for design parameter selection, and behavioral simulation for evaluation. The results of this sizing process are summarized in Table 3 and Table 4 showing the maximum (minimum) values of the circuit error mechanisms that can be tolerated in order to fulfill the required modulator performance. As an illustration, Fig.9 shows the output spectra of the modulators taking into account the non-idealities listed in these tables. The effective resolution is $\approx 13.4$ bits and $\approx 13.2$ bits for the modulators in Fig.4(b) and (c), respectively.
Figure 6. SNDR vs. input amplitude (referred to reference voltage).

Table 2: Loop filter coefficients of the modulators in Fig.4

<table>
<thead>
<tr>
<th>2-1-1-1 Modulator</th>
<th>2-2-1 Modulator</th>
<th>3-2 Modulator</th>
</tr>
</thead>
<tbody>
<tr>
<td>$R_{in} = R_{fb} = 2 , k\Omega$; $R_r = 8.2 , k\Omega$</td>
<td>$R_{in1} = R_{fb1} = 2 , k\Omega$; $R_{r1} = 9 , k\Omega$</td>
<td>$R_{in1} = R_{fb1} = 2 , k\Omega$</td>
</tr>
<tr>
<td>$C_1 = 1.875 , \text{pF}$</td>
<td>$C_1 = 1.875 , \text{pF}$</td>
<td>$C_1 = 10 , \text{pF}$</td>
</tr>
<tr>
<td>$k_{g1} = 150 , \mu\text{S}$</td>
<td>$k_{g1} = 166 , \mu\text{S}$</td>
<td>$k_{g1} = 312 , \mu\text{S}$</td>
</tr>
<tr>
<td>$k_{g3...5} = 20 , \mu\text{S}$</td>
<td>$k_{g2} = 30 , \mu\text{S}$</td>
<td>$k_{g2} = 130 , \mu\text{S}$</td>
</tr>
<tr>
<td>$k_{f1} = 60 , \mu\text{S}$</td>
<td>$k_{g3} = 200 , \mu\text{S}$</td>
<td>$k_{g4} = 26 , \mu\text{S}$</td>
</tr>
<tr>
<td>$k_{in2...4} = k_{fb2...4} = 180 , \mu\text{S}$</td>
<td>$k_{g5} = 20 , \mu\text{S}$</td>
<td>$k_{g3} = 104 , \mu\text{S}$</td>
</tr>
<tr>
<td>$k_{f2} = 260 , \mu\text{S}$</td>
<td>$k_{r2} = 13 , \mu\text{S}$</td>
<td>$k_{f2} = 208 , \mu\text{S}$</td>
</tr>
<tr>
<td>$k_{ff1} = 63 , \mu\text{S}$</td>
<td>$k_{g4} = 46 , \mu\text{S}$</td>
<td>$k_{f3} = 78 , \mu\text{S}$</td>
</tr>
<tr>
<td>$k_{in2} = k_{fb2} = 100 , \mu\text{S}$</td>
<td>$k_{f2} = 46 , \mu\text{S}$</td>
<td>$k_{f4} = 130 , \mu\text{S}$</td>
</tr>
<tr>
<td>$k_{in3} = k_{fb3} = 180 , \mu\text{S}$</td>
<td>$k_{r3} = 26 , \mu\text{S}$</td>
<td>$k_{r2} = 26 , \mu\text{S}$</td>
</tr>
</tbody>
</table>

Table 3: High-level sizing of Fig.4(b)

| Front-end opamp | 
|------------------|------------------|
| Gain            | $>600 \, \text{MHz}$ |
| DC Gain         | $>70 \, \text{dB}$ |
| Phase Margin    | 60°              |
| Parasitic Input Capacitance | $<0.2 \, \text{pF}$ |
| Parasitic Output Capacitance | $<0.2 \, \text{pF}$ |
| Diff. Output Swing | $>0.5 \, \text{V}$ |
| Transconductors |                  |
| DC Gain         | $>50 \, \text{dB}$ |
| Diff. Input Amplitude | 0.3 \, \text{V} |
| Diff. Output Amplitude | 0.3 \, \text{V} |
| Third-order non-linearity | $>56 \, \text{dBV}$ |

Table 4: High-level sizing of Fig.4(c)

| Front-end opamp | 
|------------------|------------------|
| Gain            | $>600 \, \text{MHz}$ |
| DC Gain         | $>60 \, \text{dB}$ |
| Phase Margin    | 60°              |
| Parasitic Input Capacitance | $<0.2 \, \text{pF}$ |
| Parasitic Output Capacitance | $<0.2 \, \text{pF}$ |
| Diff. Output Swing | $>0.5 \, \text{V}$ |
| Transconductors |                  |
| DC Gain         | $>60 \, \text{dB}$ |
| Diff. Input Amplitude | 0.4 \, \text{V} |
| Diff. Output Amplitude | 0.4 \, \text{V} |
| Third-order non-linearity | $>53 \, \text{dBV}$ |
Figure 7. SNR loss due to clock jitter.

Figure 8. SNR loss vs. mismatch for: (a) 2-2-1 CT ΣΔM. (b) 3-2 CT ΣΔM.

Figure 9. Output Spectra for: (a) 2-2-1 CT ΣΔM. (b) 3-2 CT ΣΔM.
5. CONCLUSIONS

In this paper a new methodology of synthesizing cascaded continuous-time $\Sigma\Delta$ modulators has been presented. It has been demonstrated that more efficient topologies in terms of circuit complexity can be generated if the design is directly done in the continuous-time domain and the cancellation logic is taken into account in the synthesis procedure. In order to illustrate the method, several cascaded architectures have been synthesized and designed to achieve VDSL system requirements: 12-bit@20MHz. Behavioral time-domain simulations considering their most critical limiting factors show that these architectures are good candidates for in-coming broadband telecommunication systems.

ACKNOWLEDGMENTS

This work has been supported by the Spanish Ministry of Science and Education (with support from European Regional Development Fund) under contract TEC2004-01752/MIC.

REFERENCES

Design of a 1.2-V 130nm CMOS 13-bit@40MS/s Cascade 2-2-1 Continuous-Time ΣΔ Modulator

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Abstract—This paper presents the design of a continuous-time multibit cascade 2-2-1 ΣΔ modulator for broadband telecom systems. The modulator architecture has been synthesized directly in the continuous-time domain instead of using a discrete-to-continuous time transformation. This method results in a more efficient modulator in terms of noise shaping, power consumption and sensitivity to circuit element tolerances. The design of the circuit, realized in a 130nm CMOS technology, is based upon a top-down CAD methodology which combines simulation and statistical optimization at different levels of the modulator hierarchy. The estimated power consumption is 60mW from a 1.2-V supply voltage when clocked at 240MHz. Simulation results show 80-dB effective resolution within a 20-MHz signal bandwidth.†

I. INTRODUCTION

Modern broadband telecommunication applications, like Very high-rate Digital Subscriber Line (VDSL) and Power Line Communication (PLC), demand Analog-to-Digital Converters (ADCs) targeting 12-14bit resolution at conversion rates of 40-80 MSamples/second (MS/s). Traditionally, these specifications have been achieved with Nyquist-rate ADCs, using pipeline or folding/interpolation topologies, because of the prohibitive sampling frequencies required by ΣΔ Modulators (ΣΔMs) [1]. However, in the last few years, the use of Continuous-Time (CT) instead of Discrete-Time (DT) circuit techniques are making possible for ΣΔMs to digitize (1-15 MHz) signals with 11-14 bit resolution [2]-[4].

In spite of achieving potentially faster operation with lower power consumption, CT ΣΔMs are more sensitive than DT ΣΔMs to some circuit errors, namely: clock jitter and technology parameter variations [5]. The latter are specially critical for the realization of cascade architectures what explains the very few Integrated Circuits (ICs) reported up to now [4].

Recent studies demonstrate that more efficient cascade CT ΣΔMs can be synthesized by using a direct synthesis method [6]. This method allows to reduce the number of analog components and to efficiently place the zeroes/poles of the noise transfer function, thus yielding to more robust architectures than using a DT-to-CT transformation [7].

This paper reports the design and electrical implementation of a cascade CT ΣΔM. The modulator architecture comprises three stages. The first two stages are a second-order topology whereas the last stage uses a first-order loop filter. All stages include 4-bit internal quantization and Non-Return-to-Zero (NRZ) Digital-to-Analog Converter (DAC) in order to attenuate the clock jitter [8]. The modulator has been synthesized directly in the continuous-time domain and no calibration is used to compensate for mismatch and element tolerances. Circuit design, realized in a 0.13μm CMOS technology and nominal 1.2-V supply voltage, has been optimized from system-level to building-block level in order to achieve the required specifications with minimum power dissipation. Simulation results demonstrate that the presented circuit can digitize 20-MHz signals with 13-bit resolution when clocking at 240MHz.

II. DESIGN CONSIDERATIONS

The modulator in this paper was designed to cope with an effective resolution over 12bit within a 20-MHz signal bandwidth. Ideally, these specifications can be achieved by different combinations of modulator order, \( L \), number of bits of the internal quantizer(s), \( B \), and oversampling ratio, \( M \). However, in practice, there are some important limiting factors precluding from using some \( \{ L, B, M \} \) triads. These limitations impose the following design constraints:

- High-order single-loop topologies may not be feasible for the mentioned specifications because of stability issues. For that reason, only cascade architectures made up of second-order and first-order stages were considered.
- High values of \( B \) force to use linearization techniques [3] or digital calibration [2] in order to control the nonlinearity of the DAC used in the modulator feedback loop.

†. This work has been supported by the Spanish Ministry of Science and Education (with support from the European Regional Development Fund) under contract TEC2004-01752/MIC.
• Large values of $M$ lead to infeasible sampling frequencies in terms of power consumption.

• Last but not least, clock jitter is an ultimate limiting error that has to be addressed from the very beginning of the design process. In fact, as demonstrated in [8], the in-band noise power caused by jitter error can be minimized by proper selection of $B$, the sampling frequency, $f_s$ and the modulator loop filter.

Taking into account the considerations mentioned above, an exhaustive exploration of different $\Sigma\Delta M$ loop filters was done using SIMSDES [9] in order to find out the optimum $\{L, B, M\}$ trade in terms of power consumption, distribution of the Noise Transfer Function (NTF) zeroes and insensitivity to clock jitter. As a result, the fifth-order ($L = 5$) cascade $\Sigma\Delta M$, conceptually shown in Fig.1, was selected. It consists of a 2-2-1 topology, clocked at $f_s = 240\text{MHz}$ ($M = 6$), with $B = 4$ and NRZ DAC in all stages in order to minimize the effect of jitter, that according to [8], must be below 3ps rms.

The modulator in Fig.1 can be synthesized from an equivalent DT $\Sigma\Delta M$. However, in order to get a functional CT $\Sigma\Delta M$ while keeping the Cancellation Logic (CL) of the original DT $\Sigma\Delta M$, every state variable and DAC output must be connected to every integrator input of later stages [7]. The number of integrating paths, and hence of analog components, can be reduced if the whole cascaded $\Sigma\Delta M$ is directly synthesized in the CT domain as proposed in [6]. In this paper we have selected the latter methodology, which does not only take into account the single-stage loop filter transfer functions ($F_{ij}$), but also the inter-stage loop filter transfer functions ($F_{ij}, i \neq j$). The latter, defined as the transfer function from $y_i$ to the $j$-th quantizer (see Fig.1), are continuous-time integrating paths appearing only when the modulator stages are connected to form the cascaded $\Sigma\Delta M$ and must be included in the synthesis methodology to obtain a functional modulator with minimum number of inter-stage paths.

For the modulator in this paper, the $F_{ij}$ shown in (1) were synthesized, where $T_s = 1/f_s$ is the sampling period and $\omega_{p1,2}$ are the pole frequencies. Coefficients $b_{ij}$ in (1) are found through an iterative simulation-based process that – starting from nominal values required to place the zeroes of the corresponding NTF – optimizes the modulator performance in terms of dynamic range and stability. For this purpose, these coefficients are varied in a range of up to $\pm 20\%$ around their nominal values in order to achieve the maximum Signal-to-Noise Ratio (SNR) while keeping stability. The partial CL transfer functions can be calculated from (1), giving the expressions shown in (2), where coefficients $n_{ij}$ are shown in (3) [6].

III. MODULATOR IMPLEMENTATION

Fig.2 shows the conceptual circuit implementation of the modulator\footnote{Although the modulator has been implemented using fully-differential circuitry, a single-ended schematic is shown here for the sake of simplicity.}. An RC-active front-end integrator is chosen for its better linearity whereas the rest of integrators are Gm-C [2][3]. The 4-bit quantizers were implemented using a flash ADC made up of a resistive ladder and 15 regenerative comparators. DACs were implemented by current-steering topologies. An extra feedback branch between the output and the input to the quantizer (DAC2 in Fig.2) and two D-latches are employed in the first two stages in order to compensate for the effect of excess loop delay [2]. The first two stages are formed by a resonator which has its poles placed at an optimum position, minimizing NTF in the signal bandwidth, $B_w$ [10]. Resistor variations can be tuned out using a combination of a discrete rough tun-

![Fig. 1: Conceptual diagram of the 2-2-1 modulator.](image_url)

![Fig. 2: Modulator implementation.](image_url)
\begin{equation}
F_{11}(s) = \frac{b_{11}s + b_{10}}{(s^2 + \omega_{p1}^2)}; F_{22}(s) = \frac{b_{21}s + b_{20}}{(s^2 + \omega_{p2}^2)}; F_{33}(s) = \frac{b_{30}}{s}
\end{equation}

\begin{equation}
F_{13}(s) = \frac{b_{10}b_{20}b_{30}}{s(s^2 + \omega_{p1}^2)(s^2 + \omega_{p2}^2)}; F_{23}(s) = \frac{b_{20}b_{30}}{s(s^2 + \omega_{p2}^2)}
\end{equation}

\begin{equation}
CL_1 = z^{-1}(n_{14} + n_{13}z^{-1} + n_{12}z^{-2} + n_{11}z^{-3} + n_{10}z^{-4})
\end{equation}

\begin{equation}
CL_2 = z^{-1}(n_{22} + n_{21}z^{-1} + n_{20}z^{-2}) \cdot (1 - 2\cos(T_s\omega_{p1})z^{-1} + z^{-2})
\end{equation}

\begin{equation}
n_{10} = n_{14} = \frac{-b_{10}b_{20}b_{30}}{\omega_{p1}^3(\omega_{p2}^2 - \omega_{p1}^2)} \cdot [T_s(\omega_{p1}^3\omega_{p2}^3 - \omega_{p1}^3\omega_{p2}^2 + \omega_{p1}^3 \sin(T_s\omega_{p2}) - \omega_{p2}^3 \sin(T_s\omega_{p1})]]
\end{equation}

\begin{equation}
n_{11} = n_{13} = \frac{-2b_{10}b_{20}b_{30}}{\omega_{p1}^3\omega_{p2}^3(\omega_{p2}^2 - \omega_{p1}^2)} \cdot [(T_s(\omega_{p1}^3\omega_{p2}^3 - \omega_{p1}^3\omega_{p2}^2)(\cos(T_s\omega_{p1}) + \cos(T_s\omega_{p2}))) + \\
+ \omega_{p2}^3 \sin(T_s\omega_{p1})(1 + \cos(T_s\omega_{p2}))) - \omega_{p1}^3 \sin(T_s\omega_{p2})(1 + \cos(T_s\omega_{p1})))]
\end{equation}

\begin{equation}
n_{12} = \frac{-2b_{10}b_{20}b_{30}}{\omega_{p1}^3\omega_{p2}^3(\omega_{p2}^2 - \omega_{p1}^2)} \cdot [T_s(\omega_{p1}^3\omega_{p2}^3 - \omega_{p1}^3\omega_{p2}^2)(1 + 2\cos(T_s\omega_{p1}) \cos(T_s\omega_{p2}))) + \\
+ \omega_{p1}^3 \sin(T_s\omega_{p2})(1 + 2\cos(T_s\omega_{p1}) - \omega_{p2}^3 \sin(T_s\omega_{p1})(1 + 2\cos(T_s\omega_{p2})))]
\end{equation}

\begin{equation}
n_{20} = n_{22} = \frac{-b_{20}b_{30}}{\omega_{p2}^3}[T_s(\omega_{p2}^3 - \sin(T_s\omega_{p2})]
\end{equation}

\begin{equation}
n_{21} = \frac{-2b_{20}b_{30}}{\omega_{p2}^3} \cdot [\sin(T_s\omega_{p2}) - T_s\omega_{p2} \cos(T_s\omega_{p2})]
\end{equation}

The loop filter coefficients, $k_j$ (implemented as transconductances) as well as the capacitances, $C_j$, and resistances, $R_j$, used in the modulator.

The modulator was high-level sized, i.e., the system-level specifications (12-bit@20-MHz) were mapped onto building-block specifications using statistical optimization for design parameter selection and behavioral simulation for evaluation [9]. The result of this sizing process is summarized in Table 2, showing the maximum (minimum) values of the circuit error mechanisms that can be tolerated in order to fulfil the

Table 1: Loop filter coefficients of the ΣΔM

<table>
<thead>
<tr>
<th>$R_{in}$</th>
<th>$R_{fb}$</th>
<th>$1$ kΩ</th>
<th>$R_{r1}$</th>
<th>$5$ kΩ</th>
</tr>
</thead>
<tbody>
<tr>
<td>$C_1$</td>
<td>$C_3$</td>
<td>$6$ pF</td>
<td></td>
<td></td>
</tr>
<tr>
<td>$C_2$</td>
<td>$2.25$ pF</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>$C_4$</td>
<td>$C_5$</td>
<td>$0.75$ pF</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

| $k_{g1}$ | $500$ µA/V |
| $k_{in2}$ | $800$ µA/V |
| $k_{g5}$ | $k_{ff1}$ | $k_{ff3}$ | $200$ µA/V |
| $k_{g2}$ | $k_{g4}$ | $k_{r2}$ | $k_{ff2}$ | $100$ µA/V |
| $k_{ff0}$ | $158$ µA/V |

Table 2: High-level sizing of the ΣΔM

<table>
<thead>
<tr>
<th>Front-end opamp</th>
<th>$&gt;580$ MHz</th>
</tr>
</thead>
<tbody>
<tr>
<td>DC Gain</td>
<td>$&gt;68$ dB</td>
</tr>
<tr>
<td>Phase Margin</td>
<td>$&gt;60^\circ$</td>
</tr>
<tr>
<td>Parasitic Input Capacitance</td>
<td>$&lt;0.4$ pF</td>
</tr>
<tr>
<td>Parasitic Output Capacitance</td>
<td>$&lt;0.5$ pF</td>
</tr>
<tr>
<td>Diff. Output Swing</td>
<td>$&gt;0.3$ V</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Transconductors</th>
<th>$\geq 50$ dB</th>
</tr>
</thead>
<tbody>
<tr>
<td>Diff. Input Amplitude</td>
<td>$0.3$ V</td>
</tr>
<tr>
<td>Diff. Output Amplitude</td>
<td>$0.3$ V</td>
</tr>
<tr>
<td>Third-order non-linearity</td>
<td>$&gt;56$ dBV</td>
</tr>
</tbody>
</table>
required modulator performance. The data in Table 2 are the starting point of the electrical design described in next section.

IV. DESIGN OF THE MAIN BUILDING BLOCKS

The modulator has been designed in a 130nm 1-poly 8-metal logic CMOS process. Metal-insulator-metal capacitors were used because of their good matching and linearity properties. The estimated power dissipation is 60mW from a single 1.2-V supply voltage. The ΣΔM building blocks were conveniently selected and sized according to the system-level specifications. Among the others, the most critical subcircuits are the opamps and the transconductors, described below.

A. Front-end operational amplifier

Fig.3 shows the schematic of the front-end operational amplifier together with its common-mode feedback circuit. It is a fully differential telescopic cascode topology with gain boosting. Note that p-type input scheme has been considered in order to cancel the body effect in PMOS devices – one of the mechanisms for substrate noise coupling. One of the major limitations of this topology is the output swing. However, this is not a problem in this modulator where proper system-level design reduces the front-end integrator output signal range to 0.3V. Table 3 sums up the simulated transistor-level performance of the circuit.

![Fig. 3: Front-end operational amplifier. (a) Core. (b) CMFB circuit.](image)

B. Transconductors

One of the main limitations in open-loop Gm-C integrators is their poor linearity. In order to tackle this problem, the transconductor shown in Fig.4, based on a quadratic term cancellation, is proposed. High-speed operation is achieved by using only feed-forward paths and by adding capacitors ($C_{pf}$) which introduces a high frequency zero that extends the frequency range of operation. This transconductor can be turned through the bias current, $I_{bias}$. In order for the tuning to be effective, each transconductance in the modulator is formed by a parallel connection of unitary transconductors of 100μA/V each. Multiple MonteCarlo simulations have been done during the design process in order to take into account the impact of mismatch on the linearity of this circuit. Table 4 shows a summary of the electrical performance.

![Fig. 4: Transconductor schematic.](image)

<table>
<thead>
<tr>
<th>GB</th>
<th>600 MHz</th>
</tr>
</thead>
<tbody>
<tr>
<td>DC Gain</td>
<td>71 dB</td>
</tr>
<tr>
<td>Phase Margin</td>
<td>80°</td>
</tr>
<tr>
<td>Parasitic input capacitance</td>
<td>0.36 pF</td>
</tr>
<tr>
<td>Parasitic output capacitance</td>
<td>0.4 pF</td>
</tr>
<tr>
<td>Differential output swing</td>
<td>0.7 V</td>
</tr>
<tr>
<td>Power consumption</td>
<td>20mW</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Table 3: Transistor-level performance of the front-end opamp</th>
</tr>
</thead>
<tbody>
<tr>
<td>DC Gain</td>
</tr>
<tr>
<td>Diff. Input Amplitude</td>
</tr>
<tr>
<td>Diff. Output Amplitude</td>
</tr>
<tr>
<td>HD3</td>
</tr>
<tr>
<td>Transconductance standard deviation, $\sigma_{g_m}/g_m$</td>
</tr>
<tr>
<td>Power consumption</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Table 4: Transistor-level performance of transconductors</th>
</tr>
</thead>
</table>

Tesis Doctoral. Ramón Tortosa Navas 184
V. SIMULATION RESULTS

The modulator was simulated considering the electrical performance described above. As an illustration, Fig. 5 shows the output spectrum for an input sine-wave of -6.5-dBV amplitude and 1.76-MHz frequency. The maximum Signal-to-(Noise+Distortion) Ratio (SNDR) is 80 dB (≈ 13 bits).

In addition to the design issues discussed in previous sections, the effect of circuit tolerances and component mismatch, especially critical in cascade CT ΣΔMs, has been taken into account. The first one can be controlled in this circuit by using tuning of time constants. However, mismatch error still remains. In order to evaluate the impact of this error on the performance of the modulator, maximum values of mismatch were estimated for a 130nm CMOS technology. The results of this analysis are shown in Fig. 6 where the SNR is represented as a function of the standard deviation of the transconductances (σ_{gm}) and capacitances (σ_{C}). For each point of these surfaces, a Monte Carlo analysis of 150 simulations was carried out. The value of the SNR represented in the vertical axis of Fig. 6 is obtained by 90% of the simulations for each case of σ_{gm} and σ_{C}. Note that even in the worst-case mismatch, the resolution is above the specified (74-dB).

CONCLUSIONS

The design of a 1.2-V, 130nm CMOS 13-bit@20-MHz cascade CT-ΣΔM has been presented. The modulator architecture has been directly synthesized in the continuous-time domain, thus optimizing their performance in terms of circuit complexity, power consumption and sensitivity with respect to mismatch.

REFERENCES

Volume 6589: Smart Sensors, Actuators, and MEMS III

PLENARY SESSION
POWER GENERATION AND LOW-POWER ARCHITECTURES
OPTICAL MEMS
MICROFLUIDIC SYSTEMS
AEROSPACE APPLICATIONS
PHYSICAL SENSORS
SMART SYSTEM INTEGRATION
FABRICATION AND PROCESS TECHNOLOGY
RF MEMS
CHEMICAL AND BIO-SENSORS
BIO-MEMS AND ACTUATORS
MATERIALS AND SIMULATION

Volume 6590: VLSI Circuits and Systems III

DIGITAL DESIGN METHODOLOGIES AND TOOLS
MULTIMEDIA I
ANALOG CIRCUITS I
FPGAS
CAD
ANALOG AND MIXED-SIGNAL DESIGN METHODOLOGIES AND TOOLS
MULTIMEDIA II
DATA COMMUNICATION
ANALOG CIRCUITS II
CIRCUIT DESIGN FOR RF APPLICATIONS
HIGH LEVEL MODELLING AND VLSI ARITHMETIC
SYSTEMS AND NETWORK ON A CHIP
TECHNOLOGY

Volume 6591: Nanotechnology III

PLENARY PRESENTATION
NANOFABRICATION I
NANOFABRICATION II
Development of automated microrobot-based nanohandling stations for nanocharacterization [6589-54]
S. Fatikow, V. Eichhorn, F. Krohs, I. Mircea, C. Stolle, S. Hagemann

Identification of wine defects by means of a miniaturized electronic tongue [6589-56]

MATERIALS AND SIMULATION

On the influence of nano-sized palladium clusters at the surface of SnO₂ thin films on the gas response [6589-38]
S. Palzer, E. Moreton, C. Yin, B. von Issendorf, J. Wöllenstein

Three-dimensional simulation of sacrificial etching [6589-40]
J. Cervenka, H. Ceric, S. Selberherr

Application of PZT thick-films on adjusting purposes in micro-optical systems [6589-41]
C. Bruchmann, B. Höfer, P. Schreiber, R. Eberhardt, W. Buss, T. Peschel, S. Gebhardt, A. Tünnermann, E. Beckert

VHDL implementation of a communication interface for integrated MEMS [6589-47]
E. Magdaleno Castelló, M. Rodríguez Valido, A. Ayala Alfonso

Modelling and simulation of a micromachined angular rate sensor with optimised mechanical suspension [6589-48]

Physical modeling of a highly sensitive linear MOS sensor for 2D detection of magnetic fields [6589-53]
A. Abou-Elnour, O. Abo-Elnor, E. Mohamed, M. Ibrahim

Coupling coefficient determination based on simulation and experiment for ST-cut quartz saw delay-line response [6589-61]
Y.-C. Hsu, N.-B. Le, L.-S. Jang

A domotic application for educational tasks [6589-63]
S. Alayón, C. González, Y. Vargas, L. Hernández

Volume 6590: VLSI Circuits and Systems III

Editors: Valentin de Armas Sosa, Kamran Eshraghian, Félix B. Tobajas

Conference Committee

Introduction
Plenary Paper 6589-200
Plenary Paper 6591-201

DIGITAL DESIGN METHODOLOGIES AND TOOLS

High-level power estimation for digital system [6590-1]
Y. Durrani, A. Abril, T. Riesgo

Crosscoupling power optimal wire spacing in quasilinear runtime [6590-22]
P. Zuber, T. Ilseher, W. Stechele

Partitioning and characterization of high speed adder structures in deep-submicron technologies [6590-2]
A. Estrada, G. Sassaw, C. Jiménez, M. Valencia

Power-driven FPGA to ASIC conversion [6590-4]
W. Fang, L. Spaanenburg

Automatic logic synthesis for parallel alternating latches clocking schemes [6590-60]
D. Guerrero, M. Bellido, J. Juan, A. Millan, P. Ruiz, E. Ostua, J. Viejo
Effects of buffer insertion on the average/peak power ratio in CMOS VLSI digital circuits [6590-61]
A. Acosta, J. Mora, J. Castro, P. Parra

HEAPAN: a high-level computer architecture analysis tool [6590-65]
D. Peñalosa, C. Jiménez, M. Valencia

MULTIMEDIA I

MPEG-4 ASP SoC receiver with novel image enhancement techniques for DAB networks [6590-25]
D. Barreto, A. Quintana, L. García, G. Callicó, A. Núñez

Toward the implementation of a baseline H.264/AVC decoder onto a reconfigurable architecture [6590-6]
S. López, A. Kanstein, J. López, M. Berekovic, R. Sarmiento, J. Mignelet

Accelerating a MPEG-4 video decoder through custom software/hardware co-design [6590-7]
J. Díaz, D. Barreto, L. García, G. Marrero, P. Carballo, A. Núñez

Optimizing coarse-grain reconfigurable hardware utilization through multiprocessing: an H.264/AVC decoder example [6590-8]
A. Kanstein, S. López Suárez, B. De Sutter

ANALOG CIRCUITS I

Low-voltage low-power reference circuits for an autonomous robot: I-SWARM [6590-9]
J. Colomer, A. Saiz-Vela, P. Míribel-Català, M. Puig-Vidal, J. Samitier

Low-voltage CMOS variable preamplifier for fiber-based gigabit ethernet [6590-10]
J. García del Pozo, S. Celma, C. Aldea, J. Alegre, D. Digón

Design of clock recovery circuits for optical clocking in DSM CMOS [6590-11]
C. Thangaraj, K. Stephenson, T. Chen, K. Lear, A. Raza

A study of mismatch in adaptive programmable CMOS sensor compensation circuits [6590-12]
G. Zatorre, N. Medrano, M. Sanz, P. Martínez, S. Celma, J. García-del-Pozo

Ultra low power switched current finite impulse response filter banks realized in CMOS 0.18 µm technology [6590-49]
R. Dlugosz

IP-based design reuse for analog systems [6590-52]
T. Levi, J. Tomas, N. Lewis, P. Fouillat

A fully integrated folded mixer in CMOS 0.35 µm technology for 802.11a WIFI applications [6590-56]
J. del Pino, R. Díaz, M. Añon, F. Cabrera, A. Iturri, S. Khemchandani

Flexible and low power binary-tree current mode min/max nonlinear filters realized in CMOS technology [6590-64]
R. Dlugosz, T. Talaška

FPGAS

Architectural design for a low cost FPGA-based traffic signal detection system in vehicles [6590-13]
I. López, R. Salvador, J. Alarcón, F. Moreno

Hand veins feature extraction using DT-CNNS [6590-14]
S. Malki, L. Spaanenburg

Real-time lane detector hardware system [6590-15]
P. Cobos Arribas, F. Jiménez Alonso

FPGA realization of a split radix FFT processor [6590-55]
J. García, J. Michell, G. Ruiz, A. Burón
CAD

**Exploring system interconnection architectures with VIPACES: from direct connections to NoCs [6590-18]**
A. Sánchez-Peña, P. Carballo, A. Núñez

**Automatic synthesis of zero-aliasing space compactors with application to testing of embedded IP cores [6590-19]**
J. Solana, J. Frechoso

ANALOG AND MIXED-SIGNAL DESIGN METHODOLOGIES AND TOOLS

**Design automation techniques for high-resolution current folding and interpolating CMOS A/D converters [6590-20]**
D. Gevaert

**Toward systematic design of multi-standard converters [6590-21]**
V. Rivas, R. Castro-López, A. Morgado, O. Guerra, E. Roca, R. del Río, J. de la Rosa, F. Fernández

**A methodology for switching noise estimation at gate level [6590-23]**
J. Castro, P. Parra, A. Acosta

**Synchronous and asynchronous multiplexer circuits for medical imaging realized in CMOS 0.18um technology [6590-50]**
R. Długosz, K. Iniewski

**Resizing methodology for CMOS analog circuits [6590-51]**
T. Levi, J. Tomas, N. Lewis, P. Fouillat

MULTIMEDIA II

**Low-cost VLSI architecture design for forward quantization of H.264/AVC [6590-5]**
G. Ruiz, J. Michell

**Multiformat decoder for a DSP-based IP set-top box [6590-24]**
F. Pescador, M. Garrido, C. Sanz, E. Juárez, D. Samper, R. Antoniello

**High parallel-pipeline integer-pel and fractional-pel motion estimation VLSI architectures for H.264/AVC [6590-26]**
A. Mora-Campos, F. Ballester-Merelo, M. Martínez-Péiró, J. Canals-Esteve

**H.264 video stream statistical analysis for post-compression improvements [6590-27]**
J. Pérez Casanova, F. Ballester Merelo, M. Martínez Peiró, J. Canals Esteve

DATA COMMUNICATION

**Variable length packet scheduler algorithm with QoS support [6590-28]**
R. Arteaga, F. Tobajas, R. Esper-Chain, M. Monzón, R. Regidor, V. De Armas, R. Sarmiento

**Integrated hardware interfaces for modular sensor networks [6590-30]**
J. Portilla, A. de Castro, A. Abril, T. Riesgo

ANALOG CIRCUITS II

**Design of a 0.13-μm CMOS cascade expandable ΣΔ modulator for multi-standard RF telecom systems [6590-31]**
A. Morgado, R. del Río, J. de la Rosa

**A design tool for high-resolution high-frequency cascade continuous-time ΣΔ modulators [6590-32]**
R. Tortosa, R. Castro-López, J. de la Rosa, A. Rodríguez-Vázquez, F. Fernández

**A highly linear fast-settling envelope detector [6590-33]**
J. Alegre, S. Celma, J. García del Pozo, P. Martínez
A design tool for high-resolution high-frequency cascade continuous-time $\Sigma\Delta$ modulators

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ABSTRACT

This paper introduces a CAD methodology to assist the designer in the implementation of continuous-time (CT) cascade $\Sigma\Delta$ modulators. The salient features of this methodology are: (a) flexible behavioral modeling for optimum accuracy-efficiency trade-offs at different stages of the top-down synthesis process; (b) direct synthesis in the continuous-time domain for minimum circuit complexity and sensitivity; and (c) mixed knowledge-based and optimization-based architectural exploration and specification transmission for enhanced circuit performance. The applicability of this methodology will be illustrated via the design of a 12 bit 20 MHz CT $\Sigma\Delta$ modulator in a 1.2V 130nm CMOS technology.

Keywords: Continuous-time $\Sigma\Delta$ modulators, high-resolution high-frequency data converters, design automation, CAD

1. INTRODUCTION

The ever shrinking minimum feature size of CMOS technologies has triggered a revolution in integrated designs, from application-specific integrated circuits (ASICs) to entire systems on a single chip (SoCs). Notwithstanding, a critical design productivity lag has been reported [1]: with a productivity growth rate of 21%, compared to a 58% complexity growth rate, design cost is increasing rapidly. Taking into account the ever demanding time-to-market pressures, this picture is clearly worrisome. For analog and/or mixed-signal (AMS) design the situation is even worse because of many different reasons, the most significant being the lack of commercial CAD tools and methodologies to efficiently support the analog design. The design methodologies and tools in this paper try to reduce this design gap for a class of circuits: Continuous-Time (CT) cascade $\Sigma\Delta$ modulators (conceptually shown in Fig.1), although some of the techniques and tools presented are applicable to other classes. The selection of this circuit class has been driven by the demands of new generations of high-speed wireless/wireline communication terminals, which require broadband Analog-to-Digital Converters (ADCs) capable of digitizing 20-MHz wideband signals with effective resolutions over 12 bits and with minimum power consumption. Although most reported $\Sigma\Delta$ modulators have been implemented using Discrete-Time (DT) circuits, the increasing demand for broadband data communication systems has motivated the use of CT techniques. In addition to showing an intrinsic antialiasing filtering, CT $\Sigma\Delta$ modulators provide potentially faster operation with lower power consumption than their DT counterparts [2],[3].

In spite of their mentioned advantages, CT $\Sigma\Delta$ modulators are more sensitive than DT ones to some circuit errors, namely: clock jitter, excess loop delay and technology parameter variations [2]. The latter are specially critical for the realization of cascaded architectures. This explains the use of single-loop topologies in most reported silicon prototypes [4][5], whereas very few experimental results of cascaded CT $\Sigma\Delta$ modulators have been reported [6]. Although single-loop CT topologies have potentially a smaller sensitivity to technological process variations than cascade CT topologies, the possibility to avoid stability problems in the latter make them specially appealing for high-resolution high signal bandwidth operation.

This paper introduces a CAD methodology to assist the designer in the implementation of continuous-time cascade sigma-delta modulators. The main components of this systematic methodology, introduced in Section 2, are:

a) Performance modeling of dominant error sources at modulator level (Section 3).

b) Efficient behavioral simulator with variable levels of modeling accuracy for architectural synthesis, specification transmission and hierarchical verification (Section 3).
2. SYSTEMATIC SYNTHESIS METHODOLOGY

Synthesis of high-speed continuous-time \( \Sigma \Delta \) modulators is a complex task which requires systematic design methods and customized tools. The objective of the synthesis process is to get a CT \( \Sigma \Delta \) modulator able to meet the objective performance specifications, with a minimum power consumption and a minimum occupation of silicon area.

The synthesis procedure, schematically shown in Fig.2, starts by an architectural exploration, which basically tries to obtain candidate architectures, defined by the order of the modulator, \( L \), the number of bits of the quantizer(s), \( B \), and the oversampling ratio, \( M \), which allows to obtain a certain SNR specification. This architectural exploration is performed by using analytical expressions which model the dominant error sources limiting the achievable SNR. The modeling of these error sources will be discussed in Section 3.
The output of this architectural exploration is a set of candidate architectures that are potentially capable of meeting the modulator performance specifications. Frequently, more than one architecture is considered for later stages for several reasons:

- The modeling equations are very approximate and, therefore, there is no guarantee that the selected architecture will continue to meet the performance specifications when more accurate models containing the non-idealities of the particular physical implementation are used.
- The optimal architecture is that which, meeting the performance constraints, minimizes objectives like power consumption or area occupation. Exploration criteria at the architectural level include considerations like order minimization, minimization of oversampling ratio to avoid infeasible sampling frequencies in terms of power consumption and minimization of number of the bits in the quantizer to avoid the use of linearization techniques [4] or digital calibration [7]. As can be observed, power or area criteria at this level are of a qualitative nature and, therefore, any ranking of candidate architectures performed may suffer significant changes when progressing through the synthesis process.

The set of candidate architectures is refined using very simple functional models combined with optimization. The simulation is performed at the functional block level as no topology has been synthesized yet. The following step is the topological synthesis, i.e., the definition of the cascade architecture, the intra-ant inter-stage loop filter transfer functions and the cancellation logic functions. A direct synthesis method in the continuous-time domain is used here instead of the more conventional discrete-time to continuous-time transformation of an equivalent discrete-time topology. The direct topological synthesis method is described in Section 4.

Then, an accurate behavioral simulation is used with the global optimization procedures to find out the maximum values of non-idealities of the different building blocks which can be tolerated while still meeting the modulator performance specifications. At this level, power consumption estimates are much more detailed as relationships with each building block specifications can be established [8]. Exhaustive verification under different operating conditions is performed using accurate behavioral simulation. If a consequence of this verification, some performance specification degrades beyond certain limits, the high-level synthesis and/or the architectural synthesis are performed again under harder constraints. Specification transmission can be made more efficient if Pareto-optimal fronts of candidate architectures are available. These fronts represent trade-off hypersurfaces between the different circuit performances [9],[10]. For illustration’s sake, Fig.3(a) shows the trade-offs between dc-gain, gain-bandwidth product (GB) and power for a cascode operational amplifier. Projection on the XY plane allows to easily visualize the best trade-off between dc gain and GB that the circuit at hand can achieve. Although not easily visualized, Pareto fronts have usually higher dimensionality: all specifications of interest of the building block. Pareto fronts make high-level exploration more efficient and allow to get better designs as there is information at the modulator level on which are the achievable specifications of each sub-block as well as which is the power and area budget for them.

The last step of the synthesis procedure is the sizing of the building blocks. This sizing is performed by combining an electrical simulator with the global optimization procedures described in Section 5. The implementation of the optimization core is flexible enough to incorporate valuable design knowledge of each building block. At the optimization level, design knowledge brings knowledge of the feasibility space, limiting, therefore, the exploration space and making the synthesis process more efficient and/or enhancing the optimization results.

With all blocks sized, a final verification of the complete modulator at the electrical level at a limited number of operating conditions is performed. This verification is complemented by a more exhaustive verification at the behavioral level with information extracted at the electrical level. Performance degradations beyond tolerable margins induce redesign iterations at the circuit and/or modulator levels.

3. PERFORMANCE MODELING AND SIMULATION

As shown in Section 2, design space exploration and specification transmission rely on multiple performance evaluations, with different levels of abstraction and accuracy. At a high level of abstraction, modulator performance is modeled by a set of closed-form equations, relatively inaccurate, but with essential information on the design parameters dominating the system behavior. The signal to noise ratio of a ΣΔ modulator is given by:

\[
SNR = \frac{A^2}{2P_e}
\]  

(1)
where \( A \) represents the magnitude of the input signal and \( P_e \) represents the in-band error power. Ideally, the in-band error power only contains the quantization noise \( P_{eq} \):

\[
P_{eq} = \frac{X_{FS}^2}{B_w f_s (2^B - 1)} \int_0^{B_w} |N_{TF}(f)|^2 df
\]

(2)

being \( X_{FS} \) the full-scale of the quantizer, \( B \) the number of bits of the quantizer, \( f_s \) the sampling frequency and \( B_w \) the signal bandwidth. However, in practice, the error power contains terms due to: quantization error power enlargement, DAC non-linearities, capacitor mismatching, thermal noise, clock jitter, finite amplifier gain, incomplete amplifier settling, etc. Therefore, the in-band error power becomes:

\[
P_e = P_{eq} + \Delta P_{eq} + P_{thermal} + P_{jitter} + P_{DAC} + P_{setting} + \ldots
\]

(3)

A dominant error source in high-speed continuous-time modulators is the error power due to clock jitter. For this reason, closed-form modeling of the influence of jitter is object of special attention. The error power due to clock jitter in CT \( \Sigma \Delta \) modulators with non-return-to-zero (NRZ) Digital-to-Analog Converters (DACs) is [11]:

\[
P_{jitter} = B_w \cdot (\sigma_{\Delta})^2 \cdot \left[ \frac{A^2 \omega_i^2}{2 f_s} + \frac{X_{FS}^2 f_s}{6(2^B - 1)} \psi(\tilde{g}, \tilde{p}, \tilde{L}, L) \right]
\]

(4)

where \( A \) and \( \omega_i \) are the amplitude and frequency of the input signal, \( \psi(\tilde{g}, \tilde{p}, \tilde{L}, L) \) is a function arising from the state-space representation of the noise transfer function of the modulator and depends on the modulator order. It can be seen that it has two terms: one which depends on the modulator input and decreases with the sampling frequency and another one which depends on the modulator architecture and increases with sampling frequency.

The use of the dominant error power terms in eq. (3) (shown in eqs. (2) and (4)) allows to extract candidate triads \([L, B, M]\) with better performance in terms of distribution of the Noise Transfer Function (NTF) zeroes and insensitivity to clock jitter.

Topology refinement, specification transmission and verification require performance evaluation mechanisms with much higher accuracy than that provided by approximate equations like (2)-(4). Moreover, as this performance evaluation is frequently performed within an iterative optimization process, simulation efficiency is critical for the synthesis process.

Figure 3: (a) Gain / GB / Power Pareto-optimal hypersurface for a cascode operational amplifier; (b) Gain / GB projection.
ΣΔ modulators are strongly non-linear sampled-data circuits, and hence, simulation of their main performance specifications has to be carried out in the time domain. Due to their oversampling nature, this means that long transient simulations are necessary to evaluate their main figures of merit. Therefore, transistor-level simulations yield excessively long computation times. An appropriate trade-off between simulation accuracy and efficiency is accomplished by using behavioral simulation. In this approach, the modulator is partitioned in a set of building blocks which are modeled by a set of equations, containing the main block functionality, as well as the most important non-idealities. The selected implementation platform has been Matlab/Simulink [12] due to its wide extension, powerful data processing tools and flexibility to build block libraries. Behavioral models of the continuous-time building blocks, are described by a set of continuous-time state-space equations which are integrated by Simulink solvers. To increase simulation efficiency, we make extensive use of S-functions [13]. This mechanism allows to model non-idealities by embedding C-code routines instead of interconnecting numerous Simulink elementary blocks. The basic building blocks modeled in the behavioral simulator, as well as its non-idealities are summarized in Table 1.

Table 1: Basic building blocks and non-idealities modeled in the behavioral simulator

<table>
<thead>
<tr>
<th>Block</th>
<th>Non-idealities</th>
</tr>
</thead>
<tbody>
<tr>
<td>Integrators</td>
<td>Finite and non-linear gain, dynamic limitations (parasitic capacitors, one- and two-pole transconductor model), thermal noise, finite output swing, linear input range, offset.</td>
</tr>
<tr>
<td>Resonators</td>
<td>Non-idealities associated to the integrators.</td>
</tr>
<tr>
<td>Comparators</td>
<td>Offset, hysteresis, signal-dependent delay</td>
</tr>
<tr>
<td>Quantizers /DACs</td>
<td>Integral non-linearity, gain error, offset, jitter, excess loop delay.</td>
</tr>
</tbody>
</table>

The developed toolbox includes several libraries of CT building blocks (integrators and resonators) considering different circuit implementations: gm-C, gm-MC, active-RC and MOSFET-C. As an illustration, let us consider, for instance, the gm-C integrator depicted in Fig.4(a). The ideal behavior of this circuit is described by the following differential equation:

\[ g_m v(t) + i(t) = C \frac{dv_o(t)}{dt} \]

where \( v_i(t) \) is the input voltage, \( i(t) \) is the input current (provided by the feedback DAC block), and \( v_o(t) \) is a state variable, which can be integrated by the Simulink solvers very efficiently.

![Figure 4](image_url)

Figure 4: (a) gm-C integrator and equivalent circuit with (b) a one-pole model and (c) a two-pole model.

Fig.5 shows the complete model of a real gm-C integrator including their most significant error mechanisms, namely: input-referred thermal noise PSD (\( S_{in} \)), output voltage saturation (\( v_{i, max} \)), non-linear transconductance (modeled as \( g_m = g_{mo} + g_{mnl1}v_1 + g_{mnl2}v_1^2 \)) and the transient response. The latter is especially critical in high-speed applications. For that purpose, both a single-pole and a two-pole models have been considered in the behavioral simulator, by using the equivalent circuits shown in Fig.4(b) and (c), respectively.
These models are included in the corresponding S-function through a set of state-variable equations. As an illustration, Fig. 5(b) shows the main parts of the S-function corresponding to a two-pole model of a gm-C integrator. In this case, the transient response is modeled as:

$$\begin{align*}
\dot{v}_m &= g_m(a_1 v_i + a_2 v_i^2) \\
\dot{v}_o &= -\frac{1}{(C+1)}(g_m/a_1 v_i + g_m/a_2 v_i^2)
\end{align*}$$

Examples of the application of this behavioral simulator can be found in Section 4 and Section 6.

### 4. TOPOLOGICAL SYNTHESIS

Cascaded continuous-time $\Sigma\Delta$ modulator architectures are usually synthesized by first synthesizing a $\Sigma\Delta$ modulator with the same performance specifications in the discrete-time domain and then applying a discrete-time to continuous-time transformation that keeps the same digital cancellation logic [14]. However, obtaining a functional continuous-time $\Sigma\Delta$ modulator from this transformation and keeping the cancellation logic requires every state variable and DAC output to be connected to the integrator input of subsequent stages as Fig. 6 shows for a 2-1-1 architecture. This means a larger number of analog components (transconductors and amplifiers), which translates into larger area, power consumption and larger sensitivity to circuit tolerances. This sensitivity is illustrated in Fig. 6(b), which shows the SNR loss as a function of the standard deviation of the transconductances ($\sigma_{\text{gm}}$) and capacitances ($\sigma_C$).
To avoid this, we have implemented a synthesis method directly in the continuous-time domain. Let us consider the general case of a cascaded CT $\Sigma\Delta$ modulator with $m$ stages shown in Fig.1 and let us denote:

$$F_{ij} = F_{ij}(s) = \frac{\text{Input Quantizer } j}{y_i(s)}$$  \hspace{1cm} (7)

the transfer function from $y_i(s)$ to the input of $j$-th quantizer.

The synthesis method starts by optimally placing the poles of the single-loop transfer functions $F_{ij}(s)$. Their numerators are refined by combining behavioral simulation with an iterative simulation process, which starting from the nominal values required to place the zeros of the corresponding Noise Transfer Function (NTF), optimizes the modulator performance in terms of dynamic range and stability. For this purpose, these coefficients are varied in a range around their nominal values in order to maximize the Signal-to-Noise Ratio (SNR) while keeping stability. Then, $F_{ij}(s)$ are automatically determined by the inter-stage integrating paths.

If the modulator input, $x(t)$, is set to zero, it can be shown that the output of each stage $y_k(z)$ can be written as:

$$y_k(z) = \frac{E_k(z) + \sum_{i=1}^{k-1} Z^{-1} \left[ H_{DACF_{ik}} \right]_{nT_s} y_i(z)}{1 - Z^{-1} \left[ H_{DACF_{kk}} \right]_{nT_s}}$$  \hspace{1cm} (8)

where $Z$ stands for the Z-transform, $L^{-1}$ is the inverse Laplace transform.

The output $y_o$ of the modulator can be written as:

$$y_o = \sum_{k=1}^{m} y_k CL_k = \sum_{k=1}^{m} \left( \frac{E_k(z) + \sum_{i=1}^{k-1} Z^{-1} \left[ H_{DACF_{ik}} \right]_{nT_s} y_i(z)}{1 - Z^{-1} \left[ H_{DACF_{kk}} \right]_{nT_s}} \right) CL_k$$  \hspace{1cm} (9)

where $CL_k(z)$ represent the partial cancellation logic transfer function of the $k$-th stage.

The partial cancellation logic transfer functions can be calculated by imposing the cancellation of the transfer function of the first $m-1$ quantization errors $E_k(z)$ in (9). This gives:
where the partial cancellation logic transfer function of the last stage, $CL_m(z)$, can be chosen to be the simplest form that preserves the required noise shaping.

Using this method the 2-1-1 architecture in Fig.7(a) is synthesized. As can be observed, the circuitry is significantly less complex than that in Fig.6(a). Another positive consequence is the better sensitivity to parameter tolerances, as the $SNR$ loss in Fig.7(b) shows for the same transconductor and capacitance mismatches that Fig.6(b).

**5. OPTIMIZATION TOOL**

Design space exploration and specification transmission rely on the interaction of some kind of performance evaluator: equations, behavioral simulator (with models at some level of abstraction), with an optimizer. The cornerstones of this process are: (1) an adequate formulation of a cost function, which quantifies the degree of compliance of the design with the targeted performance; (2) a fast yet accurate method to evaluate the cost function; and (3) an efficient technique to generate the next movement over the design space. The second point mainly depends on the performance evaluation mechanism, which has already been discussed in Section 3.

Optimization algorithms can be classified into local optimization and global optimization ones. Local optimization algorithms are generally fast but require a good initial guess. Therefore, they are appropriate for fine-tuning of already good designs, otherwise, they get quickly trapped into a local minimum. Global optimization algorithms do not need a good initial point as they incorporate mechanism to escape from local minima, at the price of a larger computation time. Global optimization algorithms include a variety of evolutionary and simulated annealing algorithms with all their derivatives.

The optimization core used here is a two-step one: in the first one, global optimization techniques inspired on simulated annealing, are applied, while deterministic ones are applied in the second. Unlike conventional simulated annealing procedures, in which the control parameter – commonly named temperature – follows a predefined temporal evolution pattern, the implemented global optimization algorithm dynamically adapts this temperature to approximate a predefined evolution pattern of the acceptance ratio (accepted movements / total number of iterations). This idea prevents excessively high temperatures which will make convergence difficult and inappropriately low temperatures which can make the algorithm to stuck on a local minimum. The amplitude of parameter movements through the design space is also synchronized with the temperature for improved convergence [15].

**Figure 7:** Cascade 2-1-1 CT ΣΔM architecture using the direct synthesis method and effect of mismatch on the SNR.
For efficiency reasons, the optimization core has been conceived as an independent application whereas the behavioral simulator runs in Matlab/Simulink. In order to integrate both processes, a special-purpose application has been developed by using the Matlab engine library [16]. This application is responsible for the communication between the optimization core and the behavioral simulator so that the optimization core runs in background while Matlab acts as a computation engine.

6. CASE STUDY

The objective specifications for the continuous-time ΣΔ modulator are 12 bits with 20MHz signal bandwidth for a VDSL application, to be implemented in a 130nm CMOS technology. As a result of the different steps of the architectural exploration process, a fifth-order \((L = 5)\) cascade ΣΔ modulator, conceptually shown in Fig.8(a), was selected. It consists of a 2-2-1 topology, clocked at \(f_s = 240MHz\) \((M = 6)\), with \(B = 4\) and NRZ DACs in all stages in order to minimize the effect of jitter.

The intra- and inter-stage transfer functions \(F_{ij}\) are

\[
F_{11}(s) = \frac{b_{11}s + b_{10}}{(s^2 + \omega_1^2)} \quad F_{22}(s) = \frac{b_{21}s + b_{20}}{(s^2 + \omega_2^2)} \quad F_{33}(s) = \frac{b_{30}}{s} \\
F_{13}(s) = \frac{b_{10}b_{20}b_{30}}{s(s^2 + \omega_1^2)(s^2 + \omega_2^2)} \quad F_{23}(s) = \frac{b_{20}b_{30}}{s(s^2 + \omega_2^2)}
\]

(11)

where \(\omega_{1,2}\) stand for the optimal placement of the pole frequencies. Coefficients \(b_{ij}\) in (11) are found through an iterative simulation-based process that – starting from nominal values required to place the zeroes of the corresponding NTF – optimizes the modulator performance in terms of dynamic range and stability. For this purpose, these coefficients are varied in a range of up to ±20% around their nominal values in order to achieve the maximum Signal-to-Noise Ratio (SNR) while keeping stability. The partial CL transfer functions can be calculated from (10), giving the expressions:
shown here.
The building blocks: front-end opamp, loop filter transconductors, quantizers and DACs are designed using the (at the block level) that can be tolerated in.
The result of this sizing process is summarized in Table 3, showing the maximum (minimum) values of the non-idealities block specifications using statistical optimization for design
The modulator was high-level sized, i.e., the system-level specifications (12-bit@20-MHz) were mapped onto building-block specifications using statistical optimization for design parameter selection and behavioral simulation for evaluation. The result of this sizing process is summarized in Table 3, showing the maximum (minimum) values of the non-idealities (at the building block level) that can be tolerated in order to fulfill the required modulator performance.

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<table>
<thead>
<tr>
<th>Table 2: Loop filter coefficients of the ΣΔ modulator</th>
</tr>
</thead>
<tbody>
<tr>
<td>$R_{10} = R_{f0} = 1 \text{ kΩ}$; $R_{s} = 5 \text{ kΩ}$,</td>
</tr>
<tr>
<td>$k_{g1} = 500 \mu \text{A/V}$</td>
</tr>
<tr>
<td>$C_1 = C_3 = 6 \text{ pF}$</td>
</tr>
<tr>
<td>$C_4 = C_5 = 0.75 \text{ pF}$</td>
</tr>
<tr>
<td>$k_{g2} = 800 \mu \text{A/V}$</td>
</tr>
<tr>
<td>$k_{g3} = k_{g5} = k_{g7} = k_{g9} = 200 \mu \text{A/V}$</td>
</tr>
<tr>
<td>$k_{g6} = 158 \mu \text{A/V}$</td>
</tr>
<tr>
<td>$k_{g8} = k_{g9} = k_{g10} = 100 \mu \text{A/V}$</td>
</tr>
</tbody>
</table>

The building blocks: front-end opamp, loop filter transconductors, quantizers and DACs are designed using the methodology described in Section 2. Due to space limitations, only the synthesis results of the front-end opamp sizing are shown here.

<table>
<thead>
<tr>
<th>Table 3: High-level sizing of the ΣΔ modulator</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Front-End Opamp</strong></td>
</tr>
<tr>
<td>DC Gain</td>
</tr>
<tr>
<td>GB</td>
</tr>
<tr>
<td>Phase margin</td>
</tr>
<tr>
<td>Differential output swing</td>
</tr>
<tr>
<td><strong>Loop Filter Transconductors</strong></td>
</tr>
<tr>
<td>DC Gain</td>
</tr>
<tr>
<td>Differential Input Amplitude</td>
</tr>
<tr>
<td>Differential Output Amplitude</td>
</tr>
<tr>
<td>Third-order non-linearity</td>
</tr>
</tbody>
</table>
Fig. 9 shows the schematic of the front-end operational amplifier used together with its common-mode feedback circuit. It is a fully differential telescopic cascode topology with gain boosting. After a simulator-in-the-loop optimization process is applied, the resulting sized circuit has the electrical performances in Table 4. A similar sizing procedure is applied for the other building blocks.

<table>
<thead>
<tr>
<th></th>
<th>GB</th>
</tr>
</thead>
<tbody>
<tr>
<td>DC Gain</td>
<td>71 dB</td>
</tr>
<tr>
<td>Phase Margin</td>
<td>80º</td>
</tr>
<tr>
<td>Parasitic input capacitance</td>
<td>0.36 pF</td>
</tr>
<tr>
<td>Parasitic output capacitance</td>
<td>0.4 pF</td>
</tr>
<tr>
<td>Differential output swing</td>
<td>0.7 V</td>
</tr>
<tr>
<td>Power consumption</td>
<td>20mW</td>
</tr>
</tbody>
</table>

The modulator performance has been verified by exhaustive simulations. As an illustration, Fig. 10 shows the output spectrum for an input sinewave of -6.5-dBV amplitude and 1.76-MHz frequency. The maximum \( \text{Signal-to-(Noise+Distortion) Ratio (SNDR)} \) is 80 dB (\( \approx 13 \text{ bits} \)). These results correspond to a full electrical-level simulation. This type of verification is only feasible for a limited set of simulation conditions. A more exhaustive verification is performed by using the behavioral simulator with data obtained from the electrical simulation of the building blocks. This allows, for instance, the application of Monte Carlo simulation to evaluate the influence of mismatch on performance deviations. In the present case, it is obtained that even in the worst-case mismatch a maximum \( \text{SNDR} \) larger than 74 dB is obtained.

**ACKNOWLEDGEMENTS**

This work was supported by the Spanish Ministry of Science and Education (with support from European Regional Development Fund) under Contract TEC2004-01752/MIC and FIT-330100-2006-134 SPIRIT Project (“Secured Platform for Intelligent and Reconfigurable Voice and Data Terminals”), funded by the Spanish Ministry of Industry, Tourism, and Commerce.

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