APS Design Alternatives in 0.18 μ m CMOS Image Sensor Technology

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Abstract—This paper presents a chip designed for the purpose of evaluating different design alternatives in a 0.18 μ m CMOS Image Sensor Technology (CIS) for Active Pixel Sensor (APS) based vision applications. CIS technology improves characteristics such as sensitivity, dark current and noise, that are strongly layout dependent. It also allows the use of special structures, such as color light filters and microlenses. This chip includes a set of pixel architectures where different parameters have been modified: layout of active diffusion, threshold voltage of the source follower transistor and the use of microlenses. Besides, structures to study the influence of crosstalk between pixels have been incorporated.

Keywords—component; Image Sensors; Active Pixels Sensor; CIS Technology

I. INTRODUCTION

CMOS Image Sensors are nowadays used in a wide range of applications, from digital photography to surveillance systems and even toys incorporate them. First CMOS image sensors were developed using standard technologies [1]. However, the performance of these image sensors in certain applications was poor (e.g. low sensitivity or large dark current), especially as technologies scaled down [2]. Therefore, foundries incorporated additional steps in their standard CMOS processes to improve sensors performances, developing what is presently known as CMOS Image Sensors Technologies. Additionally, these technologies incorporate post CMOS processing steps that are useful for imaging applications like microlenses and color filters.

During the last few years, different CIS technologies have been developed which include different optimized sensors. A first process variation consists of modifying the doping profiles of the photodiode to improve sensitivity and dark current, keeping the traditional 3-transistors APS (3T-APS) architecture. Another modification introduces the use of pinned photodiodes in a 4-transistors architecture with transfer gate [3].

It is important to remark that, in these technologies, N-Well and P implant regions are only allowed outside the pixels area; consequently, neither PMOS devices nor substrate contacts are permitted inside pixels. The lack of substrate contacts is compensated by a very low resistance substrate.

Different foundries offer this type of technologies to their customers. However, the performance of sensors designed in CIS technologies is very dependent on the size and shape of the pixel itself. For this reason, it is strongly recommended to use test chips to optimize pixel design for a given application. The pinned photodiode technology shows a higher layout dependence of the sensor performance than the 3T-APS technology, being this last one, which mainly modifies the doping profiles of the photodiode, the selected technology for this work.

Section II presents a chip prototype fabricated in the Conventional Photodiode UMC 0.18 μ m CIS technology (2P4M), where different design parameters have been varied to evaluate their impact on pixel performance. Section III presents the experimental results of this chip and finally some conclusions are drawn out in section IV.

II. CHIP DESIGN

In order to optimize the layout of the pixels in this technology, a chip has been developed which includes 12 arrays of different pixels. These arrays are addressed as parts of a unique sensor array whose dimensions are 256x138. The active row and column are multiplexed and therefore the active pixel is connected to the output buffer, which provides a signal ready to be externally read. The general block diagram of the chip is shown in Fig. 1.

The pixels are based on the 3T-APS architecture, where all the transistors are polarized at 3.3V. The schematic of the pixels is shown in Fig. 2. It contains a reset transistor (S_1) which precharges the photodiode node to a known voltage; in this case, this voltage would be VDDPIX minus the threshold voltage of the reset transistor. It also includes a row switch (S_2) to connect the source follower (M_1) to the output amplifier structure through the column selecting circuitry.

Preserving the previous circuitry, different pixel designs have been included in the chip taking into account the following parameters:

- *Threshold Voltage of Source Follower Transistor*

This technology offers three types of transistors with different threshold voltage: Zero, Low and Regular V_{th} . The use of low V_{th} transistors improves the dynamic range of the sensor, although it might affect the pixel output signal. In

Figure 1. Block Diagram of the chip.

Figure 2. Pixel schematic

this case, pixels with equal layout have been included both with low and regular V_{th} transistor.

- *Layout of Active Diffusion*

This technology does not allow all type of angles in the active diffusion layout and its connection to the reset transistor, i.e., there are layout rules for inner and outer angles in these areas. This is due to the fact that abrupt angles would result in stress and malformation which would increase non desirable effects like dark current. Therefore, we have developed the pixels in two shape-like schemes: octagonal and round-like. Octagonal-like pixels contain fewer corners in the diffusion shape than round-like ones, but their angles are more abrupt (135° degrees). Round-like ones contain more corners but angles are wider than 135° degrees. The final layouts of the pixels with respect to their active area shape are shown in Fig. 3.

- *Pixel Size*

Two different pixel sizes are used in this work $3.5 \times 3.5 \mu m^2$ and $7 \times 7 \mu m^2$. Their layouts can be seen in Fig. 3. The first dimension was selected considering a minimum photodiode area that preserved the correct angles and spacing in the connection between the active diffusion and the rest of the circuitry, but could still collect enough light to have good sensitivity values.

- *Crosstalk*

The pixel would be affected not only by the light incident directly on it but also by carriers created by light incident on its neighbor pixels that have laterally diffused or by light that scatters through the different overlaying metals until arriving

Figure 3. Different pixel layouts.

to neighbor pixels. Crosstalk effects can be studied by including arrays of pixels with all, except the central pixel, covered with the top metal and characterizing the response of the array when illuminated. Three different pixel sizes have been included in the chip ($3.5 \mu m$, $5 \mu m$ and $7 \mu m$ pitch) corresponding to three arrays of 11×11 pixels.

- *Use of Microlenses*

The microlenses are intended to increase sensitivity and minimize crosstalk between pixels. The principle of its application is shown in Fig.4. The microlenses are centered in the middle of the photo diffusion active area and focus the light to this point, part of which would have not arrived to the sensor area, especially when no perpendicular incidence of light is observed. To study the effect of microlenses in this technology, pixels with the same layout with and without microlenses are included in the chip design. An additional crosstalk array with microlenses and pixel size ($3.5 \mu m$) has been included.

Figure 4. Influence of microlenses in the light incident on the pixel sensors.

Table 1 summarizes all the arrays included indicating their main characteristics and their position in the chip according to the layout shown in Fig. 5.

TABLE I. SUMMARY OF THE ARRAYS INCLUDED IN THE CHIP.

Arrays	Characteristics				
	Array Size	Pixel Size(μm^2)	Shape-like	Low Voltage	Microlenses
1	64x64	3.5x3.5	Round	-	X
2	64x64	3.5x3.5	Round	X	-
3	64x64	3.5x3.5	Octagonal	-	-
4	64x64	3.5x3.5	Round	-	-
5	64x64	7x7	Octagonal	-	-
6	64x64	7x7	Round	-	-
7	64x64	7x7	Round	X	-
8	64x64	7x7	Round	-	X
9	11x11	3.5x3.5	Round	-	X
10	11x11	3.5x3.5	Round	-	-
11	11x11	5x5	Round	-	-
12	11x11	7x7	Round	-	-

III. EXPERIMENTAL RESULTS

In order to test the different arrays included in the chip a PCB board controlled by a FPGA has been developed. This test board retrieves the pixels voltages, converts them into digital data and stores them. When the frame is completed, the information is sent to a computer to be analyzed. The result of the mathematical analysis is presented in this section.

The test board, where the chip is mounted, has been introduced into an optical bench which incorporates a visible light source, whose output light power can be varied through a computer controlled power supply. Interference narrow bandpass filters (with FWHM=10nm) centered at wavelength ranging from 400-900nm, at 50nm steps, are used to evaluate the spectral response.

A. Sensitivity Measurements

Sensitivity measurements are shown in Fig. 6. First, it is noticeable that the use of microlenses has a significant ratio of improvement for the 3.5 μm pitch pixels, and it also affects positively in the larger size pixels but at a lower ratio. This difference in the microlenses improvement ratio is due to the fact that the dimension of the 3.5 μm pitch pixel is comparable with the height of metals and passivation layers. Therefore, the amount of light with large angles of incidence redirected into the sensor area is comparatively higher.

Second, the “softer” angles seem to enhance the behavior, as it is evident that octagonal pixels have the worst sensitivities for both pixel sizes, 3.5 and 7 μm .

Figure 5. Layout of the chip.

Third, we can observe that pixels with low threshold voltage transistors in the source follower have very similar sensitivity as the same pixel with regular transistors, with the positive effect of the expansion of the output voltage range in about 0.4 V for both sizes.

Finally, we compare the measurements at 550nm shown in Table 2 with the results of experiments in the standard corresponding technology using a test chip previously designed by our group, but using 1.8V supply voltage transistors. Measurements in the standard technology indicate 0.1655 V/s-lux for 5 μm pitch pixels and 0.0958 V/s-lux in 3 μm pitch pixels, which suggest a sensitivity about ten times lower at this wavelength [4].

Figure 6. Sensitivity vs. wavelength.

TABLE II. SENSITIVITIES AT 550 NM

Arrays	Sensitivity (V/s-lux)	Arrays	Sensitivity (V/s-lux)
1	1.37	5	1.84
2	0.918	6	2.08
3	0.837	7	2.23
4	0.858	8	2.42

B. Dark Current Measurements

A very important topic in image sensors is the dark current, as this will determine the minimum amount of detectable light power. Table 3 shows the results of the analysis for this design.

The measures have been taken in dark at different exposure times, with values as large as 5 seconds. It can be observed that dark signal is about 40mV/s in the 3.5 μm pitch pixel and around 20mV/s in the 7 μm ones. This is a substantial enhancement considering the measurements made in the standard equivalent of this UMC technology which indicate about 340mV/s in 5 μm pitch pixels and 1.22V/s for 3 μm [4].

TABLE III. DARK CURRENT MEASUREMENTS

Arrays	Dark Current (mV/s)	Arrays	Dark Current (mV/s)
1	40.358	5	15.018
2	52.271	6	17.654
3	35.28	7	17.206
4	42.408	8	17.654

C. Crosstalk Measurements

Regarding crosstalk structures, we have excited them with light of 550nm till just before the saturation of the central pixel. Fig.7 shows a zoom in the surrounding neighbors of the central not covered pixel.

We can observe in the pixels without microlenses that, as expected, crosstalk is lower for larger pixels. Regarding the 3.5 μm pitch pixel with microlenses, it can be seen that the crosstalk diminishes to an amount comparable with the results for the 5 μm pitch pixel. It is also remarkable that diagonal directions are much less affected, as well as the fact that pixel layout asymmetry induces a peak of crosstalk in the upper neighbor.

IV. CONCLUSIONS

We have successfully designed, implemented and tested pixel structures in the UMC CMOS Image Sensor Technology.

Figure 7. Crosstalk influence comparison.

Measurements show the enhancement in sensitivity and dark current of this technology compared with its corresponding standard technology.

It has also been concluded that round-like pixels have better sensitivity than octagonal-like ones. Besides, source follower transistors with low V_{th} expand the range of output voltages with no negative effect. Additionally, the use of microlenses diminishes crosstalk and improves sensitivity for small pitch designs.

ACKNOWLEDGMENT

This work is partially funded by the Spanish Ministry of Science (MICINN) through project TEC 2006-15722 and by the Andalusian regional government (Junta de Andalucía-CICE) through project 2006-TIC-2352.

Ing. Vargas-Sierra would like to express gratitude for her Ph.D. I3P grant by CSIC.

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