currents $A_0(t_n)$, $A_1(t_n)$ and $A_N(t_n)$, respectively. From their switching scheme it is obvious that these transistors act as current copier cells, and thus an inverted and half-period delayed copy of the current that is previously stored is available in time slot 2. Using M1 and M5, the following sum is available in time slot 2: $A_0 \cdot (-z^{-1/2}) + A_N \cdot (-z^{-1/2})$. As a result, according to (3), a current equal to $B_0 \cdot z^{-1/2}$ is available in this time slot. The switching scheme for transistor M6 is chosen in such a way that in time slot 2 a current equal to $(-A_N) \cdot z^{-1/2}$ is available. Also, transistor M3 provides in time slot 2 a current equal to $A_1 \cdot (-z^{-1/2})$ and thus the current $B_1 \cdot z^{-1/2}$ is produced.

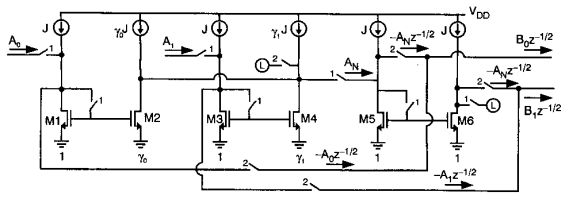

Fig. 3 *Proposed implementation of SFG in Fig. 2c*

Because of availability of reflected signals in time slot 2 it is obvious that, for the adaptor which would be subsequent in the cascade sequence, currents should be stored in time slot 2 and summed in time slot 1. In this way, the switching scheme for this adaptor should be modified accordingly. For realising the first and last adaptor configurations in Fig. 1, the corresponding modified SFGs could be obtaining following the procedure introduced in this Section.

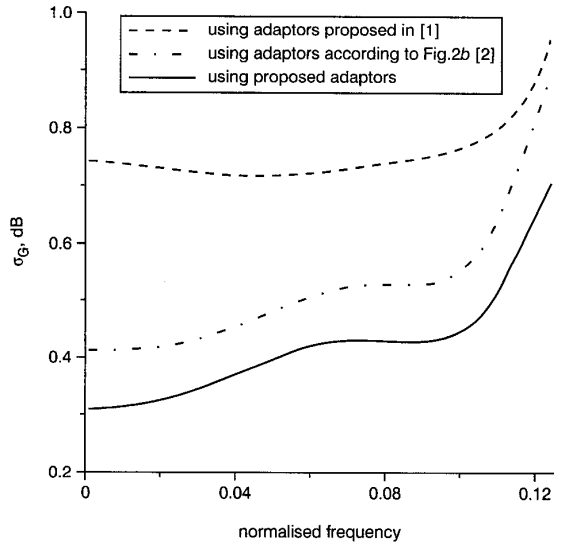

Fig. 4 *Computed standard deviations of gain for proposed filter configuration and those based on [1]* and [2]

Comparison results: A fifth-order Chebyshev SI wave lowpass filter, with 0.177 dB ripple and a normalised cutoff frequency $f_c/f_s = 0.125$, was designed. The corresponding adaptor coefficients were $\gamma_{00} = \gamma_{15} = 1.5459$, $\gamma_{10} = \gamma_{05} = 0.4541$, $\gamma_{01} = \gamma_{14} = 0.1644$, $\gamma_{11} = \gamma_{04} = 1.8356$, $\gamma_{02} = \gamma_{13} = 1.8904$ and $\gamma_{12} = \gamma_{03} = 0.1096$. The effect of MOS transistor parameter mismatch was studied using an ASIZ simulator, and considering uncorrelated 0.5% random errors for the transconductance ratios of the current mirrors. The simulated standard deviations of gain (σ_G), at passband frequencies, for the proposed filter and those derived according to [1] and [2], are shown in Fig. 4. From this plot it is concluded that the proposed filter configuration has better performance with respect to the effect of mismatching. In addition, 35 MOS transistors are required for implementing the current mirror and copier cells in the proposed filter configuration. For filters derived from [1] and [2] the corresponding requirements are 56 and 81 transistors, respectively. Thus, the proposed filter configuration also offers reduced DC power dissipation and required silicon area. Conversely, an increase of the clock feed-through effect appeared to be due to the usage of extra switches and this can be removed using the S^3I technique [5].

Conclusions: A novel SFG representation of a two-port parallel adaptor block for implementing SI wave filters is presented. This was achieved in such a way that the number of required current inversions is decreased. The derived filter configuration offers reduced sensitivity to the mismatching, lower DC power dissipation and smaller required silicon, compared to the already published implementations. Further research effort should be carried out, including the evaluation of the DC offset current and harmonic distortion caused by the mismatches in current factor and threshold voltage, in order to study in more detail the performance of the proposed configuration.

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References

1 RUEDA, A., YUFERA, A., and HUERTAS, J.L.: 'Wave analogue filters using switched-current techniques', *Electron. Lett.*, 1991, **27**, (16), pp. 1482–1483
2 YUFERA, A., RUEDA, A., and HUERTAS, J.L.: 'Programmable switched current wave analog filters', *IEEE J. Solid-State Circuits*, 1994, **19**, (8), pp. 927–935
3 JONSSON, B., and ERIKSSON, S.: 'Current-mode N-port adaptors for wave SI filters', *Electron. Lett.*, 1993, **29**, (10), pp. 925–926
4 TOUMAZOU, C., HUGHES, J.B., and BATTERSBY, N.C.: 'Switched-currents, an analogue technique for digital technology' (Peter Peregrinus Ltd., London, 1993)
5 HUGHES, J.B., and MOULDING, K.W.: 'S^3I: the seamless S^2I switched-current cell'. Proc. IEEE Int. Symp. Circuits and Systems (ISCAS), Hong Kong, June 1997, pp. 113–116

Precise 90° quadrature current-controlled oscillator tunable between 50–130 MHz

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A VLSI continuous time sinusoidal OTA-C quadrature oscillator fabricated in a standard double-poly 0.8 μm CMOS process is presented. The oscillator is tunable in the frequency range from 50–130 MHz. The two phases produced by the oscillator show an extremely low phase difference error (less than 2° over the whole frequency range). A novel current mode amplitude control scheme is developed that allows for very small amplitudes. Experimental results are provided.

Introduction: Quadrature oscillators are frequent building blocks in many telecommunications and instrumentation systems. Here, we present a tunable quadrature oscillator for the frequency range 50–130 MHz. The oscillator has been developed using OTA-C circuit design techniques, which are very appropriate for this range of frequencies [1]. The topology of the oscillator is shown in Fig. 1. The bottom part, composed of four OTAs (of transconductances g_{mA} and g_{mb}) and the two capacitors of value C, is the oscillator itself. The rest, in the upper part of the Figure, is a current-mode amplitude controlling circuitry.

OTA-C oscillator: An operational transconductance amplifier (OTA) delivers an output current I_o which is linear with its differential input voltage V_{in}, relating both signals through its transconductance gain g_m, $I_o = g_m V_{in}$. In practice the frequency dependence of g_m is crucial for OTA-C design at frequencies in the range 50–130 MHz. The most

important influence is the delay introduced by the OTA, which can be modelled by a zero at a much higher frequency ω_o [2, 3],

$$g_m(S) = g_{mo}\left(1 - \frac{s}{\omega_o}\right) \quad (1)$$

For our oscillator, because of its symmetry, the central g_{mA} OTAs output current I_1 and I_2 'see' the same impedances $Z_b(S)$ at nodes V_1 and V_2: $V_1(S) = I_2(S)Z_b(S)$, $V_2(S) = I_1(S)Z_b(S)$. Also, both have the same transconductance but with opposite sign: $I_1(S) = -g_{mA}(S)V_1(S)$, $I_2(S) = g_{mA}(S)V_2(S)$. Consequently, this results in $V_1(S) = \pm jV_2(S)$, which represents a perfect 90° phase shift between both voltages, and also between the two currents I_1 and I_2.

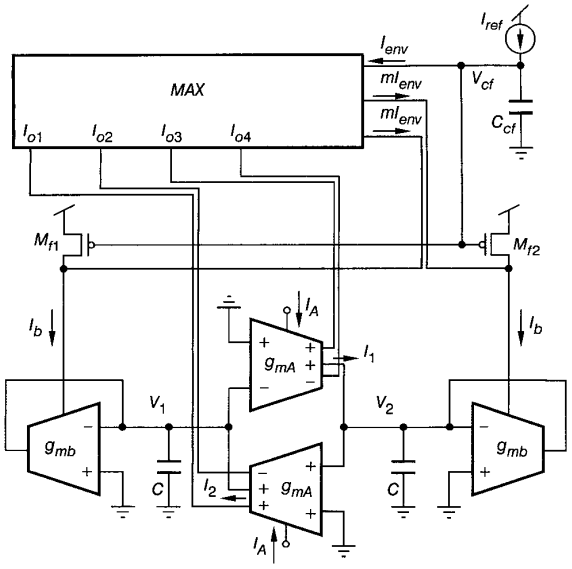

Fig. 1 *OTA-C quadrature oscillator with current-mode amplitude control loop*

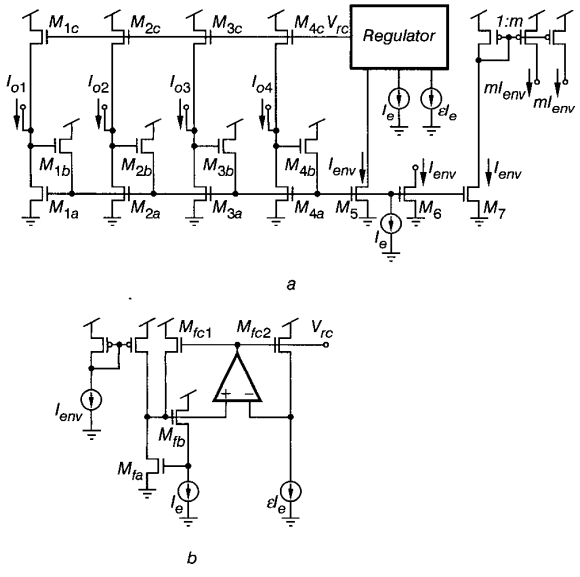

Fig. 2 *Circuit schematics of MAX circuit, and detail of regulator circuit*
a Circuit schematics of MAX circuit
b Detail of regulator circuit

Current-mode amplitude control: Each g_{mA} OTA provides two extra output currents of opposite sign. This way there will be four current signals at phases 0°, 90°, 180°, and 270°. These four signals are fed into a MAX circuit which delivers at each moment the maximum of the four inputs. Consequently, the output of the MAX circuit I_{env} extracts the instantaneous envelope of the oscillator signal (together with a small higher frequency ripple, which is actually filtered out by subsequent circuits). Current I_{env} is compared against a reference current I_{ref}, and the difference (or error) integrated onto capacitor C_{cf}. This instantaneous integral V_{cf} is used to adjust feedback currents I_b, which control the instantaneous amplitude of the oscillator. Scaled copies of the MAX circuit output mI_{env} are used to add a zero to the integrator, which is required for stability purposes [2–4]. The MAX circuit, shown in Fig. 2, is based on Lazzaro's winner-takes-all circuit [5], but where NMOS transistors M_{1c}–M_{4c} and the regulator circuit are added. Lazzaro's original circuit is not operative for signals in the range 50–130 MHz because the turning on and off of NMOS transistors M_{1b}–M_{4b} produces large voltage excursions (and delays) at the four input nodes. NMOS transistors M_{1c}–M_{4c} provide an extra current that avoids this. This extra current is minimum for the input branch and larger for the rest. The regulator circuit replicates a winner-takes-all input branch where the input current is a copy of the instantaneous maximum (or output). At the same time, a small fraction ε of bias current I_e is added to the input ($\varepsilon \simeq 1/200$), so that voltage V_{rc} is set to make transistors M_{1c}–M_{4c} drive a current εI_e for the winning branch, while driving a larger current for the rest. As a consequence, the winning branch is practically not altered, while for the rest large voltage excursions are avoided, thus speeding up significantly the time response of the MAX circuit.

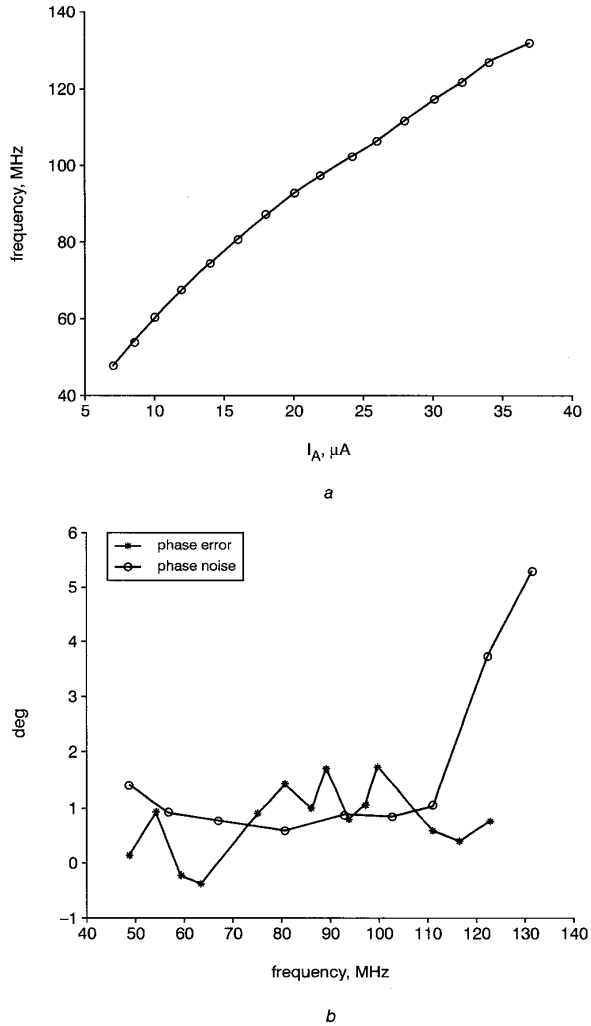

Fig. 3 *Experimentally measured dependence of oscillator frequency against control current I_A, and experimentally measured phase difference error and phase noise.*
a Experimentally measured dependence of oscillator frequency against control current I_A
b Experimentally measured phase difference error and phase noise

Experimental results: A prototype oscillator was fabricated in the AMS 0.8 μm CMOS process. It used an active area of 0.20 mm^2. The frequency was tunable between 48 and 132 MHz, by adjusting bias current I_A. The current amplitude was adjusted to be $I_{ref}=I_A/5$. This way signal excursions remain always within the same portion of the nonlinear transfer curve of the OTAs. The resulting voltage amplitude at nodes V_1 and V_2 changed between 27 and 81 mV. Fig. 3*a* shows the measured dependence between oscillation frequency and bias current I_A. The measured phase shift error between voltages V_1 and V_2 (phase(V_1)-phase(V_2)-90°) is shown (with stars) in one of the traces in Fig. 3*b*. As can be seen, there was an error of less than 2° over the complete frequency tuning range. Also shown (with circles) in Fig. 3*b* is the phase noise present at voltage V_1 (or V_2), expressed in degrees. This phase noise was computed as follows. The node voltage was recorded with 0.2 ns sampling rate over a large number of periods. Zero crossings were computed and their standard deviation calculated. This standard deviation is what is shown in the second trace of Fig. 3*b*.

Conclusions: An OTA-C topology for implementing a quadrature oscillator in the range 50–130 MHz has been presented. The topology exploits symmetry to produce the two phases at 90° phase shift. The circuit also produces four extra current signals at phases 0°, 90°, 180°, 270° which are used in a high-speed current-mode MAX circuit to extract a quasi-instantaneous envelope of the oscillations, in the current domain. This envelope is used in a properly stabilised amplitude control loop to set the oscillating amplitude at 1/5 of the current excursion range of the main OTAs, to minimise distortion. The influence of transconductance phase shift of the OTAs is considered. A complete oscillator prototype has been fabricated and tested in the AMS 0.8 μm CMOS process. The quadrature oscillator shows a phase shift between its two output signals between 89.5° and 91.7° in the frequency range from 48 to 132 MHz. Phase noise has also been characterised.

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References

1 SÁNCHEZ-SINENCIO, E., and SILVA-MARTÍNEZ, J.: 'CMOS transconductance amplifiers, architectures and active filters: a tutorial', *IEE Proc. G, Circuits Devices Syst.*, 2000, **147**, pp. 3–12
2 LINARES-BARRANCO, B., RODRÍGUEZ-VÁZQUEZ, A., HUERTAS, J.L., and SÁNCHEZ-SINENCIO, E.: 'On the generation design and tuning of OTA-C high frequency sinusoidal oscillators', *IEE Proc. G, Circuits Devices Syst.*, 1992, **139**, (5), pp. 557–568
3 LINARES-BARRANCO, B., and RODRÍGUEZ-VÁZQUEZ, A.: 'Harmonic oscillators' *in* WEBSTER, J.G. (Ed.): 'Encyclopedia of electrical electronics engineering' (John Wiley & Sons, Inc., 1999), vol. 8, pp. 632–642
4 VANNERSON, E., and SMITH, K.C.: 'Fast amplitude stabilization of an RC oscillator', *IEEE J. Solid-State Circuits*, 1974, **9**, pp. 176–179
5 LAZZARO, J., RYCKEBUSH, R., MAHOWALD, M.A., and MEAD, C.A.: 'Winner-take-all networks of *O(N)* complexity', *Adv. Neural Inf. Process. Syst. (NIPS)*, 1989, **1**, pp. 703–711

Two-step channel selection technique by programmable digital-double quadrature sampling for complex low-IF receivers

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Presented is a novel two-step channel selection technique to be adopted in complex low-IF receivers for enhancing the performance and efficiency of the front-end PLL-frequency synthesiser (PLL-FS), which will be mainly implemented by a proposed programmable digital-double quadrature sampling (D-DQS) scheme. Thus, the weaknesses of the PLL-FS in very small step-size operations including long locking time and large phase noise are significantly reduced. Simulation results of the D-DQS scheme are provided to demonstrated the feasibility of such a technique.

Introduction: In complex low-IF receivers, the intermediate frequency (IF) can be set to half of the channel bandwidth value to relax the image rejection requirement, as the maximum power of the adjacent channel is much less than the other in-band channels in most wireless communications [1]. However, when an integer PLL-frequency synthesiser (PLL-FS) is employed for channel selection, a small step-size change in the local oscillator (LO) frequency is necessary. Such traditional scenario is shown in Fig. 1*a*, where the capture of the RF channels labelled as **A**, **B**, **C** and **D**, requires a step-size of the LO frequency equal to one channel bandwidth, and the total mandatory moving steps equal to the number of channels in the entire frequency band. The resulting major drawbacks are, the longer locking time and larger phase noise values, due to insufficient bandwidth for the loop filter and large division ratio of the frequency divider in the PLL-FS [2].

In this Letter, we propose a two-step channel selection technique that alleviates the problems mentioned above through the partition of channel selection from the front-end PLL-FS to the back-end programmable digital-double quadrature sampling (D-DQS) scheme [3]. Such new channel selection technique and simulation results of the D-DQS scheme are introduced in the following Sections.

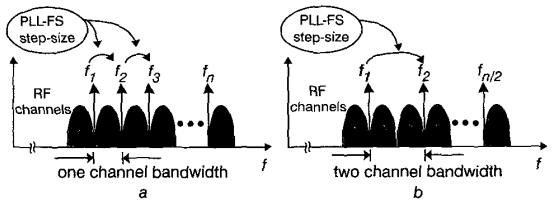

Fig. 1 *Channel selection by PLL-FS*
a Traditional method
b New proposed method

Proposed two-step channel selection technique:
Step 1: Dual-channel selection by PLL-FS: The first step of this new channel selection scheme is still performed by the PLL-FS in the front-end as shown in Fig. 1*b*, however the main difference relies on the fact that the PLL-FS only down-converts a pair of effective channels on the IF by selecting the LO frequency located between every two RF channels, e.g. channels **A** with **B** or channels **C** with **D** (the final selection between such pair of channels will be performed by the programmable D-DQS scheme in the second step). Based on this method, the block diagram of the new proposed receiver topology in shown in Fig. 2. The advantages of this topology are: (i) a higher frequency reference clock can be employed for the PLL-FS loop filter to significantly reduce the problems originated by small step-size operation, since the minimum step-size of the PLL-FS is now extended from one to two channels bandwidth; (ii) as the locking position of the LO is selected in between every two channels, the resulting moving steps of the LO frequency can be halved, which also simplifies the required division ratio of the frequency divider in the PLL-FS, thus allowing the reduction of phase noise; (iii) since the dual-channel is down-converted to a frequency range near to the baseband, the original required bandpass channel selection filters can be replaced by their lowpass counterparts. This illustrates the fact that such frequency down-conversion method can improve the PLL-FS performance and simultaneously simplify the whole receiver architecture without involving any extra-circuitry in the PLL-FS.

Step 2: Decision channel selection by programmable D-DQS: The D-DQS scheme is generally employed in the receiver back-end of the complex low-IF receiver for IF-to-baseband frequency down-conversion. Here, the programmability of D-DQS is explored in order to perform channel selection function between two adjacent channels only through a simple control. Following the channel selection from step 1, the operation of this programmable D-DQS is explained as follows: supposing that the PLL-FS has down-converted a pair of channels labelled **A** and **B** at the frequency bins $-f_{IF}$ and $+f_{IF}$ as shown in Fig. 3, (I), respectively, then the following steps will involve sampling and digitisation at the sampling frequency $f_s=4f_{IF}$. This value of f_s efficiently simplifies the following D-DQS because the multiplying values are only $\{-1, 0, 1\}$. Thus, no extra I/Q mismatch