Single Phase MOS-NDR MOBILE Networks

Juan Núñez, María J. Avedillo and José M. Quintana.
Instituto de Microelectrónica de Sevilla, Centro Nacional de Microelectrónica, Consejo Superior de Investigaciones Científicas (CSIC) and Universidad de Sevilla
Américo Vespucio s/n, 41092-Sevilla, SPAIN
FAX: +34-954466666, E-mail: {jnunez, avedillo, josem}@imse.cnm.es

***Abstract*— Devices with an *I-V* characteristic exhibiting Negative Differential Resistance (NDR) are attractive from the circuit design point of view as it has been demonstrated by Resonant Tunneling Diodes (RTDs) circuits. Ideas coming from RTD-based designs can be exported to an "all CMOS" environment by using transistor circuits to generate the NDR characteristic (MOS-NDR). In this paper novel programmable MOS-NDRs are proposed and used to realize threshold logic gates on the basis of the MOnostable to BIstable Operating principle. It is shown that these gates can be connected to build up networks that are operated in a pipelined fashion using a single phase clock scheme.**

I. INTRODUCTION

It has long been recognized that area, power and speed advantages can be obtained incorporating Negative Differential Resistance (NDR) devices in circuit design. Resonant Tunneling Diodes (RTD) exhibit such an NDR characteristic and many circuits taking advantage of it have been reported covering different applications (memories, logic, AMS) and with different goals (high speed, low power). In particular, their NDR current-voltage (*I-V*) characteristic can be exploited in logic design to significantly increase the functionality implemented by a single gate (in comparison to CMOS and bipolar technologies) [1]. In addition, those gates can be directly pipelined which results in logic networks in which each gate-level is a pipeline stage (nanopipeline) allowing very high through-output [1]. A number of threshold gates (TGs) based on RTDs monolithically integrated with three-terminal devices which implement complex logic functions have been fabricated and have demonstrated high speed and robust operation [2].

Most RTD (NDR) logic circuits are based on the MOnostable-BIstable Logic Element (MOBILE). The MOBILE [3] is a current controlled gate which consists of two NDR devices connected in series (the driver and the load) and driven by a switching bias voltage (V_{CK}). When V_{CK} is low both devices are in the on-state (or low resistance state) and the circuit is monostable. Increasing V_{CK} to an appropriate value ensures that only the device with the lowest peak current switches from the on-state to the off-state (the high resistance state). Logic functionality is achieved if the peak currents of the NDRs are controllable. For this, NDRs in series with transistor controlled by inputs (input branches) are placed in parallel to load or driver NDRs. The MOBILE structure exhibits self-latching behavior. That is, once it has evaluated with the rising edge of the clocked bias, output retains its value even if the input changes (hold phase). Because of this MOBILE gate networks operate in a pipeline fashion with a multi-phase clock scheme.

Circuit ideas coming from RTD-based designs can be exported to an "all CMOS" environment by using transistor circuits to generate the NDR characteristic, called MOS-NDR devices [4]-[8].

The contribution of this paper is twofold. First, we introduce a new programmable MOS-NDR, in which the peak current is controllable, avoiding in this way the addition of input branches to realize gates. Threshold Logic gates are designed using them. Second, we also demonstrate a single phase clock scheme to operate cascaded NDR MOBILE gates. We show that a network of MOBILE-based MOS-NDR gates can be operated with a single clocked bias signal.

The paper is organised as follows: in Section II, the proposed MOS-NDR structure is described. Section III deals with the design of inverted majority gates using this device. In Section IV, a negative edge triggered MOS-NDR device is presented, which will be used in the design of the single phase networks in Section V. Finally, some key conclusions are given in Section VI.

II. THE MOS-NDR PROGRAMMABLE DEVICE

Fig. 1*a* shows the schematic of the proposed positive edge triggered (PET) programmable MOS-NDR device, based on the structure of the non-programmable MOS-NDR device described in [5]. Figure 1*b* depicts its *I-V* characteristic. The positive differential resistance (PDR) and the negative differential resistance (NDR) region are obtained through the current of $NMOS_2$ transistor, which gate-to-source voltage is modulated by the output voltage of the CMOS inverter made

up by $NMOS_1$ and $PMOS_1$ and biased by V_{INV}. The peak voltage (V_p) and current (I_p) of the *I-V* characteristic in Fig. 1*b* is determined by properly setting up the sizes of the transistor $NMOS_2$. In this way, I_p is increased with the width of $NMOS_2$. Assuming that all transistors have the same gate length, the position of V_p is controlled by the ratio between the widths of $NMOS_1$ and $PMOS_1$. Higher values of V_P are obtained by decreasing the ratio between the widths of the transistors $NMOS_1$ and $PMOS_1$, W_{NMOS1}/W_{PMOS1}.

The peak current can be also modified by the new branch consisting of two series-connected NMOS transistors, $NMOS_S$ and $NMOS_3$. $NMOS_S$ operates as a switch controlled by the voltage supplied to terminal *PROG*, V_S, so that when it is large enough to enable $NMOS_S$, the original peak current of the device is increased. Note that other MOS-NDR devices have been proposed which control the peak current by modifying voltage V_{INV} [6], and so are not suitable to implement series-connected gates. Fig. 1*c* depicts the *I-V* characteristic, measured by a HP-4145A parameters analyzer, of a MOS-NDR which we have designed and fabricated in a standard commercial 0.13μm CMOS process. Curves for V_s='0' and V_s='1' are shown.

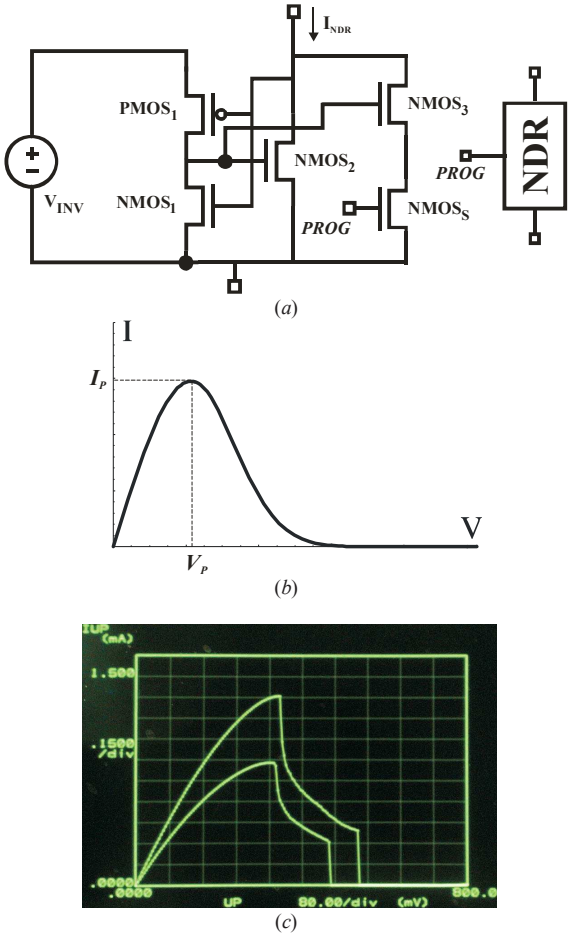


Figure 1. (*a*) Programmable MOS-NDR device and symbol. (*b*) *I-V* characteristic. (*c*) Measured *I-V* characteristic.

III. Design of MOS-NDR Inverted Majority Gates

The MOBILE operation principle can be easily extended to implement Threshold Logic gates as it has been demonstrated using RTDs [2], [1]. In the same way, TGs can be built with the proposed programmable MOS-NDR devices.

A threshold gate (TG) is defined as a logic gate with n binary input variables, x_i (i=1, …,n), one binary output y, and for which there is a set of (n+1) real numbers: threshold T and weights w_i, such that its input–output relationship is defined as:

$$F(x_1,\ldots,x_n)=\begin{cases}1 \;\; iff \;\; \sum_{i=1}^{n} w_i x_i \geq T \\ 0 \;\; iff \;\; \sum_{i=1}^{n} w_i x_i < T\end{cases} \qquad (1)$$

The basic building blocks for MOS-NDR logic circuits are Threshold Gates (TGs) instead of the conventional Boolean gates (AND, OR, NAND, NOR). This is due to the fact that when designing with these devices, threshold gates can be implemented as efficiently, in terms of performance and complexity, as conventional Boolean gates but realize more complex functions.

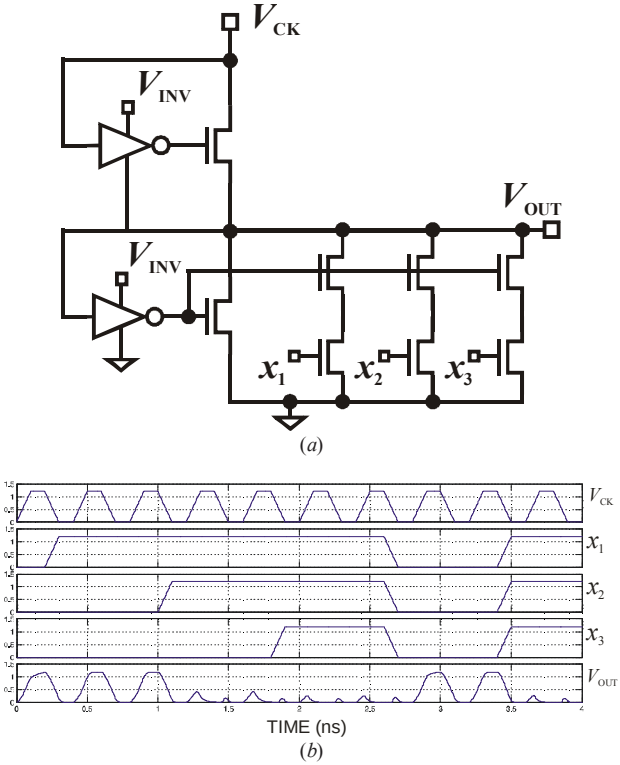


Figure 2. $NMAJ_3$ gate (*a*) PET MOS-NDR realization. (*b*) Simulation

The inverted majority gate of n inputs (n is odd), $NMAJ_n$, is a key example of TG gates. It can be written in terms of Eq. 1 as follows:

$$NMAJ_n(x_1,\ldots,x_n)=\begin{cases}1 \;\; iff \;\; \sum_{i=1}^{n} x_i < \lceil n/2 \rceil \\ 0 \;\; iff \;\; \sum_{i=1}^{n} x_i \geq \lceil n/2 \rceil\end{cases} \quad (2)$$

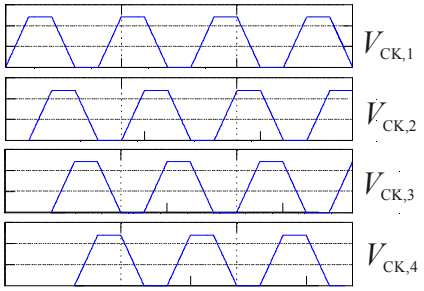


Figure 3. Four phase overlapping clocking scheme.

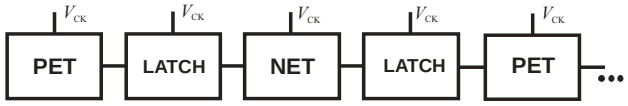
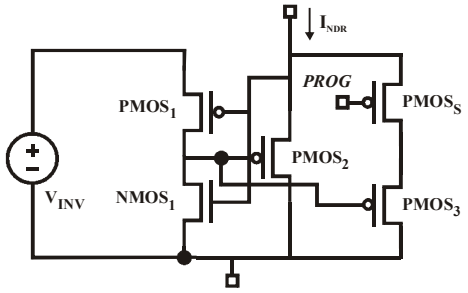
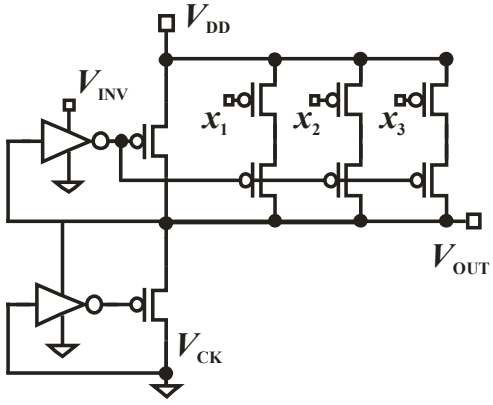


Figure 4. (*a*) Single phase pipeline network architecture



(*a*)



(*b*)

Figure 5. (*a*) NET MOS-NDR device. (*b*) NET $NMAJ_3$ gate realization.

Fig. 2*a* shows the circuit diagram of a MOS-NRD $NMAJ_3$ gate. We can consider that the structure consists on the series connection of two NDR devices (the peak current of one of them is programmed by the input set), being the output level determined by the relation between the peak currents. The operation of this gate is shown in Fig. 2*b*, where it can be observed that when two or three inputs are high (low) the output voltage goes to the low (high) level. Note that the output returns to '0' with the falling edge of the clock voltage.

IV. The Negative Edge Triggered MOS-NDR Device

Cascaded MOBILE gates are operated in a pipelined fashion using a four phase overlapping clocking scheme shown in Figure 3. The need of a multi-phase clocked bias signal is determined by the 'return to' behavior of MOBILE gates. Note that second stage ($V_{ck,2}$) evaluates while the first stage ($V_{ck,1}$) is in the hold phase. For a number of logic levels greater than three, four bias signals are required. That is, four clock signals with tight constraints on the skew between two consecutive ones have to be distributed in those circuits.

To improve the robustness of MOBILE networks, a simpler clock scheme is desirable. It has been demonstrated that a network of MOBILE-based gates can be operated with a single clocked bias signal [9]. To achieve this operation, positive edge triggered (PET) gates and negative edge triggered (NET) gates are alternated and latches are added that removes the 'return to' behavior of MOBILEs, as it is shown in Figure 4.

This solution can be easily adopted in RTD-based circuits by properly setting up the clock and the bias voltage [9]. However, since MOS-NDR circuits are made of MOS transistors, it is necessary to modify its structure in order to be able to obtain the NET MOBILE operation.

Figure 5*a* shows the circuit diagram of a MOS-NDR device suitable for NET structures (NET MOS-NDR), where the NMOS transistors $NMOS_2$, $NMOS_3$ y $NMOS_S$ are now PMOS transistors. The implementation of $NMAJ_n$ gates based on the NET MOS-NDR device is quite similar to those which are designed using PET MOS-NDR structures. Figure 5*b* depicts a $NMAJ_3$ gate based on the NET MOS-NDR device, where it can be observed that for these structures, the programmability is due to the load NDR.

V. Single Phase MOS-NDR Networks

The proposed single phase pipeline network architecture is based on the connection of alternative PET and NET gates with inverter latches inserted between them, as shown in Fig. 5. Only one clock signal is necessary to bias the circuit.

The operation of the single phase architecture is shown through the connection of four $NMAJ_3$ gates, as depicted in Fig. 6*a*. $NMAJ_1$ and $NMAJ_3$ are negative edge triggered gates, whereas $NMAJ_2$ and $NMAJ_4$ are positive edge

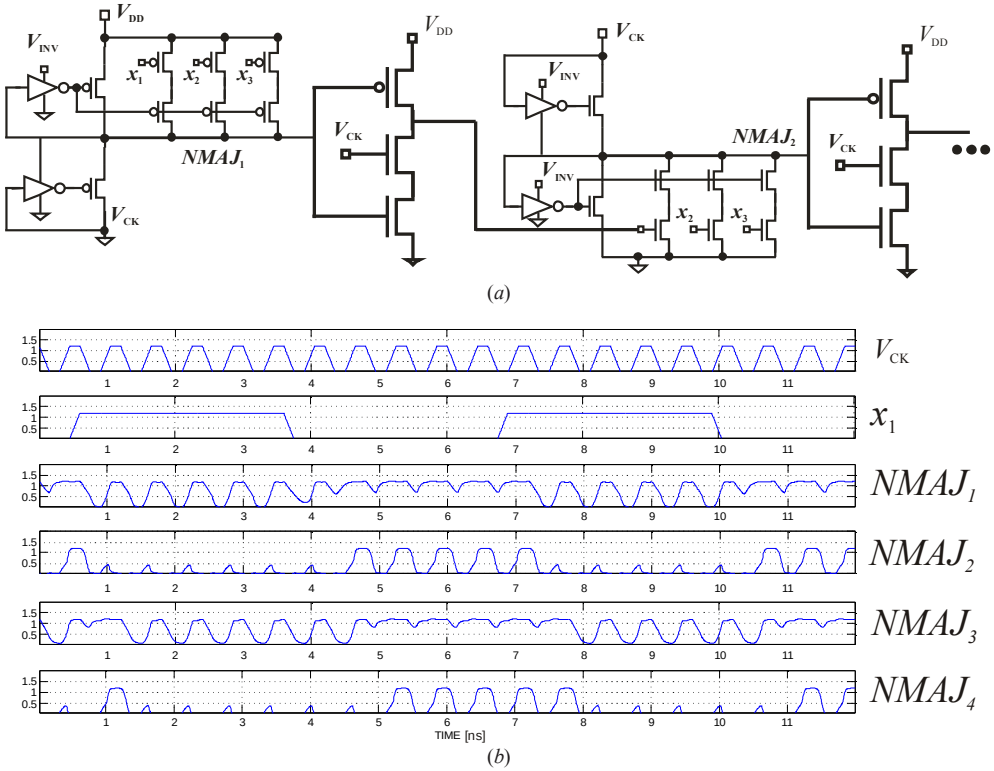


Figure 6. (*a*) Single phase connection of four inverted majority gates . (*b*) Simulation results.

triggered. For this experiment, we have considered that signals x_2 and x_3 are constant and equal to logic '0' and '1', respectively, whereas the input to the first inverted majority gate, x_1, switches between '0' and '1'.

Simulation results for a standard 0.13µm CMOS process are presented in Fig. 6*b*. We have considered that the bias voltage, V_{DD}, is equal to $1.2V$ and the voltages associated to a logic '0' and '1' are $0V$ and $1.2V$, respectively. Note that for $NMAJ_1$ and $NMAJ_3$, the reset level is equal to the top value of V_{CK}, whereas for $NMAJ_2$ and $NMAJ_4$, it is equal to the minimum value of the clock signal.

VI. Conclusions

A new realization of threshold logic gates based on a programmable MOS-NDR device is presented. We propose a single phase clock scheme to operate cascaded MOBILE-based MOS-NDR gates and improve the robustness of these networks.

Acknowledgment

This work has been funded by the Spanish Government under project NDR, TEC2007-67245/MIC, and the Junta de Andalucía through the Proyecto de Excelencia TIC-2961.

References

[1] Mazumder, P. et al., "Digital circuit applications of resonant tunneling devices", *Proc. IEEE*, 86, Apr. 1998, pp. 664-686.

[2] Pacha, C., et al., "Threshold logic circuit design of parallel adders using resonant tunnelling devices", *IEEE Trans. VLSI Systems*, 2000, 8, (5), pp. 558–572.

[3] K. Maezawa and T. Mizutani "A new resonant tunneling logic-gate employing monostable-bistable transition", *Japan Journal applied Phys. Letter*s, Vol. 37, pp. 142-144, 1993.

[4] Gan, K.-J., et al., "Four-valued memory circuit using three-peak MOS-NDR devices and circuits", *Electronics Letters*, 42, (9), pp. 514-515, 27 April 2006.

[5] K.-J. Gan, et al, "Design and fabrication of multiple-valued multiplexer using negative differential resistance circuits and standard SiGe process", *Solid-State Electronics*, 52, (6), pp. 882-885, Jun. 2008.

[6] Guo, W.-L., "CMOS-NDR transistor". *9th International Conference on Solid-State and Integrated-Circuit Technology, (ICSICT)*, pp.92-95. Oct. 2008.

[7] Wu, C., Lai, K.-N., "Integrated Λ-type differential negative resistance MOSFET device", *IEEE J. Solid-State Circuits*, SC-14, pp. 1094-1101, Dec. 1979.

[8] Nuñez, J., et al., "Fast and area efficient multi-input Muller C-element based on MOS-NDR", *ISCAS 2009. IEEE International Symposium on Circuits and Systems, 2009*, vol., no., pp.1811-1814, 24-27 May 2009.

[9] Pettenghi, H., et al.,: "Single phase clock scheme for MOBILE logic gates". *Electronics Letters*. 42. (24). pp. 1382-1383. Nov. 2006.