Systematic Generation of Performance Models of Reconfigurable Analog Circuits

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Abstract—In this work, a systematic technique to generate performance models of reconfigurable analog circuits is presented. The performance models are obtained in the form of multi-mode Pareto-optimal fronts (mm-PoFs), a new type of Pareto-optimal front (PoF) that characterizes the set of different performances that reconfigurable circuits can attain. The technique is based on the use of an evolutionary algorithm (EA) that acts as an optimizer, and the simulator HSPICE to measure the circuit performances. The use of this technique will be illustrated for a wireless multistandard problem, where a reconfigurable op-amp will be considered.

Index Terms—Analog circuits, reconfigurability, performance models, pareto-optimal fronts, evolutionary algorithms.

I. INTRODUCTION

The current trend towards the new paradigm of wireless communications (4G) aims at including more and more functionalities and support for an increasing number of communication standards in a unique device [1] [2]. This support is given traditionally by using a different circuit for each standard, but this solution compromises the area occupation. Another option is to use a unique circuit that meets the specifications of all standards, which means that the power consumption will not adapt to the communication standard being used, and, therefore, energy will be wasted. A better solution is to use reconfigurable circuits, which are capable of operating in different modes to achieve different performances. The power consumption of reconfigurable circuits can be adapted for each operation mode whereas the area occupation will be that of a single circuit.

The lack of automated CAD tools make the automation of analog design to be some steps behind the digital domain. New hierarchical design methodologies that are emerging since the last decades [3] [4] [5] propose solutions to reduce this gap between digital and analog design. Some of these methodologies are based on the use of feasibility information of the analog circuits, which can be given in the form of performance models. In this context, the use of Pareto-optimal fronts (PoF) [6] is an efficient solution, since they represent the best trade-offs among conflicting performances of the circuits

and therefore it is not necessary to explore the whole feasibility space.

Unfortunately, design methodologies based on the use of PoFs have not considered yet the analog reconfigurable circuits mainly due to the Impossibility to generate their feasibility information. For this reason, it is extremely important to generate performance models of reconfigurable analog circuits, which would support the use of these type of circuits by these design methodologies.

In this work, a systematic and fully automated technique for the generation of multi-mode PoFs (mm-PoFs), a new type of PoFs presented in [7] that models the performances of reconfigurable circuits, is presented. In the following section the generation process of the mm-PoFs using an EA is described. Section III shows some results in the form of mm-PoFs of reconfigurable operational amplifiers and their use in a multi-standard design case.

II. METHODOLOGY

The methodology proposed in this work is based on the use of an evolutionary algorithm (EA), which is an efficient way to solve multi-objective optimization problems (MOOP) [8]. EAs are based on the evolution of a population where, as in natural selection processes, new solutions are generated using mutation and crossover operators and only the best solutions, which are found using tournament and selection mechanisms, prevail. Optimization of electronic circuits can be seen as MOOPs. In a MOOP a set of conflicting functions (or design objectives) must be optimized while some constraints are fulfilled, and therefore a unique solution does not exist. MOOPs are based in the concept of Pareto-dominance, which considers that for two solutions, a and b , a is said to dominate b ($a \prec b$) if all the design objectives of a are not worse than those of b and there is at least one design objective of a that is strictly better than the same design objective of b . In the same way, a is said to be a non-dominated solution if there is no other solution that dominates it.

Reconfigurable circuits have several sets of conflicting performances (each corresponding to a different mode of operation) that must be optimized. Since their optimization can not be directly translated into a conventional MOOP, they can not be correctly solved by any available EA. Using a conventional EA, all design objectives of all operation modes would compete between them. However, there should not be a

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trade-off between the same performances of different operation modes.

In this work we propose a key modification, in the form of a new dominance criterion, in the EA NSGA-II [9], so that performances of reconfigurable analog circuits can be optimized. The basic flow of this EA is shown in Fig.1. The implementation of the new dominance criterion requires a modification of the dominance check, used in different steps of the algorithm (*Tournament and Selection* and *Filling a non-dominated sorting*).

Fig. 1. Basic flow of NSGA-II.

As stated in [7], the new dominance check must compare the operation modes of the same individual (what is called intra-individual dominance check) and the comparison between different individuals must be carried out cross-wise, that is, all operation modes of an individual are compared to all operation modes of another individual (this is called inter-individual dominance check).

Besides the implementation of this new dominance check, the definition of other parameters have been redefined to take into consideration the reconfigurability of the circuit. The **constraint violation** of the individuals, which accounts for the amount of constraints unfulfilled by the individual, is calculated as the average value between the constraint violation of its operation modes. Another important parameter is the **crowding distance**, which in a conventional MOOP is defined as the average normalized distance of the individual and its nearest neighbors in the design objective space. The crowding distance of multi-mode individuals is calculated as the average distance from their operation modes to their nearest modes in the design objective space. The importance of this parameter is related to the fact that the use of an EA to generate a PoF does not provide the true PoF, but a sampling of it. As one of the advantage of methodologies based on the use of PoF is reusability, it is desired that these sampling points are as uniform and spread as possible, because it will ensure that they can be used in a wide variety of problems. The crowding distance is a measure of this uniformity, and its correct calculation and manipulation are crucial to obtain good mm-PoFs, in terms of spread and uniformity.

In order to implement all modifications that have been described, a new structure of the individuals is used. It permits an independent treatment of the operation modes of

the individuals. Individuals are composed of modes, a global constraint violation and a global crowding distance, and each mode has its own structure composed of design objectives, constraints and crowding distance. This is shown in Fig.2.

Fig. 2. New structure of the individuals.

For the generation of the PoFs and mm-PoFs, first the topology of the circuit to be optimized is defined. **Design objectives** must be set to be maximized or minimized. **Constraints** that ensure the correct performance of the circuits must be also established. For the **design variables**, which define the circuit performance, a range for their value must be defined by the designer.

Reconfiguration strategy and directive, which refers to the variables that change from a mode to another and to how this change is done, respectively, must be specified by the designer.

Finally, the size of the population, as well as the number of generations (iterations of the evolutive loop) the optimizer will evolve, must be specified.

III. RESULTS

This section illustrates how to use a mm-PoF of an operational amplifier that is used in a multi-standard scenario where three sets of specifications must be met. Among those designs that fulfill the multi-standard specifications, it is interesting to focus on the advantages that the use of reconfigurable designs have over single-mode designs in terms of area and power consumption.

In this work, the electronic simulator used is HSPICE. The experiments have been carried out in a 0.35- μm CMOS technology with ± 1.5 -V supply voltages.

Let us consider a multi-standard problem where the 3 sets of specifications shown in Table I must be met by the folded-cascode opamp in Fig.3. The rest of transistor sizes that are not specified are dependent of these variables due to underlying circuit symmetry. The range of these variables, defined by the designer, are shown in Table II.

TABLE I
SPECIFICATIONS FOR GSM, BLUETOOTH AND UMTS STANDARDS.

Standard	DC Gain [dB]	fu [MHz]
GSM	56.90	18.1
BT	66.02	61.8
UMTS	67.96	107.6

The sets of specifications of the three standards can be achieved by means of any of three options: a single-mode

Fig. 3. Folded-cascode operational amplifier.

TABLE II
DESIGN VARIABLES AND RANGES.

Variable	Range	Variable	Range
w_1	$5 - 500 \mu m$	l_1	$0.35 - 200 \mu m$
w_3	$5 - 500 \mu m$	l_3	$0.35 - 200 \mu m$
w_5	$5 - 500 \mu m$	l_5	$0.35 - 200 \mu m$
w_7	$5 - 500 \mu m$	l_7	$0.35 - 200 \mu m$
w_9	$5 - 500 \mu m$	l_9	$0.35 - 200 \mu m$
I_{bias}	$0.35 - 200 \mu m$	-	-

design that fulfill all sets of specifications simultaneously (option 1), a different single-mode design to fulfill specifications required by each standard (option 2) or a reconfigurable design whose operation modes fulfill the specifications required by each standard (option 3). For the first two options, a single-mode PoF (sm-PoF) has been generated. For the third option, a mm-PoF with three operation modes has been generated. For both the sm-PoF and the mm-PoF, design objectives are the **DC-Gain** (A_0) and the **Unity-gain frequency** (f_u), which are maximized, and the **power consumption** (p_w) and **area**, which are minimized.

Constraints are imposed to the phase-margin, which must be between $[60^\circ - 90^\circ]$, the operation of all transistors, which must be in saturation regime. For the mm-PoF, the slew-rate must be greater than or equal to $70/90/160V/\mu s$ for the first, second and third operation modes respectively. For the sm-PoF, the slew-rate is imposed to be greater than or equal to $70V/\mu s$.

Since f_u and power consumption, as well as the slew-rate, are directly related to the bias current, a reconfiguration strategy based on the change of this variable is a very appropriate approach to attain complementary performances of the reconfigurable circuits. For the reconfiguration directive, first a value of bias current is randomly chosen in the range $[1 - 333]\mu m$. Then, this value is assigned to the bias current of the first mode and the double and triple of that value are assigned to the second and third modes, respectively. Of course, the designer has complete freedom to chose the more suitable reconfiguration strategy and directive for each

problem.

For both the single-mode and the multi-mode PoFs the population size is 1000 individuals and the number of generations is set at 200. The generation of each front required a **CPU Time** of 4h. on a 2.2 GHz processor.

Projections onto the A_0 - f_u and area-power consumption planes of the two fronts are shown in Figures 4 and 5, respectively. In Fig.6, the DC-Gain and f_u of those designs that meet the three sets of specifications by means of any of the three options previously described are shown.

Fig. 4. Projection onto DC Gain - f_u plane.

Fig. 5. Projection onto area - power consumption plane.

Fig. 6. Valid designs from options 1, 2 and 3.

As it can be seen, only modes 1 and 2 of the reconfigurable designs need to be used. In Fig.7 the area and power consumption of designs of option 1 are shown. The final design selected in this case should be one of the designs marked bold squares, which have the best trade-offs between the area and power consumption. Focusing on the extreme cases (smallest area or lowest power consumption) reduces the options between solution 1 ($743.4\mu m^2 - 1.24mW$) and solution 2 ($181.9\mu m^2 - 0.85mW$).

Fig. 7. Area and power consumption of solutions from option 1.

In Fig.8 the area and power consumption of designs from option 2 are shown. In this case, the options for GSM mode regarding smaller area and power consumption are between $(197.5\mu m^2 - 0.42mW)$ and $(90.26\mu m^2 - 0.56mW)$, while for BT and UMTS modes the options go from $(743.4\mu m^2 - 0.85mW)$ to $(181.9\mu m^2 - 1.24mW)$. These designs can be combined to form 4 solutions (from solution 3 to solution 6).

Fig. 8. Area and power consumption of solutions from option 2.

In Fig.9 the area and the power consumption of the first and second mode of reconfigurable designs from option 3 are shown. Focusing on those design with the best trade-offs between area and power consumption, the best options are between $(225.3\mu m^2 - 0.64mW)$ (solution 7, with smallest area) and $(330.7\mu m^2 - 0.61mW)$ (solution 8, with lowest power consumption) for the first operation mode, which are translated into $(225.3\mu m^2 - 1.29mW)$ and $(330.7\mu m^2 - 1.23mW)$ in the second operation mode.

Fig. 9. Area and power consumption of solutions from option 3.

In Table III the area and power consumption of the solutions of each option are shown. Reconfigurable solutions are among

the best results. Unique designs that fulfill specifications of the three standards simultaneously (option 1) either have a much larger area (solution 1) or the power consumption is much higher (solution 2) than reconfigurable designs (option 3). Solutions of option 2 have a lower power consumption in GSM mode and, for solutions 3 and 4, also in UMTS mode. However, except solution 6, the area of these solutions is higher than that of reconfigurable designs.

TABLE III
COMPARISON OF THE RESULTS

		GSM		Bluetooth & UMTS	
		area [μm^2]	power [mW]	area [μm^2]	power [mW]
OPTION 1	1	743.4	0.85	743.4	0.85
	2	181.9	1.24	181.9	1.24
OPTION 2	3	940.9	0.42	940.9	0.85
	4	833.7	0.56	833.7	0.85
	5	379.4	0.42	379.4	1.24
	6	272.2	0.56	272.2	1.24
OPTION 3	7	225.3	0.64	225.3	1.29
	8	330.7	0.61	330.7	1.23

IV. CONCLUSIONS

A new fully automated, systematic design flow methodology to generate multi-mode performance models, in the form of Pareto-optimal fronts, of reconfigurable circuits, has been presented. This concept supports the use of reconfigurable analog circuits in emerging hierarchical design methodologies. Reconfigurable analog circuits introduce important advantages in the design of multi-standard communication systems. As it has been demonstrated with the use of the automated flow presented here, reconfigurable circuits reduce the area occupation and permits an efficient distribution of the power consumption, and, therefore, an important reduction in cost.

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