Radiation Characterization of the austriamicrosystems 0.35 μm CMOS Technology

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Abstract—The design of mixed-signal ASICs for space requires a detailed knowledge of the behaviour of the technology to be used in an environment imposing radiation levels and temperatures beyond those found in standard applications. Commercial foundries providing standard CMOS technologies do not usually have or make available data on the behaviour of their devices under those conditions. Instituto de Microelectrónica de Sevilla and Universidad de Sevilla (IMSE-USE) have started a long term collaboration with the Spanish Instituto Nacional de Técnica Aeroespacial (INTA) to extend its experience on mixed-signal design to the field of ASICs for space applications. The assessment of a commercial (austriamicrosystems) 0.35 μm CMOS technology is a first step towards the development of a mixed-signal design methodology, including the development of an RHBD digital library suitable for use in space conditions.

Index Terms— aerospace electronics, mixed-signal ASICs, radiation hardening.

I. INTRODUCTION

The design of mixed-signal ASICs for space applications imposes knowledge of the response of integrated devices to the different types and levels of radiation that they may encounter during a given mission. While digital designs can tolerate TID induced voltage shifts or leakage currents within a wide range of total dose, the requirements of high-performance analog circuits translate into a reduced range of acceptable total dose, and parameter variations due to TID have to be incorporated in the form of larger design margins. Because foundries do not usually have information on the variation of device parameters with radiation, the establishment of a design methodology for space application mixed-signal ASICs has to begin with a careful radiation characterization of the chosen technology.

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IMSE-USE has selected the austriamicrosystems 0.35 μ m and is currently committed to a significant effort to evaluate its behaviour with radiation and at low temperatures.

One question that could arise is if it is justified to undertake the effort for characterization of a 0.35 μ m technology which by today's digital standards can be considered obsolete. There are a number of reasons to support the choice of such an "old-fashioned" technology. Analog designs do not require the small device dimensions that are essential for complex digital designs, as they use mostly transistors that are considerably larger and/or longer than the minimum dimensions offered by current technologies, as needed to get high performance devices (large transconductance, low-noise, device matching, large output impedance). The higher supply voltage of older technologies is also a bonus as it increases the dynamic range that can be achieved with a given circuit architecture. Long-term reliability is another aspect to consider; the degree of reliability required for missions that may last more than one decade in an aggressive radiation environment is more demanding than for short-lived, ground-level consumer products, and may not be sufficiently assessed for the most recent processes. With respect to obsolescence, 0.25-0.35 μ m technologies are widely used by the automotive industry and other high-reliability and long product-life applications. In those markets, foundries are often requested to maintain technologies available for time spans considerably longer than those required for consumer electronics.

The technology will be first applied in the design of ASICs for a mission to Mars. In this case, TID should not be a big concern as it is estimated to remain below 50 krad, but the effect of high-energy protons and ions has to be properly addressed in the design. Although not related to radiation effects, a further complication for designers comes from the fact that the devices will need to operate at temperatures of -110°C. Activities to characterize low-temperature behaviour, although not reported here, are being carried out in parallel with radiation measurements.

II. TECHNOLOGY EVALUATION

A multipurpose test chip (Fig. 1) has been designed, manufactured and characterized to obtain a preliminary experimental evaluation of the response to radiation (TID, SEE, latch-up), low-temperatures (down to -110°C), and the impact on device models of closed geometry transistors.

The chip contains transistor arrays of different geometries and sizes; resistors of all the types available in the technology; digital circuits (ring oscillators and shift-registers) for evaluation of SEE and latch-up; specific structures to verify the efficiency of guard rings to protect against latch-up; lateral and vertical bipolar devices; and two instantiations of a band-gap circuit, one with standard layout and another using radiation-hardened NMOS transistors.

Two levels of signal multiplexing are used for the characterization of the devices. One is internal to the test chip, to reduce the number of pins in the package; the second is external to the chip, using a reed-relay switch matrix. The chip design is easily reusable by replacement in the layout of the transistor arrays. It can handle up to 80 transistors grouped in five arrays of 4 x 4 transistors each. Fig. 2 shows a simplified schematic of one of the arrays. This arrangement makes possible to access the terminals of the 80 transistors using only 17 pins. The second multiplexing level is external to the chip: a custom-designed matrix

switch board, connected to a PC through an USB, manages the connections between a parameter analyzer and the DUT-board as well as the configuration bits needed to control the test chip.

The TID characterization setup uses a HP-IB controlled HP-4155 Semiconductor Parameter Analyzer. A PC controls the HP-IB and USB buses and generates the test sequence commands for characterization of all individual devices in the chip (CMOS transistors, bipolar transistors, resistors). A complete test takes 90 minutes to complete.

Four different transistor layout geometries have been used for NMOS transistors of thin- and thick-oxide: standard two-edged, annular, ringed-source, and dual-drain ringed-source [1, 2]. The characterization tests for each device makes measurements to extract the following parameters: V_{th} in saturation and linear regions, gain factor, mobility, body effect factor, saturation current and sub-threshold leakage current.

For measurements involving large currents, the parasitic resistance of the on-chip multiplexers has to be compensated. When small currents have to be measured, the ESD protection pads and the on-chip multiplexers contribute to parasitic leakage current. Dummy devices (open/short) are included in the arrays for compensation of those parasitic effects. Even so, the accuracy that can be achieved in the very low current ranges needed for characterization of leakage currents is limited by experimental errors and by the leakage currents flowing through devices placed in parallel with the DUT in the same column of the transistor arrays.

A. TID Measurements

The irradiation of the devices for evaluation of total dose effects has been carried out in the facilities of the Laboratorio de Radiofísica of the Universidad de Santiago de Compostela (Spain). The laboratory has a fully equipped Co-60 source, including dosimetry equipment to monitor the actual amount of radiation received by the samples. Achievable dose rates, which are controlled by changing the source-target distance, fall in a range of 40 rad/hr (0.012 rad/s) to 10 krad/hr (2.7 rad/s).

A one-day preliminary test, reaching 65 krad in four steps (5, 10, 20, 30 krad), was performed to quickly decide if the technology was robust enough to justify further testing. The results were promising, and a more detailed irradiation and measurement campaign was carried out over nine days. The experiment reached 350 krad in 8 steps, maintaining constant the irradiation time (~20 hours), and doubling the dose rate for each consecutive step. The dose rate was 70 rad/hr (0.019 rad/s) for the first step and 8960 rad/hr (2.5 rad/s) for the last step. During irradiation all CMOS transistors were biased for worst-case conditions, with their gate connected to the positive supply and all other terminals grounded. Four samples of the test chip were used for the TID tests. They were irradiated simultaneously during night-time (from 17:00 until 09:00), and during daytime, the samples were taken one-by-one out of their sockets in the irradiation board and measured in a thermal chamber held at a constant temperature of 25°C. During the time (90 minutes) needed to measure a sample, the other three continued to be irradiated. Each irradiation/measurement step thus took 24 hours to complete.

After irradiation, the parameters of the four irradiated samples have continued to be measured once a week, to monitor its evolution with time at room temperature. After six weeks, the samples have been annealed 168 hours at 100°C, the first half of that time unbiased, and the other half with the same worst-case bias used during irradiation.

B. SEE Measurements

SEE measurements have not yet been performed. A test board is being developed, and will be debugged using a Californium (Cf-252) source at the Centro Nacional de Aceleradores (Sevilla), before moving to the HIF facilities at the University of Louvain-la-Neuve for heavy-ion testing. SEE results should hopefully be available at the time of the conference.

III. RESULTS

The chosen technology offers two different gate-oxide options. Thin gate-oxide transistors (NMOS, PMOS) are limited to supply voltages below 3.3 V. The thick gate-oxide transistors (NMOSM, PMOSM) can be used with supply voltages up to 5 V.

A. Threshold Voltage Shift (V_{th})

For devices with thin gate-oxide (NMOS, PMOS), the average threshold voltage shift (ΔV_{th}), up to 350 krad, is small (less than 5 mV).

Thick gate oxide transistors (NMOSM, PMOSM) show a larger ΔV_{th} at a dose of 350 krad; an average of +140 mV for PMOSM, and -27 mV for NMOSM. There is little difference in ΔV_{th} between standard and enclosed layout transistors. However, ΔV_{th} is dependent on device dimension, smaller length and/or width giving larger changes in V_{th} (fig. 3).

B. Leakage Currents (SLEAK, ILDS)

The sub-threshold leakage current (SLEAK) is obtained as the linear intercept with the vertical axis of the $\log(I_{ds})$ vs. V_{gs} characteristic at maximum V_{ds} . For PMOS and PMOSM, radiation has a noticeable effect on narrow transistors, with SLEAK increasing by more than one order of magnitude at 350 krad. In wide PMOS transistors the effect is negligible. NMOS devices show a similar behaviour for narrow transistors, the SLEAK increase being smaller for enclosed layout geometries, and also for wide transistors. For wide and long NMOS transistors there is practically no increase in SLEAK at 350 krad, for either standard or enclosed layouts. Data for zero gate-bias drain-source leakage (ILDS) are more difficult to analyze because the increase of ILDS in one device affects all devices placed in parallel in the same array column. Post-processing permits to partially compensate the effect of paralleled devices, and confirms the efficiency to reduce leakage of enclosed layouts. Improved characterization of this aspect of the technology will be made on a new test chip, currently being designed, with arrays more specifically oriented to the evaluation of leakage.

C. Saturation Current (ISAT)

Changes in the saturation current (ISAT) are to be expected because it is affected by the changes in V_{th} and in carrier mobility. At 350 krad, ISAT shows an average decrease of 20% for PMOSM devices and 10% for PMOS transistors. Corresponding calculated changes in mobility are -8% and -3%. The average change of ISAT at 350 krad for N-channel transistors is negligible, in the order of +2% (NMOSM), and 1% (NMOS).

D. Bipolar Transistors

At 350 krad, bipolar transistors show degradation of beta: 25% for vertical PNPs and 50% for the lateral PNPs.

E. Resistors

There is an increase in the resistance of N-well and high-resistivity

poly devices, reaching approximately 6% for N-well and 1.5% for Hi-Poly at 350 krad.

F. Field-Oxide Leakage

Radiation-induced field oxide leakage could not be characterized, because of an error in the layout of the test structures. This error will be corrected in the next iteration of the test chip.

G. Annealing

Annealing of the samples was performed in three stages. In the first stage, samples were placed unbiased, at room temperature, and parametric measurements taken once a week during 35 days. In the second phase, samples were annealed unbiased at 100°C during 70 hours, and parameters measured at the end of that period. Finally, samples were annealed at 100°C, biased in the same conditions as during irradiation and the parameters measured after 90, 112, 133 and 157 cumulative hours. The most notable behaviour is seen once more in the NMOSM transistors. At the end of the annealing, short-channel NMOSM devices show a complete recovery of threshold drift with a slight rebound, and almost complete recovery from the increase of leakage currents (SLEAK and ILDS); but long-channel transistors, for which V_{th} drifted little during irradiation, present a strong rebound after annealing (fig. 4), stabilizing with a positive threshold shift of 50 mV. For PMOSM, the V_{th} drift recovery is only partial, the average ΔV_{th} value decreasing from 130 mV after irradiation to 100 mV after annealing.

IV. CONCLUSIONS

The results of the characterization carried out for the *austriamicrosystems* 0.35 μm CMOS technology indicate that, standard devices should work without problems up to 50 krad, and with proper use of RHBD techniques, it should be applicable to missions requiring TID up to 300 krad. Of course, such a statement has to be qualified taking into consideration the specific requirements of each design and the behaviour of the devices for different radiation levels. Circuit architectures will need to be adapted to cope with the parameter changes produced by radiation and temperature.

The SEE endurance still has to be assessed, but from reported use in other projects [4], it seems that the design of a RHBD digital library is mandatory to improve latchup resistance. IMSE is currently working in the design and evaluation of such a RHBD library.

Based on the experience obtained from the first test chip, a second iteration of the test ASIC is planned to improve the quality of the more critical measurements, and to cover gaps in transistors dimensions.

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REFERENCES

- [1] N. Nowlin, J. Bailey, B. Turfler, D. Alexander, "A Total-Dose Hardening-by-Design Approach for High-Speed Mixed-Signal CMOS Integrated Circuits", *Int. J. of High Speed Electronics and Systems*, Vol. 14-2, pp. 367-378, 2004
- [2] R. C. Laco, "Improving Integrated Circuit Performance Through the Application of Hardness-by-Design Methodology", *IEEE Trans. on Nuclear Science*, vol. 55, 2008.
- [3] R.C. Laco, J.V. Osborn, D.C. Mayer, S. Brown, and D.R. Hunt, "Total dose radiation tolerance of a commercial 0.35 μm CMOS process" 1998 IEEE Radiation Effects Data Workshop Record.
- [4] W. Magnes, M. Oberst, A. Valavanoglou, H. Hauer, C. Hagen, I. Jernej, H. Neubaer, W. Baumjohann, D. Pierce, J. Means, P. Falkner, "Highly Integrated Front-End Electronics for Spaceborne Fluxgate Sensors", in *Measurement Science and Technology*, IOP Publishing, Vol. 19, No. 11, 2008.

Fig. 1. Microphotograph of assembled test chip.

Fig. 2. Example of a transistor array. Columns are selected connecting the source and drain to the external SOURCE and DRAIN terminals. Row selection is made connecting the gates in a row to the external GATE terminal. RADIATE controls biasing during irradiation.

Fig. 3. V_{th} (linear region) vs. TID for thick gate-oxide (NMOSM) transistors of different sizes: short and narrow (triangles); short and wide (squares); long and wide (diamonds)

Fig. 4. V_{th} (linear region) vs. time for thick gate-oxide (NMOSM) transistors: short-channel (triangles); long-channel (squares). Irradiation between days 1 and 9. Annealing: days 9 to 44 at RT unbiased; 70 hours @100°C, unbiased, between days 47 and 55; 90/112/133/157 hours @100°C, worst-case bias, between days 55 and 70.