A 3.6mW @ 1.2V High Linear 8th-order CMOS Complex Filter for IEEE 802.15.4 Standard

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***Abstract*—This paper presents a fully differential 1.2V 8th-order inverter-based gm-C complex filter with 2.4MHz bandwidth and centered at 2.5MHz, designed in a 90nm CMOS process technology. Tuning is carried out through voltage controlled capacitors instead of transconductors, resulting in a significant improvement in terms of linearity. The filter presents attractive attributes in terms of power, IRR, SFDR, noise and selectivity, demonstrated by experimental measurements from a fabricated prototype.**

I. INTRODUCTION

Low-IF architectures are used in most of modern RF transceivers because they combine the advantages of both IF and zero-IF topologies while maintain a good compromise in terms of power dissipation, integration capability and complexity. However, the image problem arises in this kind of architecture: the action of mixing not only converts-down the desired band but also the image band placed symmetrically with respect the multiplying frequency (ω_{LO}). So, both the desired and the image band are superimposed in the same output band. This image signal is, with a traditional high IF architecture, sufficiently suppressed by filters in front of the mixer, but such filtering is not practical with a low-IF topology. A way to overcome the image problem in low-IF architectures is based on the use of complex or polyphase filters [1]-[3] as shown in Fig. 1. The RF signal is amplified and down-converted to IF with two mixers in quadrature. Channel selection and image rejection is performed by a complex filter.

As illustrated in Fig. 2, a complex band-pass filter centered at a given IF frequency (ω_{IF}) can be obtained by a frequency translation $s \rightarrow s{-}j\omega_{IF}$ from a low-pass prototype. In this way, the pass band is located at positive frequencies, while the negative frequencies are in the rejection band.

This paper presents a gm-C complex filter compliant with the requirements imposed in the IEEE 802.15.4 standard [4]. This application demands low voltage, low power and robust solutions under process variations accordingly to actual technologies and market pressure. The contributions of the paper are in these lines: an optimized 1.2V 8th-order inverter-based

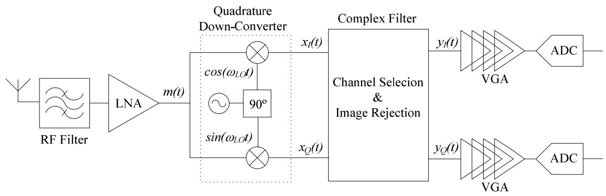

Figure 1. Typical Low-IF architecture with quadrature down-conversion

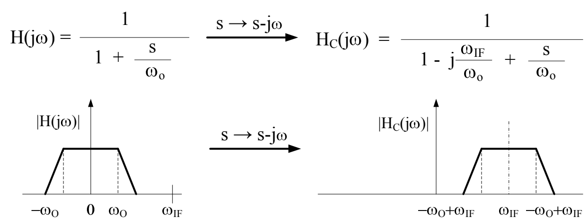

Figure 2. Ilustration of pole shifting in the complex domain

complex filter centered at 2.5MHz in a 90nm CMOS technology with high performance in terms of power, linearity and noise. Moreover, tuning is performed throughout varactors instead of the gm´s, as usually done, leading to significant improvements in terms of linearity.

The paper is organized as follows. Section II describes the filter synthesis and design accordingly to the specifications. Experimental results are presented in Section III. Finally, conclusions are given in Section IV.

II. COMPLEX FILTER IMPLEMENTATION

A. High Level Synthesis

In order to comply with the IEEE 802.15.4 specifications [4], the filter should exhibit a channel bandwidth of 2.4MHz (including 200kHz of frequency offset). Accordingly, an IF slightly larger (2.5MHz) has been chosen. The filter should reject interferers in adjacent (5MHz) and alternative channels (>7.5MHz) with minimum attenuation of 0dB and 30dB respectively (it also applies to image rejection). For convenience in our particular receiver, a gain around 10dB is also specified.

One of the goals is to find a transfer function of the LP prototype suited to low power and robust operation. From this point of view, the following issues are desirable: a) A reduced order to minimize the number of active elements. b) Low quality factors to avoid the need of Q-tuning while reducing the spread and noise. c) Minimum in-band group delay variation to avoid inter-symbol distortion in the receiver.

It can be shown that a 4^{th}-order all pole transfer function with the pole locations and quality factors in Table I accomplishes with the needs for the LP filter with certain security margins. The block-diagram of the implemented complete 8^{th}-order complex filter is shown in Fig. 3(a). A pre-amplifier block provides gain and accommodates the input common-mode voltage bias for the next sections. The rest of the filter has been built as a cascade of 2^{nd}-order transfer functions using the basic structure described in Fig. 3(b). Sections have been ordered in increasing pole quality factor for dynamic range and noise considerations. Table II shows the required parameters value for the low-pass filter, while the value of the necessary crossing transconductors for complex operation at 2.5MHz are given in Table III.

TABLE I. POLES LOCATION AND QUALITY FACTORS OF THE SYNTHESIZED LP PROTOYPE

Frequency	Quality Factor
0.9471MHz	0.6188
1.3839MHz	2.1829

TABLE II. PARAMETERS VALUE FOR 2^{ND}-ORDER SECTION STRUCTURES

Section	gm_1 (μA/V)	gm_2 (μA/V)	gm_3 (μA/V)	gm_4 (μA/V)	C_1 (pF)	C_2 (pF)
1	200	100	50	50	10.4	6.8
2	100	50	100	100	12.5	10.5

TABLE III. PARAMETERS VALUE OF CROSSING TRANSCONDUCTOR

gm_A (μA/V)	gm_B (μA/V)	gm_C (μA/V)	gm_D (μA/V)
163.2	197.3	106.6	165.4

B. The Transconductor

The transconductor should display a large enough linear range while working at low power supply voltage, satisfying the voltage headroom constraints imposed by the process. Under these circumstances, CMOS fully differential inverter-based transconductors has been demonstrated very suited for this purpose [5]-[7]. The most popular of these transconductors was proposed by Nauta in [5]. But despite of its attractive features, it has important limitations for bandpass and complex filters realization as demonstrated in [6]. Namely, and in the context of complex filters, design conflicts appear to maintain enough high quality factor of resonators generating the complex filter from the low-pass prototype, enough high DC gain of integrators and robustness not only to process and temperature variations but also to different loading conditions at each node (common mode gain depends on the loading conditions).

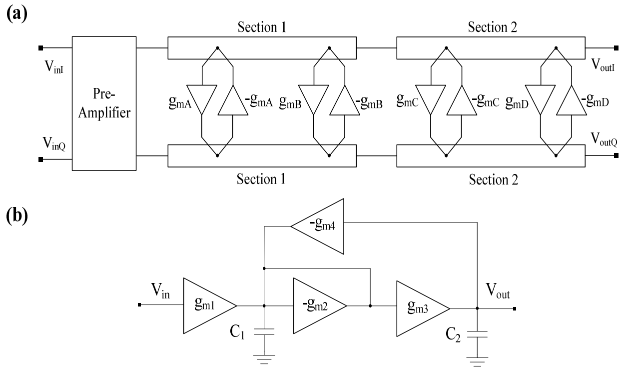

Figure 3. (a) Block diagram of the implemented filter (b) 2^{nd}-order section structure. (Single-ended versions shown for simplicity)

We decided to use the alternative topology shown in Fig. 4 [7]. Inverters I_1 and I_2 are responsible for generating the transconductance while inverters I_3-I_8 guarantee the common-mode stability; the common mode voltage is self-established to the quiescent point of the inverters. The effective differential transconductance is similar to the Nauta´s topology. As long as all transistors work in the saturation region, the stage delivers a transconductance that is linearly proportional to V_{dd}. However, it offers better common-mode stability, less output parasitic capacitance and smaller output parasitic conductance than Nauta´s transcondudtor. In other words, the implemented transconductor allows larger design margins with respect to the Nauta´s topology. In addition, it also works in voltage mode, and hence we also use it in the pre-amplifier.

The transconductors have been built by parallel connections of a unitary transconductor of 50μA/V (or slightly modified for the case of non-integer multiple). The size of transistors is: $(W/L)_p$=2.32μm/4.0μm, $(W/L)_n$=1.16μm/4.0μm. This way, good device matching and low parasitic output conductance are guaranteed (at all process corners) while the bias point is set around $V_{dd}/2$ (typical case).

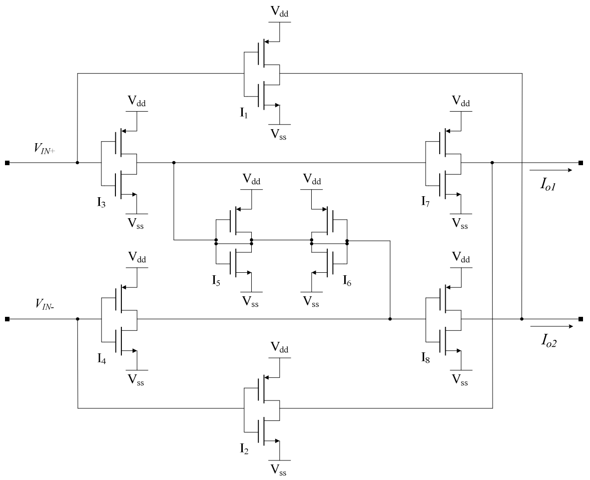

Figure 4. Schematic of the implemented transconductor

C. Tuning

This kind of filters requires, in general, a tuning strategy in terms of poles frequency (f-tuning) and quality factor (Q-tuning) in order to compensate process and temperature variations, aging effects, etc. However, the present application corresponds to a low frequency (2.5MHz) and low-Q (~2 max.) case. It together the long channel transistors used avoid the need of Q-tuning, thus limiting the tuning requirements to frequency. Because the operation is based on *gm/C* ratios, the tuning consists on setting the correct master *gm/C* ratio using a signal generated from a circuit loop controlled by an external (known) reference [5]. At this point, we are not interested on the tuning circuitry itself but in the way to perform such tuning. Because the transconductance of the implemented transconductor is strongly and linearly determined by the voltage V_{dd}, traditional tuning schemes [5] are based on regulating V_{dd} (V_{dd} is not in this case the general supply voltage of the system). But at the same time, the said strong dependency has an important drawback; the unavoidable ripple in the generated V_{dd} modulates the transconductance and hence, the transfers function of the filter. This intermodulation deteriorates both image band rejection and stop-band attenuation. For this reason, this strategy requires extreme care on the design of the tuning circuitry to minimize the ripple.

Another possibility is to realize the tuning through the capacitors. In [8], authors proposed the use of binary weighted digitally programmable capacitor arrays (DPCAs). It has the advantage that the *gm/C* ratio remains constant (no ripple) in the presence of temperature and process variations. However, this solution increases the complexity of the design while only allows a discrete-wise tuning. Moreover, the obtained performance is limited by the bit-length/accuracy of the ADCs and capacitors spread and matching.

The option we propose is to maintain the gm`s fixed and to use voltage controlled capacitors (varactors) for tuning purpose. They can provide continuous tuning, avoiding the need of DACs and DPCAs, while their limited dependency of the capacitance with respect to the voltage control can be successfully exploited to reduce the modulation of the transfer function due to the ripple in the voltage control. The goal is to be able to tune the circuit with the minimum amount of varactors as possible to avoid problems derived from their inherent non-linearity. In our design, we composed the capacitors by 70% of fixed capacitance (MIM) and 30% of varactors (MOS accumulation). The nominal value of the voltage control for the varactor has been set at $V_{dd}/2$. Fig. 5 shows the results from Montecarlo simulations demonstrating that the filter can be properly tuned with a certain margin in all process and temperature corners.

III. EXPERIMENTAL RESULTS

The design was fabricated in TSMC 90nm CMOS process. The microphotograph is shown in Fig. 6. The die size is 682x656μm^2. The filter frequency characteristics have been extracted in the lab using a Tektronix AFG320 signal generator and the spectrum analyzer HP3589A.

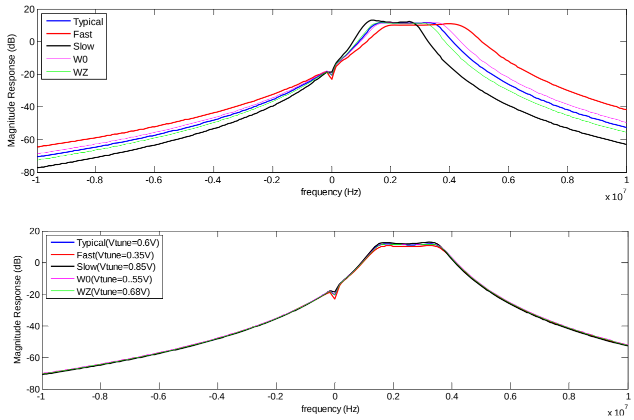

Figure 5. Complex transfer function of the filter before (top) and after tuning (bottom) for all corners process

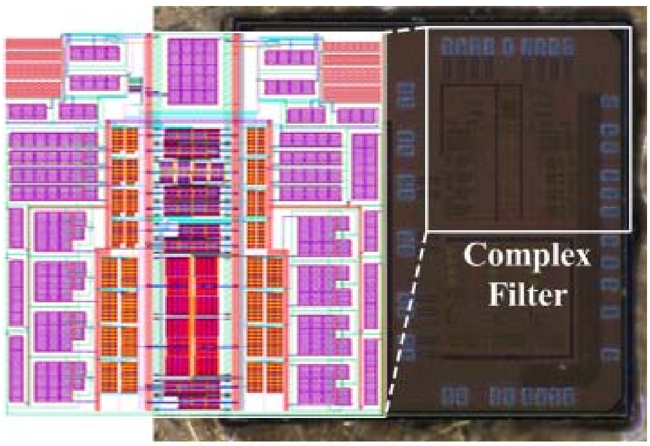

Figure 6. Microphotograph and layout of the complex filter

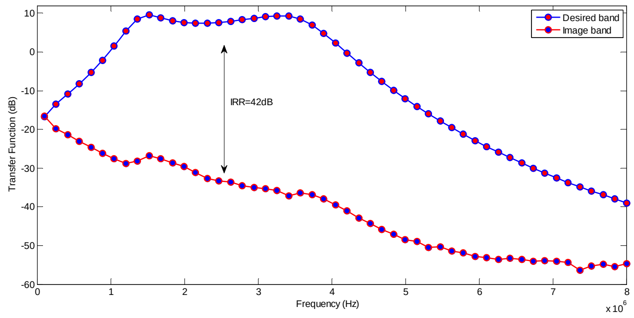

Figure 7. Measured frequency response at signal and image sides

Fig. 7 shows the filter frequency response for the signal and image sides. The image rejection ratio at 2.5MHz is 42dB which is enough for IEEE 802.15.4 specifications. The attenuation at first- and second- adjacent channels is 43.5dB and more than 55dB respectively. The filter presents a very good linearity performance. The in-band Spurious-Free Dynamic Range (SFDR) is 52.7dB. The SFDR is, respectively, 61dB and 68dB in the presence of strong blockers in the first- and second- adjacent channel. The in-band IIP_3 around the center frequency (2.5MHz) was 15.2dBm (@ 50Ω). The total input referred noise integrated over a 2.4MHz band is 44.9μV_{rms} and the pass-band gain is 9dB. Finally, the in-band group delay variation is less than 300ns, which is low enough not to cause inter-symbol distortion problems in the receiver. Table IV shows the main measurements and compares them with other similar approaches in the literature.

The intermodulation noise through the varactors and transconductors has been evaluated in the lab by measuring the third order intermodulation power at the output (IM_3). For that, a ripple (sinusoid) with different amplitudes (up to 250mV) has been injected through V_{dd} and the control voltage of the varactors. The results are shown in Fig. 8. As can be seen, IM_3 power is maintained around 20dBm below in the case of the varactors, thus corroborating the expected improvement of the linearity of the complete complex filter.

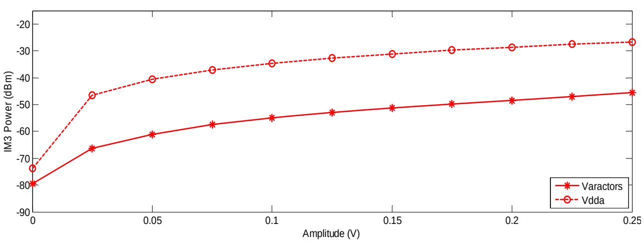

Figure 8. Comparison of Output power of the third order intermodulation (IM3) when a ripple is injected in the supply voltage (V_{dd}) and the voltage control of the varactors

TABLE IV. FILTER´S PERFORMANCE AND COMPARISON WITH OTHER WORKS

Parameter	**This work**	**[2]**	**[6]**	**[3]**
Technology	90nm	130nm	0.35μm	0.35μm
Voltage Supply	1.2V	1.2V	2.3V	2.7v
Power Consumption	3.6mW	10.8mW*	7.36mW	12.69mW
Center Freq.	2.5MHz	2 MHz	3MHz	2MHz
Order	8^{th}	14^{th}	14^{th}	12^{th}
Bandwidth	2.4MHz	1.5MHz	1MHz	1MHz
Gain	9dB	0dB	0dB	15dB
Suppression (1^{st} adj.ch.)	43.5dB	50dB	40dB	29dB
IRR	42dB	55dB	53dB	45dB
Input Ref. Noise	44.9μVrms (B_W=2.4MHz)	-	170μVrms (B_W=2MHz)	29μVrms (B_W=2MHz)
SFDR (in-band)	52.7dB	55dB	52dB	45.2dB
SFDR (near blocker)	61dB (@7.5MHz)	60dB	59dB	61dB
SFDR (distant blocker)	68dB (@12MHz)	-	62dB	
Size	682x656μm^2	1.2x1mm^2	680x550μm^2	1.6x0.8mm^2

** Power consumption of tuning circuit is included*

IV. CONCLUSIONS

A fully differential 1.2V 8th-order inverter-based gm-C complex filter with 2.4MHz bandwidth and centered at 2.5MHz has been developed in a 90nm with MIM capacitors CMOS process, being compliant with the requirements of the IEEE802.15.4 standard. Traditionally, tuning of this kind of filters is performed through the voltage supply (V_{dd}) of the transconductors. However, we propose in this work to maintain V_{dd} fixed and to realize the tuning through the control voltage of varactors. For that, capacitors in the filter are composed of 70% of fixed MIM capacitors and 30% of varactors.

Experimental results from the lab demonstrate the feasibility of the new proposed tuning strategy, resulting in a significant improvement in terms of linearity, while relaxing the complexity of the tuning circuitry. The main obtained experimental results for the complete 8^{th}-order complex filter are: nominal gain of 9dB, good selectivity (> 40dB adj. channel), high image rejection (42dB), low power consumption (3.6mW@1.2V) and low noise (44.9μV_{rms} total input referred noise). The in-band SFDR is 52.7dB, and 61dB and 68dB in the presence of strong blockers in the first- and second- adjacent channel respectively. The in-band IIP_3 around the center frequency (2.5MHz) was 15.2dBm (@ 50Ω). A significant improvement of 20dB in terms of IM3 is achieved by the tuning strategy through the varactors.

ACKNOWLEDGMENT

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REFERENCES

[1] J. Crols and M. Steyaert, "An Analogue Integrated Polyphase Filter for High Performance Low-IF Receiver," *Proc. of the VLSI Symposium*, pp. 87-88, Kyoto, Japan, 1995.

[2] Seyeob Kim, Minsu Jeong, Yanggyun Kim, Bonkee Kim, Taeju Lee, Kangho Lee and Bo-Eun Kim, "A Complex Band-Pass Filter for Low-IF Conversion DAB/T-DMB Tuner with I/Q Mismatch Calibration," *Procs. of IEEE Asian Solid-State Circuits Conference*, pp.473-476, November 2008.

[3] Ahmed A. Emira and Edgar Sánchez-Sinencio, "A Pseudo Differential Complex Filter for Bluetooth With Frequency Tuning*," IEEE Trans. on Circs. and Systems—II: Analog and Digital Signal Proccesing*, vol. 50, no. 10, October 2003.

[4] Wireless Medium Access control (MAC) and Physical Layer (PHY) Specifications for Low-Rate Wireless Personal Area Network (LRWPANs), IEEE 802.15.4, 2003.

[5] B. Nauta, "A CMOS Transconductance-C Filter Technique for very High Frequencies," *IEEE Journal of Solid-State Circuits*, vol.27, no.2, February 1992.

[6] P. Andreani and S.Mattisson, "On the use of Nauta´s Transconductor in Low Frequency CMOS gm-C Bandpass Filters," *IEEE Journal of Solid-State Circuits*, vol.37, no. 2, February 2002..

[7] H. Barthélemy, S.Meillère, J.Gaubert, N.Dehaes and S.Bourdel, "OTA based on CMOS inverters and application in the design of tunable bandpass filter," *Springer Analog Integr Circ Sig Process* (2008), vol. 57, pp. 169-178.

[8] Gang Chen, Zhiqun Li, HaiYong Su, Li Zhang and Wei Li, "A 5th-Order Chebyshev Active RC ComplexFilter with Automatic Frequency Tuning forWireless Sensor Networks Application*," Proceedings of International Symposium on Signals, Systems and Electronics (ISSSE)*, pp. 1-4, September 2010.