Silicon nanowire circuits fabricated by AFM oxidation nanolithography

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Abstract

We report a top-down process for the fabrication of single-crystalline silicon nanowire circuits and devices. Local oxidation nanolithography is applied to define very narrow oxide masks on top of a silicon-on-insulator substrate. In a plasma etching, the nano-oxide mask generates a nanowire with a rectangular section. The nanowire width coincides with the lateral size of the mask. In this way, uniform and well-defined transistors with channel widths in the 10-20 nm range have been fabricated. The nanowires can be positioned with sub-100 nm lateral accuracy. The transistors exhibit an on/off current ratio of 10^5. The atomic force microscope nanolithography offers full control of the nanowire's shape from straight to circular or a combination of them. It also enables the integration of several nanowires within the same circuit. The nanowire transistors have been applied to detect immunological processes.

1. Introduction

Silicon nanowires with high surface-to-volume ratio are the building blocks of novel and highly sensitive devices such as label-free biosensors [1-6], chemical sensors [7, 8] or electromechanical resonators [9] among other applications [10, 11]. The fabrication of Si nanowires (SiNWs) is either achieved by bottom-up or top-down approaches. Bottom-up methods are based on a catalyst-assisted growth [2, 12]. Those methods are able to generate nanowires of very small diameter, say below 5 nm, however, bottom-up methods have to contend with the positioning of the nanowires in a predetermined position of a complex device. This, in turns, limits the integration capabilities bottom-up methods. Top-down approaches are based on the use of lithography such as electron beam lithography [4, 13, 14], nanoimprint [7] or atomic force microscopy lithography [15, 16] to fabricate the SiNWs. Some of the top-down lithographies can position the nanowire with sub-100 nm accuracy. However, reliable fabrication of nanowires with diameters below 50 nm is challenging. This, in turns, limits the sensitivity of the devices fabricated by top-down approaches. Herein, we report an atomic force microscope-based nanolithography that accomplishes the fabrication of silicon nanowires devices with sub-20 nm channel widths and, at the same time, the nanolithography has the ability to position the SiNWs with sub-100 nm accuracy. The small channel width of the nanowires enables their use to detect immunological interactions. The high spatial resolution of the atomic force microscope (AFM) enables to integrate several nanowires within the same circuit lay out. The shape of the nanowires on a flat surface is easily controlled, thus, straight or circular nanowires are fabricated. In addition, the method is compatible with complementary metal oxide semiconductor technology (CMOS).

2. Experimental methods.

AFM oxidation nanolithography is a robust and flexible tip-based nanofabrication method [17-22] that has been used to fabricate templates for the growth of single molecule magnets [23], resist masks [24], nanomechanical resonators [25, 26], nanoelectronic devices [16, 27-29]. Furthermore, it can also be upscaled for large-scale patterning by using stamps [30-34]. The throughput is controlled by the AFM electronics, nonetheless, its flexibility enables the reproducible fabrication of single-crystalline SiNWs field effect transistors (FET) with sub-20 nm channel widths and their integration into complex circuits. Furthermore, the electrical properties of the SiNWs can be controlled by changing either the size or the doping concentration.

In this work, Silicon-On-Insulator (SOI) substrates have been used as substrates for the fabrication of SiNW-FETs. Some devices are fabricated on SOI substrates with 150 nm thick active layer (Si (100)) on top of a 100 nm buried oxide layer (both nominal values) purchased from University Wafer, MA, USA. The active layer has a resistivity ρ of 10-20 Ωcm. Other devices are fabricated on SOI wafer with a 57 nm active layer and a 100 nm buried oxide layer (IBIS Technology, MA, USA). Phosphorus was implanted to achieve a resistivity of 0.01-0.025 Ω cm. The SOI

substrates were cleaned by three sonication cycles in $NH_4OH/H_2O_2/H_2O$ (1:1:2) for 12 min each, then sonicated in deionized water (5 min) and blown dry in N_2.

Local oxidation nanolithography of the SOI substrates, was performed with an amplitude modulation atomic force microscope operated in the low amplitude solution (noncontact or attractive regime [21]). Figure 1 illustrates the experimental AFM set-up to fabricate SiNWs. The AFM base and optical head was placed into an inner box where temperature and relative humidity are controlled where temperature and relative humidity are controlled, respectively, in the 24-27% C and 50-70%. (Figure 1 (a)). Relative humidity values around 50% favor the field-induced formation of a water meniscus between the tip and the silicon surface [17, 19]. Doped n-type silicon cantilevers (Nanosensors, Germany) with k=42 N/m and resonant frequency of 320 kHz were used. To fabricate the silicon dioxide nanomasks a sequence of voltage pulses is applied between the AFM silicon probe and the SOI substrate (Figure 1 (b)). Typical voltage pulses are about 36 V (tip negative) for 100 μs. The formation of nanometer-size water bridges is monitored by following the instantaneous motion of the AFM tip in an oscilloscope (Figure 1 (c)). Before the application of a voltage pulse, the tip oscillates above the sample surface (I). The electrostatic interaction deflects the tip's equilibrium position and changes the AFM resonant frequency, which leads to a reduction of the oscillation amplitude (II). Once the pulse is off, the oscillation amplitude remains reduced because the capillary force of the water meniscus (III). Finally, the tip is retracted and the oscillation recovers its initial amplitude (IV). A continuous SiO_2 line is obtained when the size of the individual dots is larger than the lateral distance between pulses. This SiO_2 nanomask is used to define the size of the SiNW.

The unmasked silicon layer was removed by either wet or dry chemical etching procedures. The wet etching was performed at 50 °C with a dilute solution of KOH in deionized water (20%). To remove the unmasked silicon takes about 2 s. The dry etching was performed by reactive ion etching (RIE) with a plasma containing a gas mixture of 80% SF_6 and 20% O_2 (Oxford Instruments, U.K.). The etching time is about 4 s.

Finally, the SiNWs are contacted to micrometer size platinum source and drain contacts by either photolithography or electron beam lithography. After metallization, the sample was annealed for 30 minutes at 500ºC to improve the electrical properties of the contacts [1]. Those annealing conditions favor the formation of an ohmic contact between the nanowire and the metallic contact. Typical thickness for the metallization process is 90 nm of Pt on top of 10 nm of Ti. The electrical characterization of the devices is performed with a Station Probe (Karl Suss) and a HP4145B semiconductor parameter analyzer. The gate electrode is placed on the back side of the SOI wafer.

3. Discussion.

Figure 2 shows a SiNW with 4 μm in length and 9.5 nm in width. The SiNW bridges two platinum electrodes. Figure 2 (a) shows the silicon oxide mask. The thickness of the fabricated mask is about 3 nm. Figure 2 (b) shows the nanowire and a small section of both source and drain electrodes. The unmasked silicon has been etched by reactive ion etching (RIE). The apparent height of the nanowire is of 48.8 nm. This

value is directly obtained from the AFM image (Figure 2 (c)). The height is mainly controlled by the thickness of the device layer (~57 nm) and the RIE exposure time.

To accurately determine the nanowire channel width from the AFM image we have used image reconstruction methods [35]. The AFM image shows a nanowire with a trapezoidal cross-section with top and bottom apparent widths, respectively, of 9.3 and 49.7 nm. The top width is controlled by the AFM lithography while the bottom width represents the dilation introduced by the tip size. The silicon tip used to image the nanowire has an apex radius of about 5 nm and a half-cone angle of 22°. The angle formed between the sidewall of the tip and the substrate baseline is 68°. This value is almost identical to the angle measured between the nanowire sidewall at its base (67.5°) in the unreconstructed AFM image. This coincidence can only be explained if the AFM image is the result of the convolution of a conical tip of half angle 22.5° and a rectangular nanowire of a lateral size of 9.5 nm (Figure 2 (d)). This result is also supported by the agreement reached between the measured and the nominal resistivities of the SiNW (see below). Furthermore, the observation that the plasma etching conditions used here generates structures with vertical sidewalls is consistent with the above image reconstruction. The resulting SiNW has a section equivalent to that of a cylindrical wire of 12 nm in radius.

The electrical response of the SiNW is characterized by applying a bias between the platinum electrodes (Figure 2 (e)). At low voltages the nanowire has a linear ohmic behaviour. The total resistance of the device R_t = 2.5 MΩ can be obtained from the slope of curve. The total resistance includes the contact resistance between the nanowire and the platinum electrodes (R_{ci}), the resistance of the external circuit (R_{ext}) and the nanowire resistance (R_{nw})

$$R_t = R_{c1} + R_{c2} + R_{nw} + R_{ext} \tag{1}$$

An estimation of R_{NW} is obtained from Ohm's law and the bulk resistivity of the SOI wafer (ρ = 0.01-0.025 Ω cm) and the size of the nanowire. By applying Ohms' law

$$R_{nw} = \rho \frac{L}{A} \tag{2}$$

we obtain a maximum value of R_{nw}=2.3 MΩ (L= 4.2 μm and A= 456 nm^2). Thus, we find a good agreement between theoretical (Ohms' law) and experimental values. Two conclusions can be inferred from the above result. First, it indicates that the contact and external resistances are negligible with respect to the resistance of the nanowire. Consequently, the electrical response is controlled by the characteristics of the nanowire. Second, the nanofabrication process preserves the properties electrical properties of the active crystalline silicon layer that serves as the raw material for the fabrication of the SiNW.

The fabricated SiNW is the main element of a field effect transistor (FET) transistor by introducing a gate electrode. Here, the gate electrode is situated in the back side of a silicon-on-insulator (SOI) wafer. The output and transfer characteristics of the transistor formed with the SiNW described above are shown in Figures 3 (b), (c). The output curve shows a clear dependence on the gate voltage. The off state drain leakage

is about 10^{-11} A. On the other hand, this SiNW transistor has an on/off current ratio of 10^5.

The SiNW FET fabrication process enables to control the nanowire size, which in turns controls the electrical response of the transistors. The channel width is controlled by the width of the local oxide mask and the method used to etch away the unmasked silicon (Figure 3). The height is controlled by the thickness of the active SOI layer and the exposure etching time. Figure 3 (a) shows the cross-section of two SiNWs after wet and dry etching. The active Si layer of the SiNW exposed to KOH was 150 nm (ρ= 10-20 Ωcm) while the one exposed to plasma etching was 57 nm (ρ= 0.01-0.025 Ωcm). In both cases the buried silicon dioxide thickness was 100 nm. Although the local oxide mask was similar (~10 nm), the final width is highly dependent on the etching method. Plasma etching produces features with vertical sidewalls and a rectangular cross-section, hence the minimum lateral size of the SiNW is determined by the lateral size of the nanomask. On the other hand, etching in KOH generates SiNWs with a trapezoidal cross-section that heavily reflects the strong etching rate dependence on the Si face. The silicon etching rate in a 20% KOH solution at 50ºC is, respectively, 1.5μm/min and 4 nm/min for Si (100) and Si (111). A trapezoidal shape limits the minimum SiNW lateral size (Figure 3 (a)).

The doping concentration of the active Si layer of the SOI wafer is another factor that controls the electrical response of the SiNW transistor. This is illustrated in Figures 3 (c) where the output characteristics of the SiNW shown in Figure 3 (a) are almost identical in spite of the different size. The higher doping concentration of the smaller nanowire counter balances the differences in size. The implantation of higher doping doses in the SOI used for the fabrication of SiNW transistors results in obtaining SiNW with a higher concentration of dopants and, consequently, with a better electrical response. Finally, the electrical output of the nanowire depends mainly on the resistivity of the nanowire. So, by a doping implantation is possible to change at will the expected electrical response of SiNW devices fabricated using this method.

The top and sidewalls of the SiNW are left exposed to the environment. Thus, the electric fields associated with chemical or ligand-receptor processes occurring in the exposed regions of the nanowire could alter the carrier distribution within the nanowire. Preliminary results about the sensing capabilities of the fabricated SiNWs to detect immunological activity are illustrated in Figure 4. First, the current as a function of the voltage is measured in the presence of the water at pH=7. The water serves as the buffer solution. In this way we avoid unwanted electrochemical processes that might be associated with the presence of salts in physiological buffers [36]. This curve is taken as the reference curve. Then, the SiNW is exposed to a 1 μg/ml solution containing bovine serum albumin antigens (BSA). The curve coincides with the one obtained in the absence of BSA. Finally, the SiNW coated with BSA is exposed to a 1 μg/ml solution containing antiBSA. A significant change, well above the experimental noise, is observed in the current. In particular, at V_{DS}=0.3 V the current goes from 1.42 nA to 1.6 nA when the BSA molecules adsorbed on the nanowire surface are exposed to the antiBSA solution. A similar change is not observed when the nanowire is exposed to a solution with a different antibody. We conclude that the change observed in the current is attributed to the formation of an analyte-ligand complex. Thus, the devices fabricated by the AFM nanolithography preserves the high sensitivity shown by the SiNW devices fabricated by bottom-up methods.

Sub-100 nm positioning accuracy in the fabrication the SiNWs is readily obtained by using an AFM implemented with a high resolution closed-loop scanner (N-point, Madison, USA). The high spatial resolution of the AFM enables a precise positioning of the tip to initiate the nanolithography process. Thus, it is possible to integrate different sub-20 nm SiNWs in the same circuit layout such as the one indicated in Figure 5. The figure also illustrates the flexibility of AFM oxidation nanolithography to fabricate single-crystalline silicon nanowires of arbitrary geometry. The different nanowire designs show that local oxidation nanolithography is compatible with multiple oxidation processes on the same circuit. The compatibility with the two successive oxidations enables the fabrication of complex nanoscale devices.

5. Conclusions

We have developed a reliable and highly controllable top-down process for the fabrication of single-crystalline silicon nanowire circuits and devices. AFM oxidation nanolithography defines very narrow oxide masks on top of a silicon-on-insulator substrate. In a plasma etching, the nano-oxide mask generates a nanowire with a rectangular section, where the top side coincides with the lateral size of the mask. Uniform and well-defined SiNW transistors with sub-10 nm channel widths and a variable length from hundred of nanometers to several micrometers have been obtained. The SiNW transistors exhibit an on/off current ratio of 10^5. The nanowires can be positioned with sub-100 nm lateral accuracy. The nanolithography offers full control of the nanowire‘s shape from straight to circular. The AFM nanolithography is compatible with standard CMOS processing which enables the integration of several nanowires within the same circuit. The nanowire transistors have shown their ability to detect immunological processes.

Acknowledgments

This work was financially supported by the MICINN (Spain) (MAT2009-08650), the CSIC (Transbio, PIF08-008 and the Comunidad de Madrid (NanoObjetos, S2009/MAT-1467). The doping implantation has been performed in the ICTS clean room facility (IMB-CNM-CSIC).

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Figure Captions

Figure 1. AFM oxidation nanolithography experimental set-up and scheme of the patterning process. (a) The AFM is enclosed in a chamber where both temperature (T) and relative humidity (RH) are controlled and monitored. (b) Scheme of the nanopatterning process. (c) Dynamics of the tip's oscillation (deflection) before (I), during (II), and after the application of a voltage pulse (III, IV) in controlled environment at T=27˚C and RH=65%. Each dot represents an instantaneous value of the deflection. Once the pulse is off, the capillary force of the water meniscus damps the oscillation (III). Reestablishing the feedback loop breaks the meniscus (IV). The red line represents the voltage pulse.

Figure 2. (a) AFM image of a SiO_2 pattern to be used as mask. (b) AFM image of a SiNW connected to platinum electrodes. (c) High resolution image of the of the SiNW shown in (b). (d) Cross-section of the region marked in c. (e) I-V characteristics of the nanowire at low voltages. (f) Output (left) and transfer (right) characteristics of the SiNW transistor.

Figure 3. (a) The etching method defines the final geometry of the SiNW. Wet etching (KOH solution) produces a SiNW with a trapezoidal cross-section. Plasma etching (RIE) generates a SiNW with a rectangular cross-section. (b) Output characteristics of the SiNW obtained after KOH etching. (c) Output characteristics of the SiNW obtained after plasma etching. The active layer of the SOI is 100 nm and 60 nm, respectively, for wet and plasma etching.

Figure 4. Dependence of the SiNW sensing response with the environment. Three situations are studied: water (black), water and BSA molecules (grey) and, water, BSA and BSA antibodies (blue). Significant changes in the current are observed in the presence of complementary antigen-antibody interactions.

Figure 5. Scheme of the flexibility of AFM oxidation nanolithography to fabricate sub-20 nm nanowires of different geometries. The images of the SiNWs have been obtained by AFM. The image of the circuit has been obtained by optical microscopy. Scale bar in the AFM images of 100 nm.

Figure 1

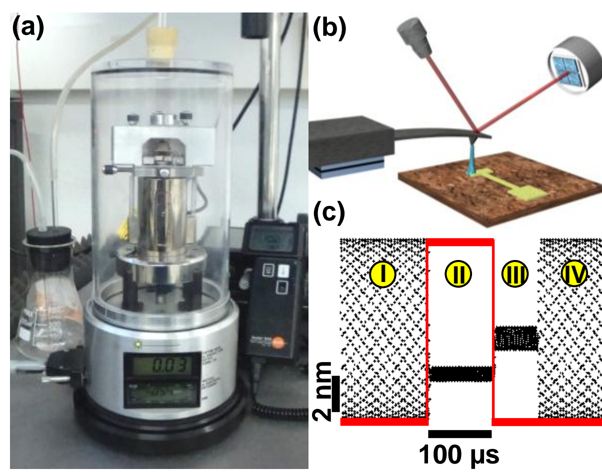

Figure 2

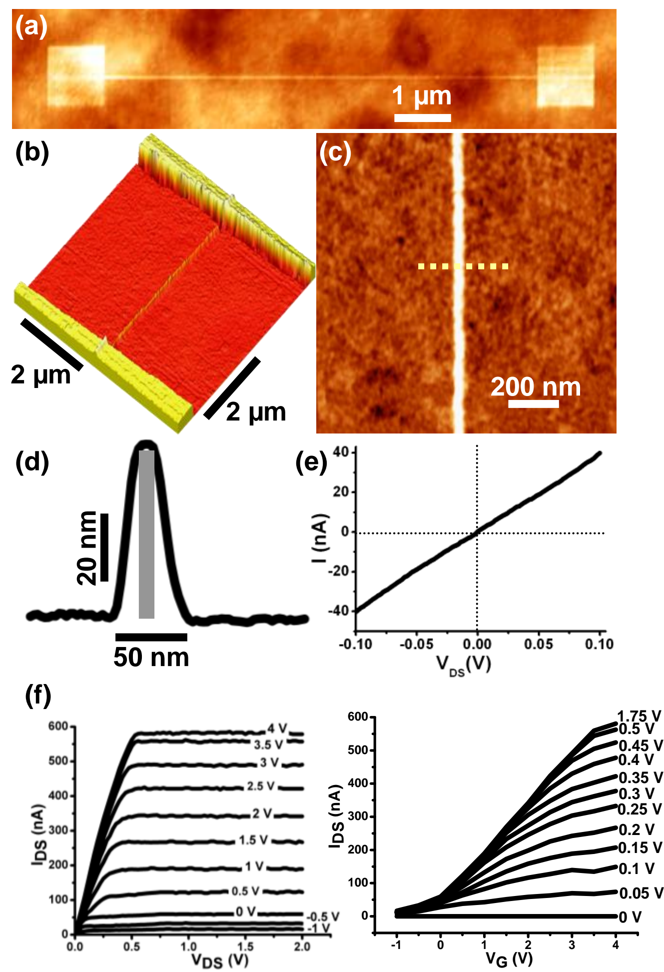

Figure 3

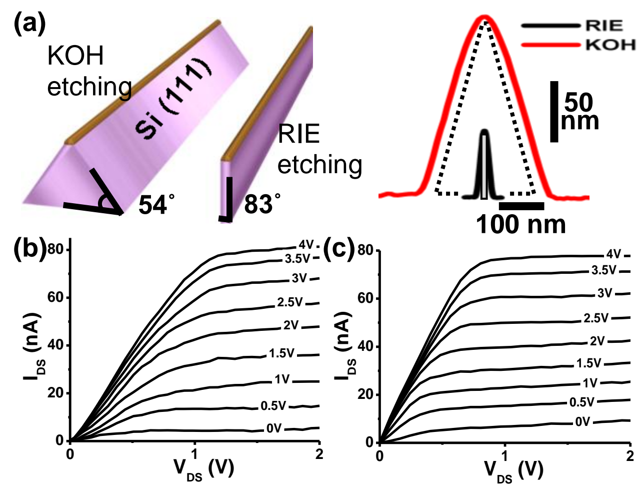

Figure 4

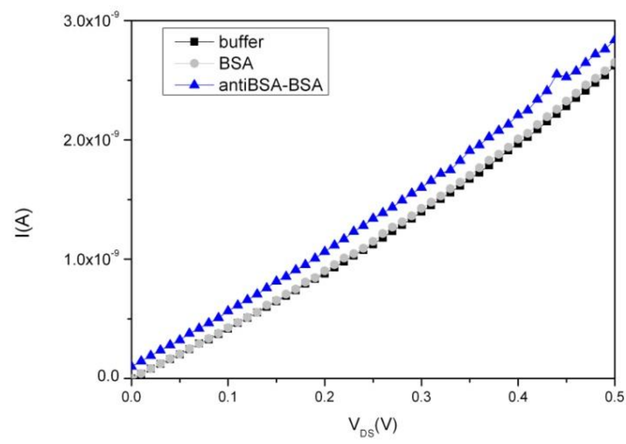

Figure 5