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Simulation of electrical parameters of new design of SLHC silicon sensors for large radii

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Abstract

As a result of the high luminosity phase of the SLHC, for CMS a tracking system with very high granularity is mandatory and the sensors will have to withstand an extreme radiation environment of up to 10^{16} part/ 2 . On this basis, a new geometry with silicon short strip sensors (strixels) is proposed. To understand their performances, test geometries are developed whose parameters can be verified and optimized using simulation of semiconductor structures. We have used the TCAD-ISE (SYNOPTIS package) software in order to simulate the main electrical parameters of different strip geometries, for p-in-n type wafers.

1) Introduction

After LHC upgrade, the CMS tracking system will have to cope with much higher radiation level and occupancy due to increasing number of emerging particles and higher tracks densities. The Central Tracker will have to be replaced, with an increase in area of pixel detectors and using shorter strips (strixels) for large radii of the tracker. We describe the test structure proposed by our collaboration as a first attempt to find the optimum strixel geometry. We used simulation package ISE-TCAD to evaluate electrical parameters for several geometries.

2) Test Structure

The test structure proposed [1] consists of two types of strips, as shown in Fig.1. Near Strips are p+ implants only under the near (bias) half of each strixel and is connected to the bias ring with a short polysilicon resistor. Far Strips are p+ implants only under the far half of each strixel and is

connected to the bias ring with a long polysilicon resistor. A thin metal routing connects the readout strip to the pads. The Near Strips pitch/width is 100/25 μm .

The readout electronics noise has a crucial contribution from the backplane capacitance of the bulk and the capacitance between adjacent electrodes (strips). These factors have been studied in order to evaluate the effect of cross talk between nearby Near-Far strips.

Fig 1. Schematics of the test structure proposed. The simulated area is marked in the rectangle.

3) Simulation results

TCAD package (SYNOPTIS) [2] was used for three-dimensional simulation of the Near-Far strip region and optimize the distance between p+ implants. For DC and AC simulations a bias of 350 and 100 V, respectively, was applied. A charge of $0.7\text{E}+11 \text{ q/cm}^2$ was considered at the interface between silicon/oxide. To compare the results, four different geometries were considered.

Layout#1 has only two Near-Near like strips (used as reference), Layout#2, Layout#3, and Layout#4 have two strips Near, Near (on one side) and one Far strip (on the other side) but the difference stands on the distance between P+ edge of Near and Far strips: at the same level, 20 μm distance and 20 μm overlap, respectively.

Table 1. The capacitances calculated for a 10 KHz frequency signal, 'strip1' and 'strip2' are the two Near- like strips, 'farstrip' is the Far-like strip.

The electric field at the junction border show a maximum value. For Layout#1 is $1.5\text{E}+5 \text{ V/cm}$ (breakdown field in Si $\sim 3.0\text{E}+5 \text{ V/cm}$), similar values for the other layouts, $(5.2\text{--}7.5) \text{E}+4 \text{ V/cm}$. The capacitances between different electrodes from the structure (as DC and AC contacts) were calculated and are presented in Table 1.

4) Conclusion

For the avalanche breakdown process, the structure demonstrates a good resistivity, the metal routing lower the electric field at the Near Strips junction. In Table 1, can be seen the clear variation of the different components of the interstrip capacitance between neighbour strips. The influence of the opposite strip to this parameter starts to be significant when the Far Strip junction is at the same level or between Near Strips. Further studies will be dedicated to the influence of the radiation damage on these values.

5) References

- [1] <https://twiki.cern.ch/twiki/bin/view/CMS/CEC>
- [2] <http://www.synopsys.com/Tools/TCAD/Pages/default.aspx>

	Layout 1 (pF/cm)	Layout 2 (pF/cm)	Layout 3 (pF/cm)	Layout 4 (pF/cm)
strip1_DC -strip2_DC	0.11	0.05	0.04	0.05
strip1_AC-strip2_DC	0.08	0.03	0.03	0.027
strip1_AC-strip1_DC	24	26	24	27
strip1_AC-strip2_AC	0.062	0.016	0.021	0.014
farstrip_AC - farstrip_DC		52	50	51.7
strip1_DC-farstrip_DC		0.17	0.1	0.16
strip1_DC-farstrip_AC		0.3	0.2	0.27
strip1_AC-farstrip_AC		0.22	0.23	0.17
strip1_AC-farstrip_DC		0.13	0.07	0.1