Mechanism controller system for the optical spectroscopic and infrared remote imaging system instrument on board the Rosetta space mission

J. M. Castro Marín,^{a)} V. J. G. Brown, A. C. López Jiménez, J. Rodríguez Gómez, and R. Rodrigo

Instituto de Astrofísica de Andalucía, CSIC, P.O. Box 3004, E-18080 Granada, Spain

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The optical, spectroscopic infrared remote imaging system (OSIRIS) is an instrument carried on board the European Space Agency spacecraft Rosetta that will be launched in January 2003 to study *in situ* the comet Wirtanen. The electronic design of the mechanism controller board (MCB) system of the two OSIRIS optical cameras, the narrow angle camera, and the wide angle camera, is described here. The system is comprised of two boards mounted on an aluminum frame as part of an electronics box that contains the power supply and the digital processor unit of the instrument. The mechanisms controlled by the MCB for each camera are the front door assembly and a filter wheel assembly. The front door assembly for each camera is driven by a four phase, permanent magnet stepper motor. Each filter wheel assembly consists of two, eight filter wheels. Each wheel is driven by a four phase, variable reluctance stepper motor. Each motor, for all the assemblies, also contains a redundant set of four stator phase windings that can be energized separately or in parallel with the main windings. All stepper motors are driven in both directions using the full step unipolar mode of operation. The MCB also performs general housekeeping data acquisition of the OSIRIS instrument, i.e., mechanism position encoders and temperature measurements. The electronic design application used is quite new due to use of a field programmable gate array electronic devices that avoid the use of the now traditional system controlled by microcontrollers and software. Electrical tests of the engineering model have been performed successfully and the system is ready for space qualification after environmental testing. This system may be of interest to institutions involved in future space experiments with similar needs for mechanisms control. © 2001 American Institute of Physics. [DOI: 10.1063/1.1366632]

I. INTRODUCTION

The International Rosetta Mission of the European Space Agency (ESA) provides a unique opportunity by which to investigate, in detail, a relic from the birth of the solar system. This new European space mission is due to be launched to the short-period comet, 46P/Wirtanen, in January 2003. A scientific payload will be on board the spacecraft to investigate the nucleus of the target comet as the spacecraft approaches to within a few nuclear radii of the surface. Moreover, new *in situ* measurements will be performed by the inclusion of a surface science package that will be placed onto the nucleus (see, for example, Refs. 1 and 2). The optical, spectroscopic infrared remote imaging system (OSIRIS) will play a major role in this investigation. A consortium comprised of seven countries is constructing the experiment. A lead scientist, who forms the single link to the principal investigator, represents each country. Within each country, several organizations will contribute to the experiment. The countries and organizations are listed in Table I. In the breakdown of hardware responsibilities, the Instituto de Astrofísica de Andalucía (IAA) is responsible for the mechanism controller board (MCB). To achieve the scien-

tific goals, the OSIRIS experiment consortium has proposed a dual camera system together with a common electronics box and two separate charge coupled device (CCD) readout electronics boxes. A narrow angle camera (NAC), with high resolution ($>1.15^\circ \times 1.15^\circ$), has been designed to study the nucleus and a wide angle camera (WAC) has been designed to view large parts of the inner coma and to investigate dust and gas emission directly above the surface of the nucleus. For a better description of the experiment see Ref. 3.

II. PHYSICAL DESCRIPTION

The MCB consists of two boards, the control board and the driver's board, mounted in the MCB frame with the components facing inward. The control board occupies the full frame capacity of 190 mm $\times$ 190 mm. The driver's board is mounted on the opposite face of the frame and occupies a space of 105 mm $\times$ 190 mm. Interconnections between the two boards are made using two flexible circuits that are qualified for space applications by Nicolitch (Sferflex Technology). These were selected because their low profile was compatible with the board spacing. Connection to the electronics box interface (EFI) is made by a KNC 0621310219, 62 pin, connector. Two DB62S connectors, 62 pins, make connections to the NAC and WAC, respectively (see Fig. 1). The subsystem overall mass is 602 g. The power consump-

^{a)}Electronic mail: castro@iaa.es

TABLE I. Organizations contributing to OSIRIS.

Country	Contributing Organization
Germany	Max-Planck-Institut für Aeronomie, Katlenburg-Lindau (MPAe) Technical University, Braunschweig (IDA) DLR-Institut für Weltraumsensorik, Berlin (DLR-WS)
France	Laboratoire d'Astronomie Spatiale, Marseille (LAS)
Italy	University of Padova (UPD)
Spain	Instituto de Astrofísica de Andalucía, Granada (IAA) Instituto Nacional de Técnica Aeroespacial, Madrid (INTA) Universidad Politécnica, Madrid (UPM)
Sweden	Astronomical Observatory, Uppsala (AOU)
ESA	Space Science Dept. of ESA, ESTEC The Netherlands (SSD)

tion varies a great deal with the mode of operation. Maximum peak power taken by the complete MCB is 3.7 W, 1.5 W quiescent.

III. OPERATIONAL DESCRIPTION

The control board contains the digital circuits for communication and mechanism control. The analog housekeeping and position monitor circuits are also mounted on this board. The digital control circuits are implemented by using two field programmable logic arrays (FPGAs). Data exchange with the digital processing unit (DPU) module is established using RS-422 line drivers and receivers (HS-26C31/32). Data gathering, packaging, transmission and command decoding are performed within the FPGAs (Actel RH1280).^{4,5} The FPGAs also translate the DPU mechanism commands into motor phase drive programs that are passed to the motor drivers mounted on the driver's board. Full dual redundancy has been employed for the line drivers, digital circuits, and the analog multiplexing and conversion circuits. The two analog data gathering multiplexers read data from single temperature sensors regardless of which circuit is in use. Similarly, either the main or the redundant digital circuit reads the single position monitors from all mechanisms.

The driver's board, although connected to the control board, is electrically isolated from it by optical coupling (HCPL6750) and by the use of only the motors' power supply. Two motor power supply lines allow the selection of

main, redundant or both driver circuits and motor windings. The board makes the power translation of the phase signals from the control board to the relevant mechanism motors. The power switching elements used are hexfets (IRHG7110). Each motor has four main phase drivers and four redundant phase drivers. There are three motors used in each of the two cameras giving a total of 48 phase driver circuits. Either the main or the redundant control board digital circuit can program all 48 phases.

Two field programmable gate arrays, the MCB_controller FPGA and the Ctr_Step FPGA, carry out all operational functions. The MCB_Controller FPGA communicates with the OSIRIS DPU via the on-board interfaces referred to previously. This FPGA also interprets commands and reports on consequences and housekeeping functions to the OSIRIS DPU. The MCB_Controller FPGA also exchanges information with the Ctr_Step FPGA. The Ctr_Step FPGA is concerned with the mechanism motor drives and generates the basic phase drive sequences. In addition to this, the Ctr_Step FPGA provides a suite of programs to optimize each mechanism's motor performance.

A. MCB_controller FPGA description

The MCB_Controller FPGA must perform the following functions: communication, command decoding and execution, housekeeping acquisition and local reset.

The communication link to and from the DPU is implemented using an asynchronous half-duplex serial interface. It uses two pairs of balanced lines, one for transmission and one for reception. The speed is 115.2 kbaud with a maximum deviation of 2%. It is 8 bits wide with 1 bit start, parity even and 1 stop bit. The circuit uses a 1.8432 MHz clock to achieve a sampling of 16 times the frequency of communications. Each bit of information is acquired with a majority method to improve immunity to noise. At the end of each packet there is one byte formed by the sum of the packet bytes, called the checksum byte. The FPGA detects any reception error in the parity, frame or checksum. If an error occurs, the command is rejected and an error bit is transmitted in the status word. The number of bytes in each packet depends upon the command type (there is a variable number of parameter bytes, from 0 to 5). Each parameter must be saved in its corresponding register to implement the received command. In transmission mode, the interface must generate the complete set of bytes for each packet of variable length from 3 to 87 bytes, generating each parity bit and the checksum byte at the end.

The command decoder is responsible for the interpretation of commands. There are three types of command: commands related to the two stepper controllers, commands related to the six motors (phases or steps) and commands related to the data acquisition (analog or digital data). When a legal command is received, it is then executed. If the command is related to any motor or stepper controller, there is a complete set of control signals between the Ctr_Step FPGA and the MCB_Controller FPGA allowing execution. The interface between both uses a number of lines. The lines to the Ctr_Step FPGA are

FIG. 1. Block diagram of the mechanism controller board.

TABLE II. Velocity values v (steps/s) vs programmed values (PV), in HEX format, stored in the MCB_Ctr_Step FPGA.

PV	v	PV	v	PV	v	PV	v	PV	v	PV	v	PV	v	PV	v
0	147.8	10	130.4	20	116.7	30	96.4	40	80.6	50	62.5	60	50.4	70	29.2
1	146.6	11	129.5	21	115.2	31	95.4	41	79.2	51	61.6	61	48.2	71	28.4
2	145.4	12	128.6	22	113.7	32	94.4	42	77.8	52	60.8	62	46.2	72	27.7
3	144.2	13	127.6	23	112.3	33	93.4	43	76.5	53	59.9	63	44.4	73	27.0
4	143.1	14	126.7	24	110.9	34	92.4	44	75.2	54	59.1	64	42.6	74	26.4
5	141.9	15	125.8	25	109.5	35	91.4	45	73.9	55	58.4	65	41.1	75	25.8
6	140.8	16	124.9	26	108.2	36	90.5	46	72.7	56	57.6	66	39.6	76	25.2
7	139.7	17	124.1	27	106.9	37	89.6	47	71.5	57	56.9	67	38.2	77	24.6
8	138.6	18	123.2	28	105.6	38	88.7	48	70.4	58	56.1	68	37.0	78	24.1
9	137.5	19	122.3	29	104.4	39	87.8	49	69.3	59	55.4	69	35.8	79	23.6
A	136.5	1A	121.5	2A	103.1	3A	87.0	4A	68.2	5A	54.8	6A	34.6	7A	23.1
B	135.4	1B	120.7	2B	102.2	3B	86.1	4B	67.2	5B	54.1	6B	33.6	7B	22.6
C	134.4	1C	119.9	2C	100.8	3C	85.3	4C	66.2	5C	53.4	6C	32.6	7C	22.2
D	133.4	1D	119.1	2D	99.7	3D	84.5	4D	65.2	5D	52.8	6D	31.7	7D	21.7
E	132.4	1E	118.3	2E	98.6	3E	83.7	4E	64.3	5E	52.2	6E	30.8	7E	21.3
F	131.4	1F	117.3	2F	97.5	3F	82.6	4F	63.4	5F	50.8	6F	60.0	7F	21.0

- (1) 13 lines for parameter (data, phases, motion direction).
- (2) 30 lines for enable/control.
- (3) 1 reset line.
- (4) 1 clock at 1.8432 MHz.

Moreover, the lines from the Ctr_Step FPGA to the MCB_Controller FPGA are

- (1) 9 lines for parameter (data, phases).
- (2) 2 status lines.

At the end of each process, the answer is transmitted to the DPU with its corresponding parameters. When the decoder detects an illegal command, it is not executed and the packet with the status indicating the error is transmitted.

The housekeeping acquisition must implement control of the external multiplexers and analog to digital (A/D) converter. Internally, it is also necessary to control the delay to acquire the data and to control the internal multiplexers. In addition to reading out the housekeeping data, the power supply for each of the temperature sensors is derived from demultiplexers controlled in parallel with the readout multiplexers. The demultiplexers ensure that the power is only present at the sensor when being read out, after one sample settling time, to avoid self-heating errors. All temperature sensor supplies are short circuit proof. There are four types of data acquired: data from the A/D converter (temperatures or voltages), data from the stepper controllers (parameters corresponding to the status of each stepper controller), data from the motors' driven signal (phases) or data from the position of mechanisms (doors or filter wheels). Each type of data needs to be read out and processed differently.

Finally, on this subsystem there are two types of reset signals, the power on reset (POR) signal⁶ and the system reset signal (SYSRES). The signal POR is generated when the supply is switched on. It is an active low pulse of 50 ms width initiated after the voltage has reached a set level. It clears all counters and registers of both FPGAs. This circuit has been included in the subsystem to ensure a reset signal after switch on of the system. The SYSRES signal is transmitted from the DPU. This is a low pulse of 8.7 μ s width.

This reset is edge triggered, since it has a digital low pass filter that rejects any pulse shorter than 2.4 μ s. Thus, if the balanced line of SYSRES remains in an active state more than 8.7 μ s, the FPGA will commence with normal functions.

The occupation level of the MCB_Controller FPGA is 52% of the logic cells with 121 input/output pads.

B. MCB_Ctr_Step FPGA description

The Ctr_Step FPGA consists of three blocks:

- (1) controller block: two independent controllers allowing the movement of two motors simultaneously with different parameters;
- (2) motor's block: generation of phases for the six motors, with the possibility of programming the initial phase of movement, and realignment of the motor's electrical and mechanical pole position for the first step;
- (3) communication block: links Ctr_Step FPGA with the MCB_Controller FPGA.

The programmable parameters of the controller are

- (1) minimum velocity: first and last step's velocity and, in case of failure, velocity for the rest of the movement;
- (2) maximum velocity: velocity in the plateau of the movement;
- (3) acceleration: ramp to achieve the maximum velocity from the minimum velocity;
- (4) deceleration: ramp to achieve the minimum velocity from the maximum velocity;
- (5) steps: number of steps in the movement; the controller sends this number plus one to realign the motor (the maximum value is 1024).

The values of the velocities are listed in Table II. Acceleration and deceleration define the length of the jump in Table II to the next step.

The step number at which the deceleration ramp begins is calculated before the beginning of the movement, presuming that the $V_{\max}$ is reached. If the ramp up is too slow, and

FIG. 2. Velocity profile of one motor.

the step calculated to begin the ramp down is reached at some other velocity than $V_{\max}$, the ramp down begins and the rest of the steps are made at $V_{\min}$.

The rest of the movement is made at $V_{\min}$ each time the velocity of the step is less than $V_{\min}$. The reasons for this situation can be bad calculation in the ramps, as explained earlier, the $V_{\max}$ programmed is less than the $V_{\min}$ or there is a glitch in the system that causes an out of range velocity.

After a Reset (commanded by the DPU or by power on) the parameters are set to default values.

Both controllers have the same capabilities.

The generation of the pulses, which changes the status of the phases, is produced by the selection of different clocks with different frequencies and preloading the counters with fixed values that are generated directly. With the algorithm that couples four hyperbolas in a smooth way, the ramps of acceleration and deceleration are linearized to optimize motor performance (see Fig. 2).

Other features include the following.

- (1) For the compensation of asymmetry in the optocouplers leading “to make before break” switching, the controller generates a delay of 54 μ s from the falling edge of one phase to the rising edge of the next phase.
- (2) A requirement of the filter wheel mechanism is to maintain the phases of the last step energized for a holding time of 463 ms.
- (3) The movement of zero steps has a special meaning, that is, to energize the programmed phases for about 1 s, and this is implemented to heat up the motors. To ensure that the power control module (PCM) can supply the power consumed in the different operational modes of the system, this so called movement has another programmable parameter, which activates two phases or only one of the four phases.

The motor block generates the phases in the full step

mode for a four-phase motor with double windings. It simultaneously produces the phases for the main and the redundant windings through different pads for security. The power supplied to the motors selects which groups of windings are energized; it is possible to work with both groups if needed.

The phase of each motor can be read and written by the DPU.

Each motor block can be driven by any of the controller blocks; with this, the system has an intrinsic redundancy.

The occupation level of the Ctr_Step FPGA is 96% of logic cells with 108 input/output pads.

IV. ENVIRONMENTAL CONSIDERATIONS

A. Thermal

The MCB is required to operate satisfactorily over -20 to 50 $^{\circ}\text{C}$. All electronic devices are procured to a specification of -55 to 125 $^{\circ}\text{C}$.

B. Radiation

A general problem in all space applications is that it is not always possible to provide dual redundant subsystems without significantly exceeding the mass and power resource limits. These problems are solved by the use of high reliability rad hard electronic devices in order to achieve the same probability of survival as the much more complex dual redundant system. Wherever possible, subsystems will have self-secure default states in order to allow degraded operation in case of failure.

For the OSIRIS instrument a total radiation dose of 20 krad is expected inside the electronic box, made of aluminum with walls 2.6 mm thick, over the 12 year mission, with a large proportion being solar protons.

The OSIRIS electronics redundancy concept fulfills the requirement to survive a single system failure without performance degradation. The MCB electronics use full redun-

dancy with rad hard and hi-rel components to ensure reliable performance for the duration of the mission. The effects fall into two categories, catastrophic failure and single event upset.

- (1) Catastrophic failure. This can only be guarded against by careful procurement of parts. Known vendors capable of achieving better than 50 krad tolerances are used for the general logic.
- (2) Single event upset. Significant where a bistable circuit element can be changed, this problem affects mainly the FPGA devices and the general logic with bistable functions. The approach adopted is S-module flip-flops are partially excluded from the synthesized output. The synthesis can be controlled to either use radiation-tolerant flip-flops (C-module or C-C flip-flops) or triple-modular redundant (TMR) structures.

The frequency of single events upset (SEU) is unknown but components have been selected with a linear energy transfer (LET) threshold greater than 25 MeV cm²/mg as a precaution. Furthermore, the electronic devices used are guaranteed latch up free by the manufacturer.

V. DISCUSSION

The hardware described above was devoted to a specific application but the system can easily be adapted to other similar requirements. By using independent phase control the motor drive mode is not confined to the unipolar full step shown in this case. More flexibility in the application can be made with little or no hardware changes. The hardware is now approaching the conclusion of its rigorous qualification and acceptance testing and further interest has already been

shown in using this within similar space applications that require automated and robotic precision events.

Further mass and electronic optimizations are being entertained while maintaining the overall design relatively unchanged.

The design, fabrication and testing of the MCB have succeeded in meeting the demands of space application by

- (1) acquiring and applying the knowledge gained by investigating and assessing "state of the art" drive/control electronics;
- (2) using improved modern electronic design technology, e.g., FPGA devices, for space applications due to the limitations imposed: high density with maintained performance for the small board size, power restrictions and weight requirements, moderate speed, low cost, and quick turnaround time;
- (3) removing the need for complex software routines needing continuous updating in a peripheral subsystem and sometimes leading to catastrophic instrument failure.

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