

# Quantization Noise Shaping Degradation in Switched-Current BandPass Sigma-Delta Modulators

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**ABSTRACT** - This paper presents a systematic analysis of the major switched-current errors and their effects on the degradation of the Noise Shaping for 4th-Order BandPass  $\Sigma\Delta$  Modulators. The results obtained have been applied to design a silicon prototype in a 0.8 $\mu$ m CMOS technology. Experimental results show 8-bit resolution for 30kHz signal band centered at 2.5MHz with 10MHz clock frequency.<sup>(1)</sup>

## 1. Introduction

Except for the influence of second-order parasitics, *switched-capacitor* (SC) and *switched-current* (SI) analog sampled-data techniques obtain inherently linear and accurate time-constants using a quite simple circuitry; much less intricate than required for analog continuous-time techniques. This is a positive consequence of their synchronous operation, another being the use of the precharging time slots for error correction. SC and SI circuits are also easily decomposable into loosely coupled modules, and hence relatively simple to design and amenable for automatic synthesis. Since, in addition, their technological requirements are modest, these analog sampled-data techniques are very well-suited for the analog interfaces of modern mixed-signal CMOS-ASICs, as it has been already demonstrated up to video frequencies [1][2]. This suitability is further enhanced through the use of techniques such as *oversampling* and *noise-shaping*. Their combined use in the field of analog-to-digital conversion result in the architectures known as sigma-delta ( $\Sigma\Delta$ ) modulators [3].

A wide variety of CMOS analog sampled-data  $\Sigma\Delta$ -modulators have been reported in literature, with their current application spanning from instrumentation to telecom [3]. Most of them used switched-capacitor circuits. However, the use of circuits operating in current domain may be advantageous for many applications. There are for instance many sensors whose outputs are currents; typical examples are light and radiation sensors, but this applies also to some temperature and magnetic sensors, and to many others found in biomedicine. For these cases, processing directly in current domain avoids the use of current-to-voltage converters, and hence, yields better performance, smaller power budget and smaller circuit cost. In addition, switched-currents (SI) circuits are specially well suited to design mixed-signal chips in standard CMOS single-poly technologies [1].

Several SI  $\Sigma\Delta$  modulator ICs have been already reported in literature [4] [5], for different applications. Recently, we have also reported a SI bandpass  $\Sigma\Delta$  realized in a single-poly 0.8  $\mu$ m CMOS technology [6].

However, up to now, there is not a systematic study of non-idealities for SI  $\Sigma\Delta$  Modulators just as for SC  $\Sigma\Delta$  Modulators where the characterization of their major sub-blocks like operational amplifier finite gain, clock jitter, etc... have been modeled and described thus as their influence on the degradation of modulators [7] allowing an automatic design methodology [8].

This paper presents a systematic analysis of the major switched-current errors and their effects on the degradation of the Noise Shaping for 4th-Order BandPass  $\Sigma\Delta$  Modulators. The aim of this study is to identify the influence of the different errors and to provide equations to facilitate the design of this class of modulators. The equations obtained have been applied to the design of a  $\Sigma\Delta$  SI BandPass modulator that allows signal demodulation at 2.5MHz with 8 bit of resolution. These results are better than the first prototype SI BandPass reported in [6].

## 2. BandPass $\Sigma\Delta$ Modulators

The process of A/D conversion involves the operations of sampling and quantization. The latter introduces the so-called quantization error, which analog IC designers usually model through an additive noise source with flat (white) power spectral density (*quantization noise*) [3]. Fig.1(a) illustrates this for a  $N$ -bit

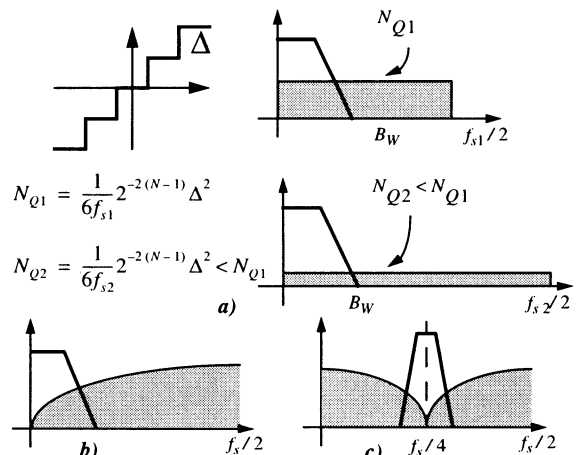


Fig. 1: Filtering of the Quantization Noise in  $\Sigma\Delta$  Modulators. a) Noise of a  $N$ -bit Quantizer. b) Lowpass  $\Sigma\Delta$ M. c) BandPass  $\Sigma\Delta$ M.

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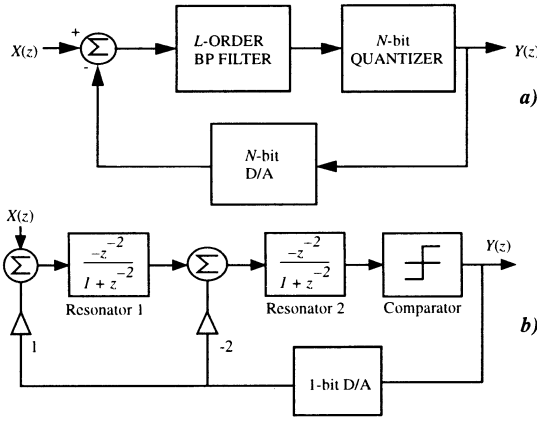


Fig. 2: Conceptual Block Diagram of BandPass  $\Sigma\Delta$  Modulator. a)  $N$ -bit  $L$ -Order. b) 1-bit 4th-Order

quantizer, where  $\Delta$  represents the quantization step. Let be  $B_w$  the band of the signal to be quantized. The in-band quantization noise power is calculated as  $N_Q B_w$ , where  $N_Q$  is the noise power spectral density,

$$N_Q = \frac{1}{12MB_w} 2^{-2(N-1)} \Delta^2 \quad 0 < f \leq f_s/2 \quad (1)$$

It has been expressed for convenience as a function of  $M$  ( $\equiv f_s / (2B_w)$ ), which is the ratio between the sampling frequency and the signal band, called Over-Sampling Ratio (OSR). Note that the density above is inversely proportional to the sampling frequency  $f_s$ ; i.e., inversely proportional to  $M$ .  $\Sigma\Delta$  modulators use oversampling (i.e., large values of  $M$ ) to decrease the power of quantization noise in the signal band (see Fig.1(a)); and filtering for shaping this noise and pushing it out of the signal band (see Fig.1(b)). This filtering is of the highpass type for lowpass modulators (Fig.1(b)), and of the bandstop type for bandpass modulators (Fig.1(c)).

Fig.2(a) shows the conceptual block diagram of a single-loop bandpass  $\Sigma\Delta$  modulator. The output is given by,

$$Y(z) = S_{TF}(z) X(z) + N_{TF}(z) E(z) \quad (2)$$

where  $X(z)$  is the input signal and  $E(z)$  represents the additive quantization noise source. Typically, bandpass  $\Sigma\Delta$  modulator architectures are obtained from corresponding lowpass prototypes by applying a  $z^{-1} \rightarrow -z^{-2}$  transformation; this maintains the stability properties of the original and enables to take advantage of the knowledge available on the properties of lowpass modulators [3]. Thus, the ideal quantization Noise Transfer Function ( $N_{TF}$ ) is of the bandstop type,

$$N_{TF}^i(z) = (1 + z^{-2})^L \quad (3)$$

where  $L$  is the loop order. This latter function has transmission zeroes at  $f_s/4$ , for  $z = \exp(j2\pi f/f_s)$ . Correspondingly, the noise transfer function for a single-loop lowpass modulator exhibits zeroes at DC. From (2) and (3) the in-band quantization noise power

is calculated from,

$$P_{EQ}^i = \int_{(f_s/4 - B_w/2)}^{(f_s/4 + B_w/2)} N_Q |N_{TF}^i(f)|^2 df \quad (4)$$

giving

$$P_{EQ}^i \approx \frac{1}{3} \frac{\Delta^2 \pi^{2L}}{2^{2N} (2L+1) M^{2L+1}} \quad (5)$$

On the other hand, taking into account that the largest amplitude sinewave that the modulator will accommodate without saturating has peaks at  $\pm\Delta/2$ , we obtain the following expression for the maximum Signal Noise Ratio ( $SNR$ ) due to quantization for a sinusoidal input,

$$SNR_{Q_{max}} = 10 \log \frac{3(2^{2N} (2L+1) M^{2L+1})}{8\pi^4} \quad (6)$$

The  $SNR$  can alternatively be expressed as a function of the number of equivalent bits,  $b$ ,

$$SNR = 6.02b + 1.76 \quad (7)$$

Equation (6) shows that the  $SNR$ , and hence the number of equivalent bits in (7), increases for the oversampling ratio  $M$ , the filtering order  $L$ , or the number of quantization levels  $N$  increasing. However, practical circuit implementations of the bandpass  $\Sigma\Delta$  modulator architecture deviate significantly from this ideal scenario. First, high-filter orders larger than  $L = 2$  result in serious stability problems [9]. Second, large  $N$  values are unfeasible due to the sensitive influence of unavoidable linearity errors in the in-loop multi-bit D/A converter [3]. Third, the shaping of the quantization noise may become severely degraded due the circuit parasitics (loading effects, incomplete settling, charge injection, etc.) [7]. Last, but no least, the intrinsic circuit noise may dominate as compared to the quantization noise, and hence may destroy the benefits of oversampling and filtering [7].

As stated in the introduction, this paper focuses on 1-bit ( $N = 1$ ) modulators with  $L = 2$ . These modulators are easy to understand and simple to design, are capable to provide high resolution together with large tolerance to imperfections and robust stable operation. These features render them a convenient trade-off for implementation purposes, for lowpass as well as for bandpass[7][10]. Thus, we will start from a 2nd order lowpass, which after the  $z^{-1} \rightarrow -z^{-2}$  transformation, results in the associated bandpass architecture of Fig.2(b), whose transfer function for the input signal ( $S_{TF}$ ) is a double delay. The expressions for the quantization noise power and the maximum  $SNR$  due to quantization are calculated from (5) and (6) by making  $L=2$  and  $N=1$ ,

$$P_{EQ}^i = \frac{\Delta^2 \pi^4}{60M^5} ; SNR_{Q_{max}}^i = 10 \log \left( \frac{15M^5}{2\pi^4} \right) \quad (8)$$

Fig.3(a) depicts the  $SNR_{Q_{max}}$  as a function of the

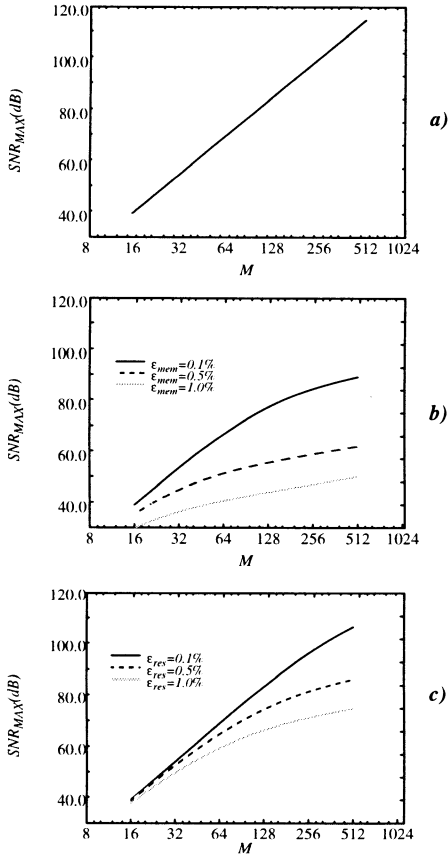


Fig. 3:  $SNR_O$  Degradation with errors. a) Ideal Case. Nulling all errors except (b) the memory cell error or (c) the gain error.

oversampling ratio for this ideal case where filtering is free of errors. In this ideal scenario the resolution increases with  $M$  at a rate of about 2.5bits per octave. This is to be compared with the corresponding curves of Figs.3(b) and (c) which depicts the influence of different errors in the shaping of the quantization noise. We will postpone any further explanation of these curves until the next section.

### 3. Non-Ideal Quantization Noise Shaping in SI Circuits

#### A. SI Basic Building Blocks and Associated Errors

The *resonator* is the only linear building block in the bandpass architecture of Fig.2(b). It can be realized as an interconnection of smaller subblocks (memory cells and integrators) using different alternatives [10]. Fig.4(a) shows one that uses two LD integrators in a feedback loop. Out from the different resonator realization alternatives, this is actually the only which, when considered as a stand-alone unit, remains stable under changes of the feedback coefficient due to circuit parasitics -- the reason why we have adopted this structure in our work. Fig.4(b) illustrates the movements of the resonator poles under changes of  $A_F A_{FB}$  around its nominal value of 2. It can be seen how they remain at the unity circle.

Fig.4(c) shows the architecture of a bandpass modulator based on the resonator of Fig.4(a). The scal-

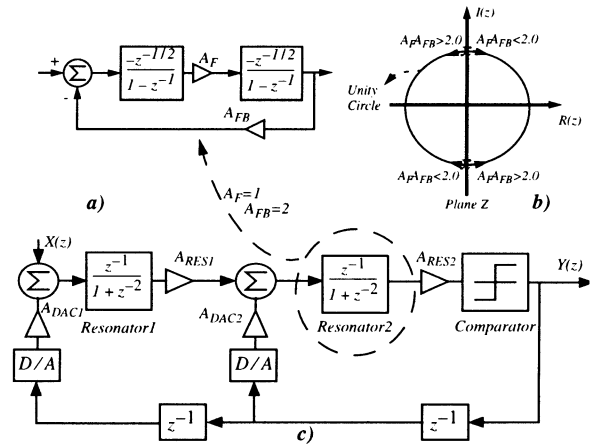


Fig. 4: a) Resonator based on BE-Integrator. b) Movement of Poles around the Unity Circle for Changes on Feedback Gain. c) Block Diagram of the BPΣΔM based on the Resonator of (a).

ing factors can be optimized to obtain similar dynamic range for both resonators, bearing in mind the general recommendations about the scaling of SC and SI circuits [4]. This obtains the following nominal values,

$$A_{RES2}^{nom} = A_{DAC2}^{nom} = -A_{DAC1}^{nom} = 1; A_{RES1}^{nom} = 1/2 \quad (9)$$

Fig.5 shows conceptual SI realizations of the memory and the BE integrator. The memory cell is a second generation one to avoid mismatch errors in its operation[1]. On the other hand, double sampling [3] is not used to reduce constraints in the modulator frequency band. The attenuation of charge injection errors in the actual circuits is achieved through dummy switches and the fully-differential topology.

*Errors in the Memory Cell:* In accordance to [1], its major error sources are: *finite drain conductance* (represented through a parameter  $\epsilon_g$ ); *incomplete settling* ( $\epsilon_s$ ); and *switch charge injection* ( $\epsilon_q$ ). In the more general case, the original half-delay transfer function is modified into,

$$H_{cell} = \frac{-az^{-1/2}}{b + cz^{-1}} \quad (10)$$

where the coefficients  $a$ ,  $b$  and  $c$  are different for each error as Table 1 shows.

*Errors in the BE Integrator and Resonator:* Table 1 summarizes the influence of the memory cell errors in both blocks, calculated hierarchically from the non-ideal memory cell transfer functions. The bottom part contains the non-ideal resonator transfer functions due to deviations in the scaling coefficients included

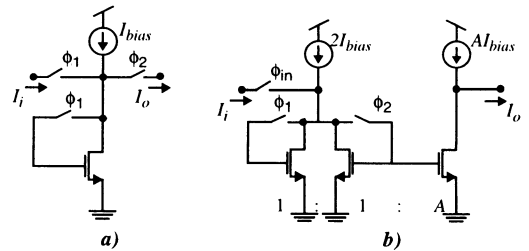


Fig. 5: Conceptual SI Second Generation (a) Memory Cell. (b) BE-Integrator.

in the resonator architecture of Fig.4 (a),

$$A_F = A_F^{nom} (1 - \epsilon_F); A_{FB} = A_{FB}^{nom} (1 - \epsilon_{FB}) \quad (11)$$

These scaling errors are due to the finite output resistance of the integrator gain stage, and the mismatch error in the current mirror used as output stage. Thus, this scaling error is given generically as

$$\epsilon_{gain} = \frac{R_{in}}{R_{out}} \epsilon_{mis} \quad (12)$$

where  $R_{in}$  is the integrator input resistance,  $R_{out}$  is the output resistance of the integrator gain stage resistance and  $\epsilon_{mis}$  is the mismatch error. Other scaling errors are found at the modulator level, they do not hence influence on the resonator transfer function, and affect to the resonator and the DAC gains,

$$\begin{aligned} A_{RES1,2} &= A_{RES1,2}^{nom} (1 - \epsilon_{RES1,2}) \\ A_{DAC1,2} &= A_{DAC1,2}^{nom} (1 - \epsilon_{DAC1,2}) \end{aligned} \quad (13)$$

### B. Non-Ideal Quantization-Noise Shaping

Because of the errors mentioned above, the zeroes of  $N_{TF}$  are shifted from their nominal positions at  $f_s/4$ , thus degrading the filtering performed by the resonators and making the quantization noise floor to increase in the signal band and, correspondingly, the SNR to decrease. Table 2 shows the quantization noise power grouped in three families: memory cell errors ( $\epsilon_g, \epsilon_s, \epsilon_q$ ) which we will represent generically by the parameters  $\epsilon_{mem}$ ; resonator loop gain errors ( $\epsilon_F, \epsilon_{FB}$ )  $\epsilon_{res}$ ; and transmission gain errors ( $\epsilon_{RES1}, \epsilon_{RES2}, \epsilon_{DAC1}, \epsilon_{DAC2}$ )  $\epsilon_{gain}$ .

Note that the non-ideal shaping of the quantization noise results in an increased noise power  $\Delta P_Q$ , different for each family. These power noise increments have identical expressions for the different members of

Table 1: SI Block Degradation

Error	Function Degradation	
	Memory Cell	Integrator
$\epsilon_{g,q}$	$\frac{-z^{-1/2}}{1 + \epsilon_{g,q}}$	$\frac{-(1 - 2\epsilon_{g,q})z^{-1/2}}{1 - (1 - 2\epsilon_{g,q})z^{-1}}$
$\epsilon_s$	$\frac{-(1 - \epsilon_s)}{1 - \epsilon_s z^{-1}} z^{-1/2}$	$\frac{-(1 - \epsilon_s)(1 - \epsilon_s z^{-1})z^{-1/2}}{(1 - \epsilon_s^2 z^{-1})(1 - z^{-1})}$
<b>Resonator</b>		
$\epsilon_{g,q,s}$	$\frac{(1 - 4\epsilon_{g,q,s})z^{-1}}{1 - 4\epsilon_{g,q,s}z^{-1} + (1 - 4\epsilon_{g,q,s})z^{-2}}$	
$\epsilon_F$	$\frac{(1 - \epsilon_F)z^{-1}}{1 - 2\epsilon_F z^{-1} + z^{-2}}$	
$\epsilon_{FB}$	$\frac{z^{-1}}{1 - 2\epsilon_{FB}z^{-1} + z^{-2}}$	

the same family of errors providing an identical degradation of the maximum SNR.

Table 2 provides insight on the significance of the different error sources. For completeness this has to be complemented with the ranges expected for the errors parameters, which depending on the adopted circuit strategy may vary typically between 0.1% and 1%. Several conclusions are drawn from Table 2.

- The first two family of errors, respectively, dominate as compared to the third family.
- For the family of memory cell errors, the deviation in the quantization noise power is dominated by the term  $(\epsilon_{mem}M)^2$  up to  $\epsilon_{mem}M \approx 0.6$ ; beyond this limit the term  $(\epsilon_{mem}M)^4$  dominates, thus practically destroying all the benefits of oversampling. It is illustrated in Fig.3(b), which depicts the maximum SNR as a function of  $M$  for three values of  $\epsilon_{mem}$ , assuming the other errors are null.
- Correspondingly, for the family of transmission errors, the term  $(\epsilon_{mem}M)^2$  dominates up to  $\epsilon_{mem}M \approx 2.2$ . Fig.3(c) shows the maximum SNR as a function of  $M$  for three values of  $\epsilon_{res}$ .
- For similar values of parameters  $\epsilon_{mem}$  and  $\epsilon_{res}$ , the memory cell errors produce larger deviations in the noise transfer function than the resonator loop gain errors. This is illustrated in Fig.6 showing the SNR-peak vs. the error for  $M=167$ .

All these results have been validated by a behavioral simulation using SIMULINK [11]. In Fig.7 is shown the FFT of the simulated modulator output for a sinusoidal input of -6 dB range centered on 2.5MHz. Fig.7(a) is for an ideal modulator, Fig.7(b) and (c) are for  $\epsilon_{mem}$  or  $\epsilon_{res}=1\%$  respectively. This figure illustrates how the effect of  $\epsilon_{mem}$  degrades  $N_{TF}$  more significant than  $\epsilon_{res}$ . By other hand, in all figures the theoretical model -solid line of  $N_{TF}$  is also depicted showing a good accordance between the behavioral simulation and the proposed model.

### 4. Guidelines for the design of a 4th Order BandPass $\Sigma\Delta$ Modulator

A conservative estimation for practical design is to

Table 2: Quantization Noise Degradation

Error	Quantization Noise Power ( $P_Q$ )
$\epsilon_{mem}$	$\frac{\pi^4 \Delta^2}{60M^5} \left( 1 + \frac{640\epsilon_{mem}^2 M^2}{3\pi^2} + \frac{5120\epsilon_{mem}^4 M^4}{\pi^4} \right)$
$\epsilon_{res}$	$\frac{\pi^4 \Delta^2}{60M^5} \left( 1 + \frac{40\epsilon_{res}^2 M^2}{\pi^2} + \frac{80\epsilon_{res}^4 M^4}{\pi^4} \right)$
$\epsilon_{gain}$	$\frac{\pi^4 \Delta^2}{60M^5} (1 + 2\epsilon_{gain})$

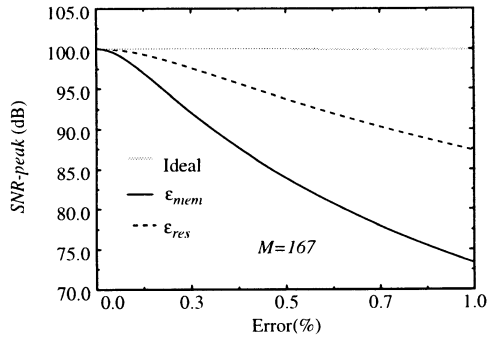


Fig. 6:  $SNR$ -peak degradation with each family of error.

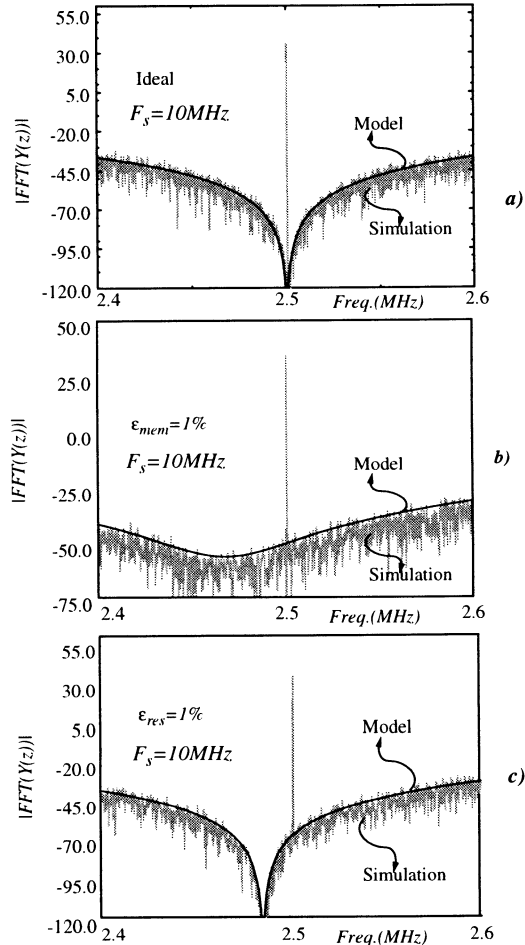


Fig. 7: a) Ideal  $N_{TF}$ . b)  $N_{TF}$  Degradation with  $\epsilon_{mem}$  and c)  $\epsilon_{res}$ .

consider that all the power noise increments are cumulative, which yields the following expression for the maximum  $SNR$ ,

$$SNR_{Q_{max}} = SNR_{Q_{max}}^i - \Delta P_Q^{total} \quad (14)$$

In addition to this degradation other ultimate limiting factor in practical realizations of  $\Sigma\Delta$  modulators is the thermal noise. While the most important contribution of 2nd-order lowpass  $\Sigma\Delta$ Ms is due to the first integrator, this is not the case of 4th order bandpass  $\Sigma\Delta$ Ms where both integrators of resonator 1 should be taken into account.

Previous considerations have been applied to design a silicon prototype in a  $0.8\mu\text{m}$  CMOS sin-

gle-poly double-metal technology. This unit converts BandPass signals with a bandwidth of 30kHz around a center frequency of 2.5MHz being the sampling frequency 10MHz.

Fig.8(a) shows the schematic of the integrator used in the modulator. It is based on a fully-differential regulated folded cascode memory cell [12] with common mode feedback. This cell incorporates local feedback in the signal path to increase the input conductance and thus reduce the interconnection loading errors. Minimum size dummy transistors are used to attenuate feedthrough error.

A major application of these modulators is converting RF signals at the AM broadcast band. For this application, an  $SNR > 50\text{dB}$  is required. Our analyses and behavioral simulations demonstrated that for this  $SNR$ , the error bound must be:  $\epsilon_{mem} < 1\%$ ,  $\epsilon_{res} < 2\%$  being the effect of  $\epsilon_{gain}$  neglected for this resolution. According to these bounds as specifications, we design the memory cell and integrator with FRIDGE, an optimizing tool developed by our group based on simulated annealing techniques [8]. The table inset of Fig.8(b) summarizes the integrator transistor sizes. Other table is included in Fig.8(c) with the memory cell and resonator errors. These are low enough to achieve the targeted modulator resolution.

Other blocks of the modulator are the comparator block which is based on a regenerative latch followed by an RS flip-flop [13] and the 1-bit D/A are current-sources controlled by the comparator output being the reference current  $50\mu\text{A}$ .

## 5. Experimental Results

Fig.9 is a microphotograph of the prototype including an internal clock phase generator and a current mode buffer for easy testing. It occupies  $0.79 \times 0.54\text{mm}^2$  (without bounding pads) and consumes 60mW from a 5V supply. Fig.10(a) shows the measured power spectrum of the modulator output when the clock frequency is 10MHz and the input is a  $-9\text{dB}@2.5\text{MHz}@\text{single tone}$ . Fig.10(b) shows the measured  $SNR$  versus input for the same modulator evaluated in a bandwidth of 30kHz. The bit streams were obtained using the unit HP82000 and Hanning-windowed 32768 point FFTs were performed for each input amplitude using MATLAB software. These measurements show  $SNR$ -peaks of 8bit@10MHz clock frequency@30kHz signal band centered at 2.5MHz and 9bit@5MHz clock frequency@20kHz signal band centered at 1.25MHz.

## 6. Conclusions

The effect of SI errors on the degradation of the Noise Shaping in 4th-Order BandPass  $\Sigma\Delta$  Modulators has been analyzed. These considerations have been applied to design a silicon prototype. Measurements are according to the digital AM receiver requirements

and improve the results obtained in our previous prototype performing correctly up to 10MHz instead 5MHz as [6] and achieving one more bit at this last clock frequency.

## 7. References

- [1] C.Toumazou, J.B.Hughes, and N.C. Battersby (editors), *Switched-Currents: An Analogue Technique for digital technology*, London: Peter Peregrinus Ltd.,1993.
- [2] J.E. Franca, Y. Tsividis (editors), *Design of analog-digital VLSI circuits for Telecommunications and signal processing* New Jersey. Prentice Hall, 1994 (2nd Edition).
- [3] S.R. Norsworthy, R. Schreier, G.C. Temes (editors), *Delta-Sigma Converters. Theory, Design and Simulation*. New York, IEEE Press, 1997.
- [4] N. Tan and S. Eriksson, "A Low-Voltage Switched-Current Delta-Sigma Modulator", *IEEE Journal of Solid-State Circuits*, Vol. 30, pp. 599-603, May 1995.
- [5] M. Bracey, W. Redman-White, and J.B. Hughes, "A Switched-Current  $\Sigma\Delta$  Converter for Direct Photodiode Interfacing", *Proc. 1994 IEEE Int. Symp. Circuits and Systems*, pp. 287-290, May 1994.
- [6] J.M. de la Rosa, B. Pérez-Verdú, F. Medeiro and A. Rodríguez-Vázquez, "CMOS Fully-Differential BandPass  $\Sigma\Delta$  Modulator Using Switched-Current Circuits", *Electronics Letters*, Vol.32, pp.156-157, February 1996.
- [7] B. Boser and B.A. Wooley, "The Design of Sigma-Delta Modulation Analog-to-Digital converters", *IEEE J. Solid-State Circuits*, Vol. 23, No. 6, pp.1298-1308, December 1988.
- [8] F.Medeiro, B. Pérez Verdú, A. Rodríguez Vázquez, and J.L. Huertas, "A Vertically-Integrated Tool for Automated Design of  $\Sigma\Delta$  Modulators". *IEEE Journal of Solid-State Circuits*, Vol. 30, pp. 762-772, July 1995.
- [9] S. Ardalan and J.Paulos, "An Analysis of nonlinear behavior in delta-sigma modulators", *IEEE Trans. on Circuits and Systems*, pp. 593-603, June 1987.
- [10] F.W. Singor and W. M. Snelgrove, "Switched-Capacitor Band-pass Delta-Sigma A/D Modulation at 10.7 MHz", *IEEE J. Solid-State Circuits*, pp. 184-192, March 1995.
- [11] MATLAB: User's guide, The Math Works Inc., 1991.
- [12] M. Goldenberg, R. Croman, and T. S. Fiez, "Accurate SI Filters Using RGC Integrators", *IEEE J. Solid-State Circuits*, Vol. 29, pp. 1388-1395, November 1994.
- [13] M. Bracey and W. Redman-White, "Design Considerations for Current Domain Regenerative Comparators", *Advanced A-D and D-A Conversion Techniques and their Applications*, pp.65-70, July 1994.

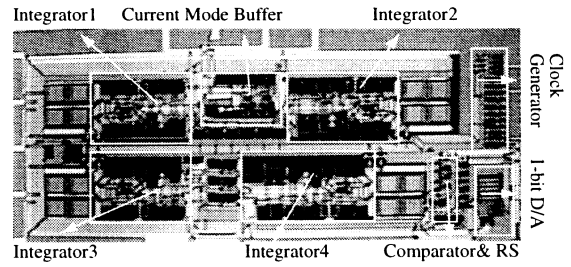


Fig. 9: Microphotograph of the BandPass  $\Sigma\Delta$  Modulator.

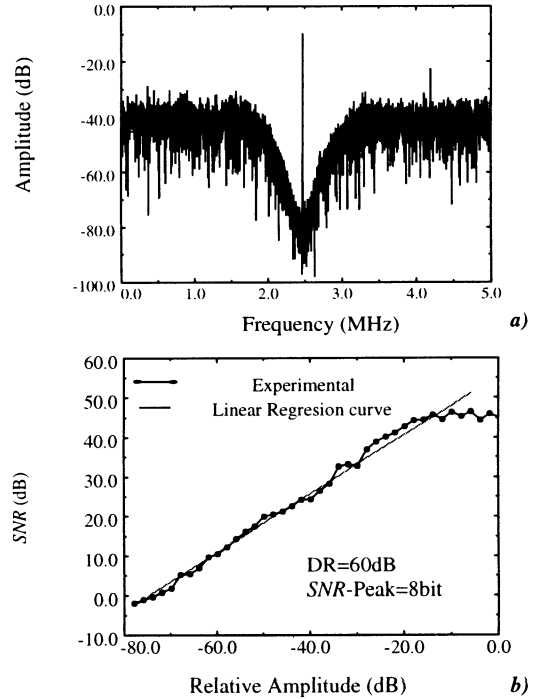


Fig. 10: a) Measured output spectrum of the modulator at 10MHz clock frequency for -9 dB input amplitude. b) Measured SNR for an input tone of 2.47MHz and clock frequency 10MHz @  $B_w=30$ kHz.

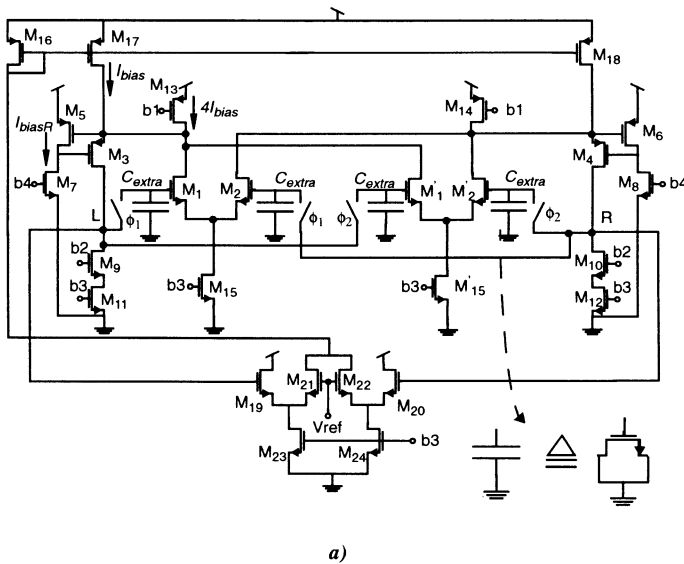


Fig. 8: a) Schematic of the Integrator. b) Transistor sizes. c) Error Values.

Transistor	Size ( $\mu\text{m}/\mu\text{m}$ )	Error	Value
$M_{1,2}$	10.1/2.3	$\epsilon_g$	0.06%
$M_{3,4}$	50/0.8	$\epsilon_q$	0.3%
$M_{5,6}$	3.7/0.8	$\epsilon_s$	0.3%
$M_{7,8}$	3/2	$\epsilon_F$	0.6%
$M_{9,10,11,12}$	27.2/2	$\epsilon_{FB}$	1.5%
$M_{13,14}$	108.8/2		
$M_{15}$	108.8/2		
$M_{16,17,18}$	27.2/2		
$M_{19,20,21,22}$	4.4/0.8		
$M_{23,24}$	27.2/2		

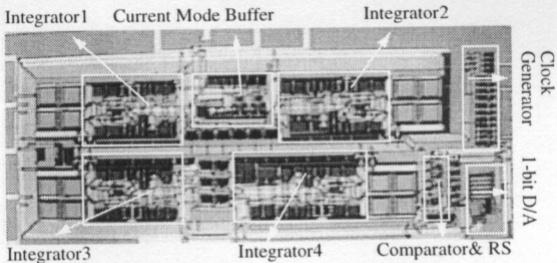


Fig. 9: Microphotograph of the BandPass  $\Sigma\Delta$  Modulator.