Reconfiguration of Cascade ΣΔ Modulators for Multistandard GSM/Bluetooth/UMTS/WLAN Transceivers

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***Abstract* – This paper presents design considerations for cascade Sigma-Delta Modulators (ΣΔMs) included in multistandard wireless transceivers. Four different standards are covered: GSM, Bluetooth, UMTS and WLAN. A top-down design methodology is proposed to find out the optimum modulator architecture in terms of circuit complexity and reconfiguration parameters. The selected 2-1^{L-2} expandible ΣΔM is high-level sized and several reconfiguration strategies are adopted at both architecture- and circuit-level in order to adapt the modulator performance to the different standards requirements with adaptive power consumption. Time-domain simulations are shown to validate the presented approach.**[†1]

I. INTRODUCTION

The extraordinary growth of wireless communication technologies has prompted the emergence of multitude of new applications and standards. These new standards —like IEEE 802.11 Wireless Local Area Network (WLAN) and Universal Mobile Telecommunications System (UMTS)— are complementing rather than replacing the existing ones —such as Global System for Mobile (GSM) communication— giving rise to the so-called *universal* or *multistandard* transceivers. These systems are able to operate over a variety of specifications, thus benefiting of the different services and functions offered by co-existing wireless standards [1].

Multistandard transceivers need to be implemented by reconfigurable building blocks that can be adapted to each specification with little adjustment made to their circuit parameters and with adaptive power consumption. One of the most challenging building blocks is the Analog-to-Digital Converter (ADC), because of the different sampling rates and dynamic ranges required to digitize the wide range of signals coming from each individual operation mode [2].

Sigma-Delta Modulators (ΣΔMs) are good candidates for the implementation of the ADC in multistandard, multimode communication systems [3][4]. On the one hand, these ADCs have lower sensitivity to circuitry imperfections than Nyquist-rate ADCs, thus making easier to include reconfigurability and programmability functions without significant performance degradation. On the other hand, ΣΔMs trade analog accuracy by signal processing, thus facilitating their integration in deep-submicron VLSI technologies, more suited to implement fast digital circuits than precise analog functions [5].

Several multistandard ΣΔM Integrated Circuits (ICs) have been reported up to now [6]-[10]. Most of them are based on reconfiguring architecture-level parameters (modulator order, oversampling ratio and/or number of bits of the internal quantizers), whereas less emphasis is normally put at circuit-level parameters.

This paper presents design considerations applicable to expandible cascade ΣΔMs intended for multistandard receivers, covering four standards: GSM, Bluetooth, UMTS, and WLAN. A complete top-down design procedure is described, putting special emphasis on optimizing the circuit design for different operation modes. To this purpose, different strategies are adopted at both architecture- and circuit-level in order to fulfil specifications with minimum power consumption.

II. MODULATOR ARCHITECTURE

The modulator in this paper has been designed to meet the requirements of direct-conversion receivers. This receiver architecture is commonly used in multistandard applications because it eliminates the need for both IF and image reject filtering and requires only a single oscillator and mixer [11]. The ADC effective resolution was extracted from an iterative simulation-based procedure considering the propagation of the different standard test signals through the receiver front-end. Table I lists the ADC specifications for the standards covered in this work.

Given that reconfigurability issues must be boosted in the targeted multistandard application, the expandible cascade ΣΔM in Fig.1 has been selected as the best suited architecture [12]. This cascade topology comprises a 2nd-order first stage followed by 1st-order stages, and can be easily extended to build a ΣΔM of a generic order L by simply adjusting the number of 1st-order stages. Note that every cascade ΣΔM belonging to the family in Fig.1 can be univocally described by three parameters: the modulator order (L), the oversampling ratio (OSR), and the number of bits in the last stage (B). Thus, a $\{L, B, OSR\}$ triad is used to codify them.

The first step in the design of the multistandard ΣΔM is the exploration of the $\{L, B, OSR\}$ candidates for each standard

TABLE I. ADC SPECIFICATIONS

	GSM	Bluetooth	UMTS	WLAN
Resolution	13bit	11bit	9bit	7bit
Bandwidth	200kHz	1MHz	3.84MHz	20MHz

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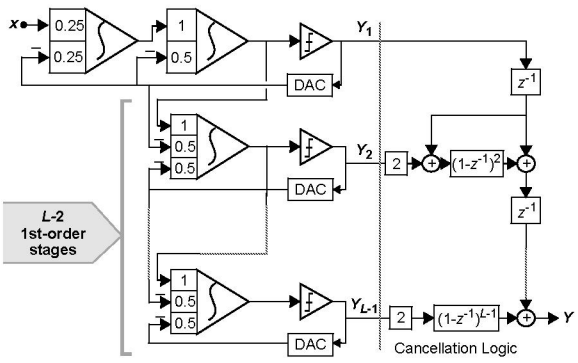

Figure 1. 2-1^{L-2} cascade ΣΔM.

that achieve minimum power consumption while fulfilling its corresponding requirements. At this step, an updated version of the analytical procedure described in [12] to estimate the power consumption of 2-1^{L-2} ΣΔMs has been followed. The procedure, based on compact expressions that contemplate both architectural and technological features, schematically consists of the following steps:

1) The in-band quantization error power (P_Q) is calculated for given values of $\{L, B, OSR\}$ and V_{ref}, considering also leakages due to capacitor mismatch, finite amplifier DC gain, and errors in the multibit quantizer (if $B > 1$).
2) The in-band error power due to circuit noise (P_{CN}) is considered. The value of the sampling capacitor at the modulator front-end (C_S) is selected so that $P_Q + P_{CN}$ is smaller than the maximum allowed total in-band error power. P_{CN} will be mainly contributed by kT/C noise, but some room is left at this step for the contribution of the front-end amplifier noise.
3) The amplifier Gain-Bandwidth product (GB) is estimated so that the in-band error power due to the integrator defective settling (P_{st}) is non-limiting ($P_{st} \ll P_Q + P_{CN}$). A linear settling model is used, considering that it takes a number $\ln(2^{ENOB})$ of time constants to settle within $ENOB$ resolution.
4) The amplifier GB is related to its power dissipation, for which the amplifier topology must be known a priori. Suitable candidates are closely related to the process technology: supply voltage, minimal device length, etc. Usual choices are folded cascodes for supplies above 3V or two-stage amplifiers below 2.5V. In our case fully differential folded-cascode opamps with a 3.3V supply will be assumed.
5) Once the power dissipation of the front-end integrator has been estimated, that of the remaining ones (with, in practice, less demanding specifications) is estimated as a fraction of it. The overall estimated modulator power is then basically obtained by adding up all contributions, together with the dynamic power in the SC stages.

Given the targeted multistandard application, the design space has been explored in terms of suitable $\{L, B, OSR\}$ triads for each standard by applying the former procedure under the next global constraints:

- The modulator reference is fixed to 1.2V in order to place the input signal level at -5.6dB below Full Scale (FS) (near the modulator overload) and maximize the $SNDR$.
- Given the targeted range of resolutions (≤ 13bit), the explored values of L are restricted to 2, 3, and 4.
- The sampling frequency (f_s) is restricted to values $\div 1$, $\div 2$, $\div 4$, etc., from a maximum of 160MHz, in order to make it easy the frequency division of a master clock frequency from one standard to another. This imposes a constraint on the practical OSR values that are explored and forces to expand the bandwidth in UMTS from 3.84MHz to 4MHz.
- The smallest value for the unit capacitor (C_u) is fixed to 0.25pF for mismatching issues.
- In order to simplify the circuit reconfiguration, the sampling capacitor at the modulator front-end can only take values that are multiple of C_u.

Table II summarizes the ranking of ΣΔMs with the lowest estimated power for each standard. Together with the values for $\{L, B, OSR\}$, those required for f_s and C_S, and the obtained Dynamic Range (DR) and $SNDR$ peak are also enclosed. The highlighted rows in Table II correspond to the ΣΔMs for each standard that we have selected for further consideration. Note that the rest of candidates are directly covered by the selected ones, since the former just imply an increase of the modulator order or of the internal multibit resolution. Thus, the selected ΣΔMs at this step globally comprise:

- 3rd- and 4th-order cascades.
- Single-bit and multibit quantization of 2, 3, 4, or 6 bits.
- Sampling frequencies of 20MHz, 40MHz, 80MHz, or 160MHz.

TABLE II. RANKING OF ΣΔMS ACCORDING TO THEIR ESTIMATED POWER

Standard	L	B	OSR	f_s (MHz)	C_S (pF)	DR (bit)	$SNDR_{peak}$ (bit)	Power (mW)
GSM	4	1	50	20	0.50	14.42	13.59	10.9
	3	2	50	20	0.50	14.39	13.56	11.7
	3	3	50	20	0.50	14.41	13.58	12.5
	4	2	50	20	0.50	14.42	13.59	13.4
	3	4	50	20	0.50	14.41	13.58	14.1
	4	3	50	20	0.50	14.42	13.59	14.2
	4	4	50	20	0.50	14.42	13.59	15.8
	3	1	100	40	0.25	14.42	13.59	17.0
	4	1	100	40	0.25	14.42	13.59	20.0
Bluetooth	4	1	20	40	0.25	12.82	11.99	18.1
	3	3	20	40	0.25	12.76	11.93	20.6
	3	4	20	40	0.25	13.05	12.22	22.5
	4	2	20	40	0.25	13.16	12.33	23.0
	4	3	20	40	0.25	13.21	12.38	23.9
	4	4	20	40	0.25	13.22	12.39	25.5
	3	1	40	80	0.25	13.40	12.57	32.1
UMTS	3	4	10	80	0.25	10.81	9.98	37.3
	4	2	10	80	0.25	10.45	9.62	38.6
	4	3	10	80	0.25	11.46	10.63	42.0
WLAN	3	6	4	160	0.25	8.12	7.29	70.9
	4	6	4	160	0.25	8.57	7.74	80.8

- Sampling capacitors of 0.25pF or 0.5pF.

These issues can be handled at circuit level, by reconfiguring the last stage of the expandible cascade to either single-bit or multibit with programmable resolution, by dividing the master clock frequency by a factor 2, 4, or 8, and by using switchable capacitors at the modulator front-end, respectively.

Seeking for a single circuit that covers all the former possibilities can a priori be done, but such a large degree of freedom in the reconfigurability will considerably increase the circuit complexity. Thus, only one $\{L, B, OSR\}$ triad will definitively be selected for each standard. However, given that the estimated power consumption is not very different from one case to another, the final decision will be taken after extracting their complete set of building-block requirements using more accurate behavioral simulations.

III. HIGH-LEVEL SYNTHESIS

The formerly selected candidates have been extensively simulated using SIMSIDES [13], a time-domain simulator for ΣΔ modulators that includes accurate behavioral models for thermal noise, integrator defective settling, distortion sources, etc. This way the architecture specifications can be mapped onto more refined building-block requirements in terms of amplifier DC gain, GB, Slew Rate (SR), equivalent input noise, switch on-resistance, etc.

The followed steps for this process are:

1) Validate that the ΣΔMs selected from Table II achieve the required DR for each standard, taking into account quantization error and kT/C noise.
2) Determine the maximum equivalent input noise for each amplifier that does not degrade the former performance.
3) Determine the required amplifier dynamics (GB and SR), taking into account settling errors during both the integration and sampling phases.
4) Refine the DC gain and SR requirements at each front-end integrator in order to limit the generated distortion near the modulator overload level.

At this step different amplifiers are considered for each integrator in order to gain insight on their individual needs. Once the final architecture is selected for each standard, the global amplifier specifications will be tried to be covered using reconfigurable amplifiers (in terms of bias currents and/or transistor sizings).

However, switches will not be reconfigured from one standard to another, so that they must be sized at this step taking into account their slow-down effect on the integrators dynamics and the dynamic distortion they introduce at the modulator front-end [14]. They have been sized to exhibit a maximum on-resistance around 250Ω, which does not to compromise settling nor distortion in the different standards and avoids the use of clock-boosting techniques.

The requirements of the selected ΣΔMs after the former fine-tuning process are summarized in Table III, in terms of the amplifier equivalent input noise, DC gain, and dynamics for each integrator.

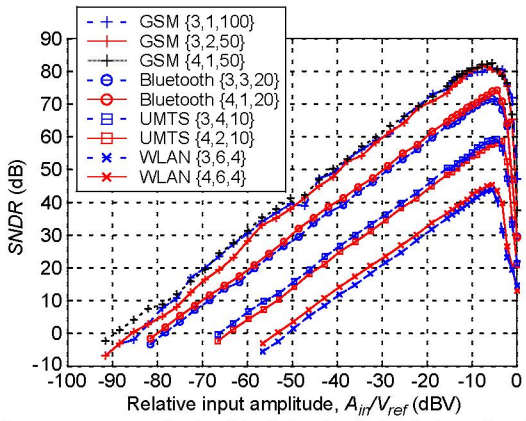

Figure 2. $SNDR$ curves obtained by behavioral simulation after the fine tuning of the building-block specifications.

IV. SIMULATION RESULTS

As shown in Fig.2, the modulator sizings in Table III achieve the specifications of the different standards. The figure depicts the $SNDR$ curves obtained by behavioral simulation and shows that the ΣΔMs exhibit an $SNDR$ peak larger than 81dB for GSM, 71dB for Bluetooth, 58dB for UMTS, and 44dB for WLAN.

Based on the results shown in Table III, especially on those related to the amplifier dynamics, the final selection of the ΣΔM architecture for each standard is:

- For GSM: $\{3, 1, 100\}$
- For Bluetooth: $\{4, 1, 20\}$
- For UMTS: $\{4, 2, 10\}$
- For WLAN: $\{3, 6, 4\}$

The selected $\{L, B, OSR\}$ triads have also the advantage of requiring the same sampling capacitor (0.25pF —see Table II), thus eliminating the need for switchable capacitor arrays at the modulator front-end. As an illustration, Fig.3 shows the modulator output spectra, based on a 65536-point FFT, obtained by behavioral simulation for GSM and WLAN.

CONCLUSIONS

A design methodology for the design of multistandard cascade ΣΔ modulators has been described. Both architecture and circuit-level reconfiguration strategies have been considered in order to find out the optimum architecture in terms of power dissipation and silicon area. As an application of the proposed methodology, the high-level design of a cascade ΣΔ modulator has been presented to cope with the requirements of several wireless standards.

REFERENCES

[1] X. Li and M. Ismail: *Multi-standard CMOS wireless receivers: analysis and design*. Kluwer Academic Publishers, 2002.

[2] K. Gulati and H.S. Lee: "A Low-Power Reconfigurable Analog-to-Digital Converter". *IEEE J. of Solid-State Circuits*, pp. 1900-1910, Dec. 2001.

[3] K.T. Tiew *et al.*: "MASH Delta-Sigma Modulators for Wideband and Multi-Standard Applications", *Proc. IEEE Int. Symp. on Circuits and*

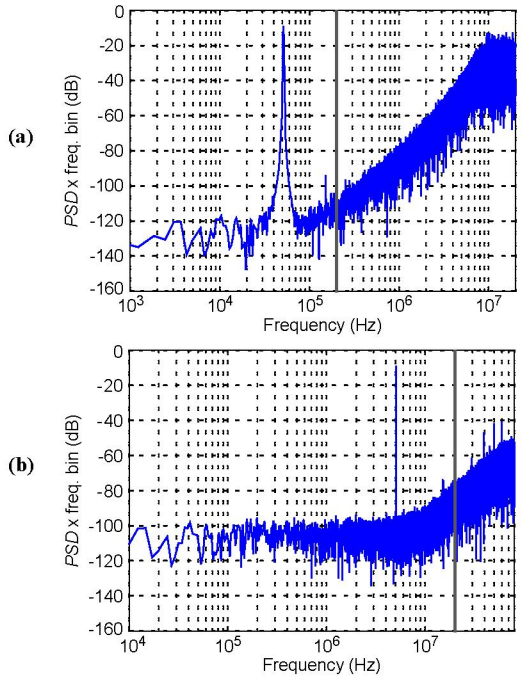

Figure 3. Modulator output spectra obtained by behavioral simulation for: (a) GSM; (b) WLAN.

Systems, pp. IV.778-781, 2001.

[4] B.J. Farahani and M. Ismail: "A Low Power Multi-Standard Sigma-Delta ADC for WCDMA/GSM/Bluetooth Applications", *Proc. IEEE Northeast Workshop on Circuits and Systems*, pp. 241-243, 2004.

[5] A. Rodríguez-Vázquez, F. Medeiro, and E. Janssens (Eds.): *CMOS Telecom Data Converters*. Kluwer Academic Publishers, 2003.

[6] T. Burger and Q. Huang: "A 13.5mW 185-Msample/s ΔΣ Modulator for UMTS/GSM Dual-Standard IF Reception". *IEEE J. of Solid-State Circuits*, pp. 1868-1878, Dec. 2001.

[7] G. Gomez and B. Haroun: "A 1.5V 2.4/2.9mW 79/50dB DR ΣΔ Modulator for GSM/WCDMA in a 0.13μm Digital Process". *Proc. IEEE Int. Solid-State Circuits Conf.*, pp. 1.306-307, 2002.

[8] L. Gardelli *et al.*: "Tunable Bandpass Sigma-Delta Modulator Using One Input Parameter". *Electronics Letters*, Vol. 39, no. 2, pp. 187-189, Jan. 2003.

[9] T.M.R. Miller and C.S. Petrie: "A Multibit Sigma-Delta ADC for Multimode Receivers". *IEEE J. of Solid-State Circuits*, pp. 475-482, March 2003.

[10] T.O. Salo *et al.*: "80-MHz Bandpass ΔΣ Modulators for Multimode Digital IF Receivers". *IEEE J. of Solid-State Circuits*, pp. 464-474, March 2003.

[11] A.A. Abidi: "Direct-conversion radio transceivers for digital communications". *IEEE J. of Solid-State Circuits*, pp. 1399-1410, Dec. 1995.

[12] F. Medeiro *et al.*: "High-Order Cascade Multi-bit ΣΔ Modulators". Chapter 9 at *CMOS Telecom Data Converters* (A. Rodríguez-Vázquez, F. Medeiro, and E. Janssens, Eds.). Kluwer Academic Publishers, 2003.

[13] J. Ruiz-Amaya *et al.*: "An Optimization-based Tool for the High-Level Synthesis of Discrete-time and Continuous-Time ΣΔ Modulators in the MATLAB/SIMULINK Environment". *Proc. IEEE Int. Symp. Circuits and Systems*, pp. V.97-100, 2004.

[14] R. del Río *et al.*: "Highly Linear 2.5-V CMOS ΣΔ Modulator for ADSL+". *IEEE Trans. on Circuits and Systems - I*, Vol. 51, pp. 47-62, Jan. 2004.

TABLE III. AMPLIFIER REQUIREMENTS AFTER FINE TUNING OF THE DIFFERENT $\{L, B, OSR\}$ CANDIDATES.

Standard	{*L*, *B*, *OSR*}	Integrator	Amplifier input noise ($nV/\sqrt{Hz}$)	Amplifier DC gain	Transconductance (mA/V)	Maximum Output Current (μA)	Equivalent capacitive load (pF)	*GB* (MHz)	*SR* (V/μs)
GSM	{3, 1, 100}	#1	7.0	1500	0.26	150	3.51	11.9	55.1
		#2	135.0	250	0.42	130	5.67	11.7	47.0
		#3	237.5	250	0.19	60	5.67	5.4	21.7
	{3, 2, 50}	#1	6.0	700	0.42	200	3.70	18.1	68.1
		#2	32.5	400	0.62	130	5.67	17.3	47.0
		#3	225.0	250	0.23	130	16.03	2.3	25.1
	{4, 1, 50}	#1	6.0	800	0.39	200	3.71	16.7	67.9
		#2	12.5	250	0.86	120	5.67	24.2	43.4
		#3	125.0	250	0.25	170	5.67	7.1	61.5
		#4	212.5	250	0.23	50	5.67	6.5	18.1
Bluetooth	{3, 3, 20}	#1	8.0	2000	1.36	240	3.51	61.8	88.2
		#2	26.0	550	2.52	300	5.67	70.8	108.5
		#3	49.0	350	4.04	1000	16.03	40.1	193.4
	{4, 1, 20}	#1	7.0	2000	1.25	320	3.51	56.8	117.6
		#2	12.0	350	2.52	300	5.67	70.8	108.5
		#3	19.0	400	1.19	750	5.67	33.4	271.2
		#4	40.0	300	0.46	375	5.67	12.9	135.6
UMTS	{3, 4, 10}	#1	18.0	2500	2.39	413	3.53	107.6	150.9
		#2	12.0	500	6.40	800	5.70	178.8	289.1
		#3	35.0	400	13.26	2550	16.15	130.7	492.6
	{4, 2, 10}	#1	11.0	1800	2.62	506	3.53	118.3	184.9
		#2	18.0	400	6.19	750	5.70	172.9	271.1
		#3	45.0	450	8.14	1000	5.70	227.4	361.4
		#4	35.0	450	6.61	1000	16.15	65.2	193.2
WLAN	{3, 6, 4}	#1	45.0	1000	8.78	750	3.65	382.8	271.2
		#2	30.0	1375	21.50	1700	5.90	579.9	610.9
		#3	22.5	675	28.45	7000	16.83	269.1	1351.8
	{4, 6, 4}	#1	45.0	1500	8.77	825	3.67	380.1	299.0
		#2	17.0	1000	24.29	1600	5.93	651.8	577.4
		#3	20.0	525	17.29	2750	5.93	464.0	992.4
		#4	47.5	650	19.26	3150	16.95	180.9	607.7