CMOS Sigma-Delta Converters – From Basics to State-of-the-Art

Circuits and Errors

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OUTLINE

1. Circuits and Errors in DT $\Sigma\Delta$ Modulators
   - Errors degrading NTF
   - Additive noise sources
   - Harmonic distortion
   - Case study

2. Circuits and Errors in CT $\Sigma\Delta$ Modulators
   - CT $\Sigma\Delta$M subcircuits
   - Building-block errors
   - Architectural timing errors
   - Case study

3. Layout & Prototyping
   - Layout floorplanning
   - Chip package
   - Test PCB and Set-up
DT-ΣΔMs: Overview of Non-idealities

- Ideal In-Band Error Power:
  \[ P_{\text{Ideal}} = \frac{1}{12} \left( \frac{\Delta}{2^n - 1} \right)^2 \frac{\pi^{2L}}{(2L+1)\text{OSR}^{2L+1}} \]
- Actual In-Band Error Power:
  \[ P_r = P_{\text{Ideal}} + P_{\text{Noise}} + P_{\text{Non-linearity}} + \ldots \]

- Capacitors:
  - Mismatch
  - Non-linearity

- Amplifiers:
  - Output swing
  - DC gain
  - Dynamic limitations (GB, SR)
  - Thermal and 1/f noise
  - Gain non-linearity

- Switches:
  - Finite on-resistance
  - Thermal noise
  - Charge injection
  - Clock feedthrough
  - Non-linearity

- Capacitors:
  - Mismatch
  - Non-linearity

- Comparators:
  - Hysteresis
  - Offset

- References:
  - Thermal and 1/f noise
  - Output impedance

- Multi-bit ADCs & DACs:
  - Gain error
  - Offset error
  - Non-linearity

- Depending on the building-block:
  Depending on the building-block:
  Depending on the building-block:

- Fully-diff SC schematic of a 2nd-order ΣΔM

- Clock:
  - Jitter

- References:
  - Thermal and 1/f noise
  - Output impedance

- Multi-bit ADCs & DACs:
  - Gain error
  - Offset error
  - Non-linearity
DT-ΣΔMs: Overview of Non-idealities

Depending on their effect:

**ERRORS DEGRADING NTF**
- **AMPLIFIER DC_GAIN**
- **CAPACITOR MISMATCH**
- **INTEGRATOR SETTLING**
  - Amplifier GB
  - Amplifier SR
  - Switch R\textsubscript{on}

**SINGLE-LOOP ΣΔMs**
- Low sensitivity

**CASCADE ΣΔMs**
- **Noise leakages**
  - Imperfect cancellation of low-order quantization errors

**MODELED AS ADDITIVE ERRORS**
- **CIRCUIT NOISE**
  - Thermal noise (switches, opamps, refs)
  - 1/f noise (opamps, refs)
- **CLOCK JITTER**
- **DISTORTION**
  - Non-linear amplifier gain
  - Non-linear capacitors
  - Non-linear settling
  - Non-linear switches

Front-end dominates

Similar impact on different topologies
**DT-ΣΔMs: Integrator Leakage**

- **Effect of amplifier gain on the integrator transfer function:**

  *Ideal SC integrator*

  \[ g = \frac{C_1}{C_2} \]

  \[ v_{o,n} = v_{o,n-1} + g \cdot v_{i,n-1} \]

  \[ \mathcal{H}(z) = g \frac{z^{-1}}{1 - z^{-1}} \]

  \[ v_{o,n} = \frac{1}{1 + (1 + g) A_{DC}^{-1}} \left[ \mathcal{H}(z) \cdot v_{o,n-1} + g \cdot v_{i,n-1} \right] \]

  \[ \mathcal{H}(z) \equiv g \frac{z^{-1}}{1 - z^{-1} \left( 1 - \frac{g}{A_{DC}} \right)} = g \frac{z^{-1}}{1 - z^{-1} (1 + \mu)} \]

  \[ \mu = \frac{1}{A_{DC}} \]

  **Shift of the pole from DC (z = 1)**

- **Effect on single-loop ΣΔMs:**

  - **Ideally:**
    \[ \mathcal{H}(z) = \frac{z^{-1}}{1 - z^{-1}} \]
    \[ Y(z) = z^{-2}X(z) + (1 - z^{-1})^2 E(z) \]

  - **In practice:**
    \[ \mathcal{H}(z) = \frac{z^{-1}}{1 - z^{-1} (1 - \mu)} \]
    \[ NTF(z) = [1 - z^{-1} (1 - \mu)]^2 \]
    \[ = (1 - z^{-1})^2 + 2 \mu z^{-1} (1 - z^{-1}) + \mu^2 z^{-2} \]
    \[ P_0(\mu) \approx \frac{\Delta^2}{12} \frac{\pi^4}{5 OSR^2} + \frac{\Delta^2}{12} \frac{\pi^2}{2 OSR^2} + \frac{\Delta^2}{12} \frac{1}{OSR^2} \]

  **Lth-order ΣΔM:**

  \[ \Delta P_0 \approx \frac{\Delta^2}{12} \frac{1}{(2L - 1) OSR^{2L-1}} \]

  *Quite insensitive to leakages (\(\mu^2, L-1\) shaping)*

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Effect on cascade $\Sigma\Delta$Ms:

- Ideally:
  \[ Y(z) = STF(z)X(z) + NTF(z)E(z) + NTF(z)E(z) + NTF(z)E(z) \]
  \[ = z^{-4} STF(z) + 0 NTF(z) + d_3(1-z^{-1})^4 \]

- In practice:
  \[ H(z) = \frac{z^{-4}}{1-z^{-1}(1-\mu)} \]

Mismatch between analog and digital filtering

- Sensitivity to integrator leakages of cascades increases with OSR and $L$
- 1st-stage leakages dominate ($L_1$-1 shaping)

Comparison of integrator leakage effect on 4th-order $\Sigma\Delta$Ms

- Ideally:
  \[ H_1(z) = z^{-1} \]
  \[ H_2(z) = (1-z^{-1})^2 \]
  \[ H_3(z) = z^{-1} \]
  \[ H_4(z) = (1-z^{-1})^3 \]

- In practice:
  \[ P_0(z) = \frac{\mu}{125(\mu+2\pi^2\text{OSR}^2) + \frac{\mu^2\pi^2}{\text{OSR}^2}} \]

- Low-order leakages ($L_1$-1, $L_2$-1, ...)

→ Sensitivity to integrator leakages of cascades increases with OSR and $L$
→ 1st-stage leakages dominate ($L_1$-1 shaping)
DT-ΣΔMs: Capacitor Mismatch

Circuit primitive:

Physical implementations:

"Analog" CMOS

"Digital" CMOS

"Mixed" CMOS

Density
Linearity
Temperature
Parasitics
Matching

MOS cap

Local and global errors in:

C = C_{ox} \times (W \cdot L)

Actual ≠ Ideal

Edge Errors

Errors in thickness and dielectric constant gradient

Area

Capacity per Unit Area

\[ g = \frac{C_1}{C_2} = \frac{n C_u}{m C_m} \]

\[ \sigma_c \sim 0.05\% - 0.1\% \]

using good quality caps and adequate layout strategies

Centroid techniques
**DT-ΣΔMs: Capacitor Mismatch**

### Effect on single-loop ΣΔMs:

- **2nd-order ΣΔM**
  
  - Ideally:
    
    \[
    g_1 = g_1' \quad g_2 = 2g_1'g_2 \\
    Y(z) = z^{-2}X(z) + (1 - z^{-1})^2E(z)
    \]

  - In practice:
    
    \[
    g_1^\# = g_1(1 \pm \varepsilon_{g_1}) \quad \sigma_{g_1} = \frac{\sigma_{g_1}}{g_1} = \frac{1}{m_i} \sigma_C
    \]

    \[
    STF(z) \equiv (1 - |\varepsilon_{g_1} - \varepsilon_{g_1}'|)z^{-2} \equiv z^{-2}
    \]

    \[
    NTF(z) \equiv \frac{1}{1 + \varepsilon_{g_1}}(1 - z^{-1})^{-2}, \quad \varepsilon_g = \varepsilon_{g_2} + \varepsilon_{g_1}'
    \]

    Slight increase of error, but shaping is preserved

    \[
    P_Q(\varepsilon_g) \equiv \frac{1}{12} \left( \frac{1 + \varepsilon_{g_1}}{5 OSR} \right)^2
    \]

### Effect on cascade ΣΔMs:

- **2-1-1 ΣΔM**

  - Ideally:
    
    \[
    Y(z) = STF(z)X(z) + NTF_1(z)E_1(z) + NTF_2(z)E_2(z) + NTF_3(z)E_3(z)
    \]

    \[
    \begin{align*}
    STF(z) &= z^{-4} \\
    NTF_1(z) &= 0 \\
    NTF_2(z) &= 0 \\
    NTF_3(z) &= d_1(1 - z^{-1})^4
    \end{align*}
    \]

  - In practice:
    
    \[
    g_1^\# = g_1(1 \pm \varepsilon_{g_1})
    \]

    Mismatch between analog and digital coeffs

    Low-order leakages (\(L_1, L_2, \ldots\))
**DT-ΣΔMs: Capacitor Mismatch**

- **Effect on cascade ΣΔMs:**

  ![Graph showing SNDR vs Relative input amplitude for 2-1-1 ΣΔM (OSR = 32) with capacitor mismatch effects.]

  - $\sigma_C = 0.5\%$
  - $\sigma_C = 0.1\%$

- **Effect on cascade ΣΔMs:**

  Required $\sigma_C$ for 1-bit loss in DR

  ![Graph showing $\sigma_C$ vs Oversampling ratio (OSR) for different configurations (2-2, 2-2-2, 2-1, 2-1-1, 2-1-1-1).]

  - Sensitivity to mismatch rapidly increases with:
    - Oversampling ratio (OSR)
    - Cascade order ($L$)

  1st-stage leakages dominate ($L_1$ shaping)
If only amplifier gain is considered, the relation between $v_o$ and virtual ground is assumed to be independent on time.

In practice, this relation depends on time.

Integrator temporal evolution:
- error due to amplifier finite bandwidth
- slew-rate limitation

Modulator output spectrum:
- increase on the noise floor
- harmonic distortion due to slewing

SNDR degradation

Integrator temporal evolution: [Rio00]
- Both integration and sampling dynamics considered
- 1 pole model + SR limitation in amplifiers
- All parasitic caps taken into account

Amplifier Model
- Single-pole non-linear Dynamic

Bottom plate parasitics considered
DT-$\Sigma\Delta$Ms: Integrator Incomplete Settling

Integrator temporal evolution: [Rio00]

\[ v_{o}(t) = \frac{1}{2} \left( \frac{C_{o}}{C_{m}} \right) \left( \frac{1}{\exp(\frac{t}{T_{S}})} - 1 \right) + \frac{1}{2} \left( \frac{C_{o}}{C_{m}} \right) \left( \frac{1}{\exp(\frac{t}{T_{S}})} + 1 \right) \]

\[ v_{o}(t) = v_{r_{i}}, n = 1 \left( \frac{1}{C_{o}} C_{i} \right) v_{i}(t) \left( \frac{T_{S}}{2} \right) \]

**Integration-Phase:**
- finite opamp dynamic
- linear operation or slew

**Sampling-Phase:**
- finite opamp dynamic
- linear operation or slew

\[ C_{eqf} = C_{i} + C_{p} + C_{o}(1 + \frac{C_{p} - C_{o}}{C_{o}}) \]

\[ C_{eqs} = C_{p} + (C_{j} + C_{n1} + C_{n2})(1 + \frac{C_{p}}{C_{o}}) \]

\[ v_{o}(T_{S}) = v_{o}(\frac{T_{S}}{2}) \left( 1 + \frac{C_{o} - C_{i}}{C_{o}} \right) \]

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\begin{multicols}{2}

**DT-ΣΔMs: Integrator Incomplete Settling**

**Integrator temporal evolution:** [Rio00]

\begin{center}
\begin{tabular}{|c|c|}
\hline
INTEGRATION & SAMPLING \\
\hline
1 & LINEAR \\
2 & PARTIAL SLEW \\
3 & SLEW \\
4 & LINEAR \\
5 & PARTIAL SLEW \\
6 & SLEW \\
7 & LINEAR \\
8 & PARTIAL SLEW \\
9 & SLEW \\
\hline
\end{tabular}
\end{center}

\[ v_n(t) = \frac{C_1}{C_0} (V_{12} - V_{11}) - \frac{C_1}{C_0} V_{12} - V_{11} + \Theta(t-T_{S/2}) \times \Theta(t-T_{S/2}) \]

Traditionally not taken into account

- **Effect of the amplifier GB:**
  - If only amplifier GB is considered (assuming no SR limitation)
  - Can be viewed as a systematic error in the integrator weight
  - Effect on ΣΔMs similar to a mismatch between analog and digital coeffs
  - It causes low-order noise leakages in cascade ΣΔMs

\end{multicols}
**DT-ΣΔMs: Integrator Incomplete Settling**

- **Additional effect of the amplifier SR (+ GB):**
  - "Dominant" linear dynamics are not mandatory in order to fulfill specs
  - SR can trade for GB
  - It can be used to optimize the power consumption of amplifiers

- Non-linear dynamics cause distortion!
  - SR at the front-end integr must be carefully tackled

**Graph:**

- **Half-scale SNDR (dB):**
  - Normalized amplifier SR

- **INTEGRATION:**
  - Linear settling
  - Full-slew

- **SAMPLING:**
  - Linear settling
  - Full-slew

**Additional effect of the switches Ron (+ GB + SR):**

- Input is sampled with an error
  - \[ v_{in,s} = \exp \left( \frac{-1}{2R_{on}C_{S}^{2}} \right) \]

- Linear dynamics are slowed down
  - \[ GB_{l, on} = \frac{GB}{1 + GB \cdot 2R_{on}C_{S}} \]
  - \[ GB_{s, on} = \frac{GB}{1 + GB \cdot 2R_{on}C_{S}} \]

- Slew time shortens
Main noise sources in SC integrators:

- Switches → Thermal noise
- Amplifiers → Thermal and flicker noise
- References → Thermal and flicker noise

**Noise contribution of the switches (input-referred):**

Switches for sampling

\[
S_X = 2kT \cdot 2R_{on}
\]

\[
BW_{n,S_X} = \int_{0}^{\infty} |H_{S_X}(f)|^2 df = \frac{1}{4 \cdot 2R_{on} C_S}
\]

\[
S_m,S_X(f) \equiv \frac{2BW_{n,S_X}}{f_s} : \frac{kT}{C_S f_s}
\]

Aliased component: [Fisc82]
DT-ΣΔMs: Circuit Noise

Noise contribution of the amplifier (input-referred):

- **Thermal component**
  \[ S_{\text{Th}}(f) = \frac{1}{(1+s/p_1)(1+s/p_2)} \]
  \[ BW_{\text{Th}} = \frac{2}{4} \frac{1}{p_1} \]
  \[ S_{\text{Th,op}}(f) = \frac{2}{f_s} \frac{BW_{\text{Th}}}{f} \cdot S_{\text{Th}}^t \]

- **Flicker component**
  \[ S_{\text{F}}(f) = S_{\text{op}}^f \cdot \frac{f_{cr}}{f} \]

  Low-pass filtered version at the integ input:
  \[ S_{\text{F,op}}(f) = S_{\text{op}}^f \cdot \frac{f_{cr}}{f} \]

  Folded tails are “submerged” into the aliased thermal noise

Total noise PSD for the front-end integ:

\[ S_{\text{eq, in}}(f) = \frac{2kT}{C_s} \frac{S_{\text{Th}}}{2f_s} + \frac{S_{\text{op}}}{2f_s} \left( GB + \frac{f_{cr, op}}{f} \right) + \frac{S_{\text{ref}}}{2f_s} \left( GB_{\text{ref}} + \frac{f_{cr, ref}}{f} \right) \]

Switches:
- kT/C is the ultimate limitation on the converter resolution
- It can only be decreased by increasing Cs and/or fs (it does not depend on Ron!)
- ×2 in fully-diff implementations (3-dB increase, but signal power is 6dB larger!)

Amplifiers & References:
- GBs should be as low as settling errors allow (reduces folding!)
- 1/f contributions decrease with the corner frequency
- Adequate techniques can be applied in low-freq apps: CDS, chopper, … [Enz96]

\[ P_{\text{CN, in}} = \frac{2kT}{C_s} \left( \frac{S_{\text{Th}}}{2f_s} + \frac{S_{\text{op}}}{2f_s} + \frac{S_{\text{ref}}}{2f_s} \right) + \ln \left( \frac{f_p}{f_0} \right) \left( S_{\text{op}} f_{cr, op} + S_{\text{ref}} f_{cr, ref} \right) \]

In-band error power due to circuit noise in the ΣΔM

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Effect of noise leakages and thermal noise on a 2-1 cascade

Effect of 1/f and thermal noise on the spectra of a 4th-order \( \Sigma \Delta M \)
(silicon results for several fs)

Be careful with Flicker models for transistors!
Front-end amplifier needed redesign!
## DT-$\Sigma\Delta$Ms: Clock Jitter

- **Sampling time uncertainty** [Boser88]:
  \[ S_J = \frac{A_J^2}{2} \left( 2\pi f_s \sigma_J \right)^2 \]

- If jitter is modeled as random:
  \[ P_J = \frac{A_J^2}{2} \left( 2\pi f_s \sigma_J \right)^2 \text{OSR} \]

  Error is larger, the larger input freq (wideband apps!)

## DT-$\Sigma\Delta$Ms: Non-linearity of Capacitors

- In an ideal capacitor: \( dq = CdV \)
- In practice: \( dq = C(V)dv \), with \( C \) being voltage-dependent
  \[ C(V) = C(1 + a_1 V + a_2 V^2 + ...) \]

- Considering the effect of the sampling cap only [Bran97]:
  \[
  V_{o,n} = V_{o,n-1} + g_1 V_{in,n-1} \left( 1 + \frac{a_1}{2} V_{in,n-1} + \frac{a_2}{3} V_{in,n-1}^2 \right)
  \]

  - Even-order distortion cancels w/ fully-diff
  - Non-linearity of sampling cap dominates
  - Valid for weak non-linearities (MOS caps are very non-linear!)

- Ideal
  \[ \sigma_J = 0.1 \text{ns}, f_s = 125 \text{kHz} \]
  \[ \sigma_J = 0.1 \text{ns}, f_s = 500 \text{kHz} \]

- Non-uniform sampling of the input

- Error is larger, the larger input freq (wideband apps!)

- Even-order distortion cancels w/ fully-diff
- Non-linearity of sampling cap dominates
- Valid for weak non-linearities (MOS caps are very non-linear!)

- \( a_1 = 500 \text{ppm/V}, a_2 = 500 \text{ppm/V}^2 \)

- \( HD_2 = -94.0 \text{dB} \)
- \( HD_2 = -89.9 \text{dB} \)
- \( HD_2 = -89.8 \text{dB} \)
DT-$\Sigma\Delta$Ms: Non-linear Amplifier Gain

- Actual amplifier gain depends on output voltage:

$$A_{DC} = 500, \gamma_1 = 10\%/V \text{ (single-ended $\Sigma\Delta$M)}$$

- Increasing $A_{DC}$ helps a lot!
- $A_{DC}$ at the front-end larger than noise leakages require

$$A_{DC}(V_o) = A_{DC}(1 + \gamma_1 V_o + \gamma_2 V_o^2 + \ldots)$$

$$HD_2 = 20\log_{10} \left( \frac{\gamma_1 \left(1 + g\right)}{A_{DC}} \right) g A_x$$

$$HD_3 = 20\log_{10} \left( \frac{\gamma_2 \left(1 + g\right)}{4 A_{DC}} \right) g^2 A_x^2$$

[Ref: Yin94]

DT-$\Sigma\Delta$Ms: Non-linear Settling

- SR can trade for GB in the integrator settling, but non-linear dynamics cause distortion:

$$I_o (\mu A)$$

$$\text{Settling time (ns)}$$

HD$_2$ at the front-end larger than settling requires
DT-ΣΔMs: Non-linear Switch Resistance

Switches exhibit a finite $R_{ON}$ which is also non-linear:

- Non-linear sampling [Geer02]:
  - Distortion is dynamic (increases with input freq!)
  - Front-end switch dominates
  - $R_{ON}$ at the front-end smaller than settling requires
  - Very important in low-voltage!

DT-ΣΔMs: Comparators and Multi-bit Quantizers

- **Single-bit ΣΔMs:**
  - Comparator:
    - Offset $\rightarrow$ Attenuated by the integrator DC gain
    - Hysteresis $\rightarrow$ Shaped similarly to quantization error [Boser88]
      \[ P_h = 4h^2 \frac{\pi^2 L}{(2L+1)OSR^{2L+1}} \]

- **Multi-bit ΣΔMs:**
  - Multi-bit ADC $\rightarrow$ Errors attenuated/shaped
  - **Multi-bit DAC** $\rightarrow$ Non-linearity directly added to the input!

Effect of DAC errors on a 2nd-order 3-bit ΣΔM

[Mede99]: \[ \sigma^2_{\text{INL}} = \frac{1}{2} \left( \frac{A}{2^B - 1} \right)^2 \text{INL}^2 \text{LSB} \]

DEM techniques: Dual quantization
2-1-1 w/ dual quantization

- Two different amplifiers: 2-stage OA in the 1st stage, and 1-stage OA in 2nd and 3rd stages.
- Standard CMOS switches (no clock-boosting).
- Only 2-branch integrators and 2x16 unit capacitors (MIM).
- Comparators: regenerative latch + preamplification stage.
- 3-bit quantizer in the last stage:
  - Resistive-ladder DAC (no calibration).
  - Flash ADC: Static differential input stage + latched comparators.
- Power-down control.

---

### Blocks Specs

#### EQUATION DATABASE

<table>
<thead>
<tr>
<th>Quantization noise</th>
<th>Typical</th>
<th>Worst Case</th>
</tr>
</thead>
<tbody>
<tr>
<td>DC gain</td>
<td>90.3dB</td>
<td>86.2dB</td>
</tr>
<tr>
<td>Cap.</td>
<td>Temperature range: -40ºC to +110ºC</td>
<td>88.4dB</td>
</tr>
<tr>
<td>DAC error</td>
<td>96.4dB</td>
<td>84.5dB</td>
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<tr>
<td>Thermal noise</td>
<td>84.8dB</td>
<td>82.2dB</td>
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<tr>
<td>kT/C noise</td>
<td>88.1dB</td>
<td>86.0dB</td>
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<tr>
<td>Amplifier noise</td>
<td>87.5dB</td>
<td>84.5dB</td>
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<tr>
<td>Clock jitter</td>
<td>-90.1dB</td>
<td>-89.3dB</td>
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<tr>
<td>In-band error power</td>
<td>82.3dB</td>
<td>80.3dB</td>
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<tr>
<td>Dynamic range</td>
<td>88.8dB</td>
<td>80.8dB</td>
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</tbody>
</table>

#### Blocks Specs

<table>
<thead>
<tr>
<th>MODULATOR</th>
<th>Topology: 2-1-1(3b)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Oversampling ratio</td>
<td>16</td>
</tr>
<tr>
<td>Reference voltage</td>
<td>1.5V</td>
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<tr>
<td>Clock frequency</td>
<td>70.4MHz</td>
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<tr>
<td>Clock jitter</td>
<td>15ps (0.1%)</td>
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<tr>
<td>DAC error</td>
<td>0.66pF</td>
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<tr>
<td>Cap. tolerance</td>
<td>±20%</td>
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<tr>
<td>Bottom parasitic cap.</td>
<td>1%</td>
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<tr>
<td>Switch on-resistance</td>
<td>150Ω</td>
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<tr>
<td>DC gain</td>
<td>3000 (70dB)</td>
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<tr>
<td>GB (1.5pF)</td>
<td>265MHz</td>
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<td>Slew rate (1.5pF)</td>
<td>800V/μs</td>
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<td>Output swing</td>
<td>±1.8V</td>
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<tr>
<td>Input equivalent noise</td>
<td>6nV/√(Hz)</td>
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<td>Hysteresis</td>
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<td>Offset</td>
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<tr>
<td>Resolution time</td>
<td>3ns</td>
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<tr>
<td>3-bit QUANTIZER</td>
<td>DAC INL: 0.5%FS</td>
</tr>
</tbody>
</table>

**Corner analysis:**
- Fast and slow devices
- Temperature range: [-40ºC, +110ºC]
- ±5% variation in the 2.5-V supply
DT-ΣΔMs: Case Study

\[ P_{CN} = P_{KTC} + P_{op} = \frac{4K T C}{f_0} + \frac{2\pi GB}{2OSK} \]

\[ GB_{eff} = \frac{GB}{1 + GB/f_{sm}} = \frac{GB}{1 + GB \cdot 2\pi \cdot 2R_m C_S} \]

<table>
<thead>
<tr>
<th>Typical</th>
<th>Worst Case</th>
</tr>
</thead>
<tbody>
<tr>
<td>Quantization noise</td>
<td>-88.1dB</td>
</tr>
<tr>
<td>Ideal</td>
<td></td>
</tr>
<tr>
<td>DC gain leakage</td>
<td>-99.8dB</td>
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<tr>
<td>Capacitor mismatch leakage ((\sigma_c = 0.05% \text{ or } 0.1%))</td>
<td>-95.4dB</td>
</tr>
<tr>
<td>DAC error</td>
<td>-96.4dB</td>
</tr>
<tr>
<td>Thermal noise</td>
<td>-84.8dB</td>
</tr>
<tr>
<td>(kT/C) noise</td>
<td>-88.1dB</td>
</tr>
<tr>
<td>Amplifier noise</td>
<td>-87.5dB</td>
</tr>
<tr>
<td>Clock jitter</td>
<td>-90.1dB</td>
</tr>
<tr>
<td>In-band error power</td>
<td>-82.3dB</td>
</tr>
<tr>
<td>Dynamic range</td>
<td>82.8dB (13.5bit)</td>
</tr>
</tbody>
</table>

- **MODULATOR**
  - Topology: 2-1-1(3b)
  - Oversampling ratio: 16
  - Reference voltage: 1.5V
  - Clock frequency: 70.4MHz
  - Clock jitter: 15ps (0.1%)

- **FRONT-END INTEGRATOR**
  - Sampling capacitor: 0.66pF
  - Cap. sigma (MIM, 1pF): 0.05%
  - Cap. tolerance: +20%
  - Bottom parasitic cap.: 1%
  - Switch on-resistance: 150Ω

- **AMPLIFIER**
  - DC gain: 3000 (70dB)
  - \(GB\) (1.5pF): 265MHz
  - Slew rate (1.5pF): 800V/μs
  - Output swing: ±1.8V
  - Input equivalent noise: 6nV/sqrt(Hz)

- **COMPARATORS**
  - Hysteresis: 20mV
  - Offset: ±10mV
  - Resolution time: 3ns

- **3-bit QUANTIZER**
  - DAC INL: 0.5%FS

**Integrator Dynamics**

- **GB > 2.5f_s** is ideally enough to limit settling errors (this architecture w/ OSR = 16).

- **Switch on-resistance** slows down the effective amplifier response:

\[ GB_{eff} = \frac{GB}{1 + GB/f_{sm}} = \frac{GB}{1 + GB \cdot 2\pi \cdot 2R_m C_S} \]

\[ R_m \sim 150\Omega \text{ requires just } GB > 3.2f_s \]

**Standard switches** (no clock-boosting) (assuming that 85% of the clock cycle is useful)

- Slew rate must be large enough to let the linear dynamic to correctly settle.

\[ SR/(V_{ref} \cdot f_s) = 6.5 \]

\[ SR = 800V/\mu s \]

- Partially slew-rate limited operation of the front-end integrator introduces distortion.

\[ GB = 265MHz \]

\[ R_m = 0\Omega \quad (f_m = -) \]
\[ R_m = 150\Omega \quad (f_m = 11.4f_s) \]
\[ R_m = 300\Omega \quad (f_m = 5f_s) \]
\[ R_m = 500\Omega \quad (f_m = 3.4f_s) \]
DT-ΣΔMs: Case Study

Amplifiers

<table>
<thead>
<tr>
<th>INTEGR. 1</th>
<th>INTEGR. 2</th>
<th>INTEGR. 3</th>
<th>INTEGR. 4</th>
</tr>
</thead>
<tbody>
<tr>
<td>Unit capacitor</td>
<td>0.66pF</td>
<td>0.45pF</td>
<td>0.45pF</td>
</tr>
<tr>
<td>DC gain</td>
<td>3000 (70dB)</td>
<td>600 (56dB)</td>
<td></td>
</tr>
<tr>
<td>GB (1.5pF)</td>
<td>265MHz</td>
<td>210MHz</td>
<td></td>
</tr>
<tr>
<td>Slew rate (1.5pF)</td>
<td>800V/μs</td>
<td>350V/μs</td>
<td></td>
</tr>
<tr>
<td>Output swing</td>
<td>±1.80V</td>
<td>±1.60V</td>
<td></td>
</tr>
<tr>
<td>Input equivalent noise</td>
<td>6nV/sqrt(Hz)</td>
<td>50nV/sqrt(Hz)</td>
<td></td>
</tr>
</tbody>
</table>

OPA

OPB

- SC CMFB nets
- pMOS input scheme
- Cancelled body effect (substrate noise coupling)
- Smaller 1/f noise

Input equivalent noise

Output swing

Slew rate (1.5pF)

GB (1.5pF)

DC gain

Unit capacitor

Power consumption

19.4mW

17.2mW

129F

126F

Typical | Worst Case |
<table>
<thead>
<tr>
<th></th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td>DC gain</td>
<td>78.6dB</td>
</tr>
<tr>
<td>GB (1.5pF)</td>
<td>446.8MHz</td>
</tr>
<tr>
<td>PM (1.5pF)</td>
<td>64.0º</td>
</tr>
<tr>
<td>SR (1.5pF)</td>
<td>1099V/μs</td>
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<tr>
<td>Output swing</td>
<td>±2.09V</td>
</tr>
<tr>
<td>Input eq. noise</td>
<td>5.1nV/sqrt(Hz)</td>
</tr>
<tr>
<td>Input capacitance</td>
<td>126F</td>
</tr>
<tr>
<td>Power consumption</td>
<td>17.2mW</td>
</tr>
</tbody>
</table>
DT-ΣΔMs: Case Study

### Amplifiers

<table>
<thead>
<tr>
<th></th>
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<td></td>
<td></td>
</tr>
</tbody>
</table>

- SC CMFB nets
- pMOS input scheme
  - Cancelled body effect (substrate noise coupling)
  - Smaller 1/f noise

### OPB folded-cascode amplifier

**Switch on-resistance**
- Slow-down of the integrators dynamics
- Incomplete sampling (RC time constant)
- Dynamic distortion (front-end integrator)

**Standard CMOS switches**
- No clock-boosting
- No low-Vt transistors
DT-ΣΔMs: Case Study

Switch on-resistance

Dynamic distortion evaluated through electrical simulation

- Sinewave input
  \( THD < -96\text{dB} \)

- DMT input
  \( MTPR < -81\text{dB} \)

MiM capacitors

CMOS tech with mixed-signal facilities

Thin oxide between metal 4 and metal 5

- Cap. matching: 0.05\% (1pF)
- Bottom plate parasitic: 1\%
- Cap. spread: ±20\%

- Very good matching (0.1\% assumed for 6-\( \sigma \) design)
- Helps to limit the capacitive load to integrators

Integrators weights:

- Front-end integ, 0.66pF: 27\( \mu \)m x 27\( \mu \)m
- Remaining ints, 0.45pF: 22\( \mu \)m x 22\( \mu \)m

- Also MiM caps in OPA, in the SC CMFB nets, and in the anti-aliasing filter
Resistive-ladder DAC
- 700-Ω ladder between references +2V/+0.5V (14x50Ω, 3.21mW)
- Unsalicided n+ poly used in resistors
- References obtained from the on-chip analog supply

Flash ADC
- Static input scheme (no caps)
  - Reduces capacitive load to 4th integrator
  - Saves silicon area
- Extra differential pair in comparators

Comparator
- Pre-amp + Regenerative latch + SR latch (Different supplies)

<table>
<thead>
<tr>
<th>Hysteresis</th>
<th>Offset</th>
<th>Power consumption</th>
</tr>
</thead>
<tbody>
<tr>
<td>127.5μV</td>
<td>6.3mV</td>
<td></td>
</tr>
</tbody>
</table>

3-bit Quantizer

<table>
<thead>
<tr>
<th>Input capacitance</th>
<th>Resolution time, LH</th>
<th>Resolution time, HL</th>
</tr>
</thead>
<tbody>
<tr>
<td>100F</td>
<td>3.9ns</td>
<td>2.8ns</td>
</tr>
</tbody>
</table>

DT-ΣΔMs: Case Study

Layout & Prototyping

CMOS 0.25μm
- 2.78mm² w/o pads
- 44-pin plastic QFP

- Dedicated analog, mixed, and digital supplies
- Guard rings with dedicated pad/pin
- Increased distance among analog and digital blocks
- Layout symmetry and common-centroid techniques
- Shielded bus for distributing the clock signals
- Extensive on-chip decoupling
- Pad ring divided blocking cells
- Multiple bonding techniques

4-layer PCB
### DT-$\Sigma \Delta$Ms: Case Study

**Experimental results**

- SFDR = 90dB
- THD = -87dB

**ST20184**

ST20190 Utopia ADSL2+ solution for CPE

Part of a commercial modem

In mass production (STMicroelectronics)

### CT-$\Sigma \Delta$Ms: Overview of CT-$\Sigma \Delta$M Non-Idealities

**CT-$\Sigma \Delta$M Non-Idealities**

- Building-block Errors
  - Opamp finite (non-linear) DC gain
  - Integrator transient response
  - Element tolerances
  - Time-constant error
  - Non-linearity (Front-end V-I and DAC)
  - Noise

- Architectural Timing Errors
  - Quantizer metastability
  - Excess loop delay
  - Clock jitter
### CT-ΣΔMs: Basic building blocks

- **Active-RC**
  \[ H(s) = \frac{1}{s\tau} \]

- **MOSFET-C**
  \[ \tau = R_{ch}C \]

- **Gm-C**
  \[ \tau = \frac{C}{g_m} \]

- **Gm-MC**
  \[ \tau = \frac{C}{g_m} \]

- **A Gm-MC implementation**
  - 2nd-order single-loop ΣΔM
  - 1-bit switched-current DAC
  - 1-bit (latch) comparator

### CT-ΣΔMs: Non-ideal Integrator Transfer Function

- **Integrator Transfer Function (ITF) degraded by circuit non-idealities**

\[ Y(s) = \frac{1}{\tau s} X(s) \]

**Ideal Transfer Characteristics**

\[ Y(s) = \left[ \frac{1}{\tau_i} \cdot \frac{1}{s} \cdot \frac{T_{in}(s)}{} \right] X(s) \]

**First-Order Actual Transfer Characteristics**

\[ T_{in}(s) = \frac{s}{s + \omega_{pl}} \]

\[ T_{ln}(s) = \frac{s}{(s + \omega_{pl})(s + \omega_{ph})} \]

\[ T_{lp}(s) = \frac{s}{(s + \omega_{lp})(s + \omega_{ph})} \]

**First-Order Non-ideal Integrator Behaviours:**

- Deviations in the Unity Gain Frequency $\omega_u$
- Low-Frequency Pole $\omega_{pl}$ Due to Losses
- Produce Finite DC Gain
- Magnitude Errors for $\omega \approx \omega_{pl}$
- Phase Errors for $\omega \approx \omega_{pl}$
- High-Frequency Poles and Zeros $T_{lp}(s)$
- Phase Errors for $\omega \approx \omega_{pl}$, $\omega_{ph}$
CT-ΣΔMs: Effect of finite DC gain error

Opamp finite DC gain (I)

RC integrators [Gerf03]

\[
\text{ITF}(s) = \frac{\alpha}{s + \gamma} \quad \alpha = \frac{A_0}{1 + A_0} \quad \gamma = \frac{1}{\tau} \cdot \frac{1}{1 + A_0}
\]

- Same IBN degradation as in SC ΣΔMs \( \tau = 1/f_s \)

\[
P_A = \frac{\Delta^2}{12 kT C} \left[ \frac{1}{A_0^2} \sum_{m=1}^{L} \frac{\pi^2}{(2m+1)^2} \frac{(L-m-1)!}{A_0^{2L-2m-4} (L-m)^m} \right]
\]

Opamp finite DC gain (II) – Gm-C integrators

Power Spectral Density of an \( L \)th-order \( \Sigma\Delta \)M

\[
S_q(f) = \sqrt{\sum_{i=0}^{L-1} \left( \frac{f_{\text{in}}}{\omega_{\text{pl}}} \right)^i} \frac{\Delta^2}{12 \cdot A_{\text{dc}}^2} f_s
\]

Relative increase of \( P_Q \) in a 2nd-order \( \Sigma\Delta \)M

\[
\frac{P_Q}{P_Q_{\text{dc}} \rightarrow \infty} = \frac{5}{\pi} \left( \frac{M}{A_{\text{dc}}} \right)^4 + \frac{10}{3\pi} \left( \frac{M}{A_{\text{dc}}} \right)^2 + 1
\]
Integrator transient response (I)

- Less critical than in DT ΣΔMs
- Need to be taken into account, specially in broadband applications

Influence of GBW [Gerf03]

\[ P_{GBW} = \frac{L^2}{12k_i^2k_q^2} \left[ \frac{\pi}{2L+1} \right]^{2L-1} \left( \frac{k_i}{GBW_i} \right)^L \prod_{i=2}^{L} \left( 1 + \frac{1}{GBW_i} \right)^2 \]

GBW - \( A_0 \cdot \omega_g \) \[ \text{ITF}(s) = \frac{GBW}{s(GBW+k_i/\tau)} \]

Other dynamic effects

- 2nd-order poles
- Slew-rate

Model of GBW for RC-active based CT-ΣΔMs [Ortm04]

- Modeled as a gain error (GE) and extra loop delay
- Each delay is different for each feedback path

\[ T_{D1st} = \frac{1 - e^{-\omega_2/\omega}}{\omega} \quad T_{D2nd} = \frac{\omega_1^2(1 - e^{-\omega_2/\omega_2}) - \omega_2^2(1 - e^{-\omega_1/\omega_1})}{\omega_1\omega_2(\omega_1 - \omega_2)} \]
**CT-ΣΔMs: Circuit element tolerances**

- **Element tolerances**
  - Scaling coefficients accuracy limited by random errors in resistors/capacitors
    \[
    \frac{\Delta r}{r} - \frac{\Delta C}{C} - \frac{\Delta g_m}{g_m} = \sigma_r - \sqrt{\sigma_C^2 + \sigma_{g_m}^2}
    \]
  - Especially critical in:
    - High-order single-loop architectures (instability)
    - Cascade architectures (analog/digital coefficient ratios)
  - Two types of random errors:
    - Absolute tolerances: variations from chip to chip (10-20%)
    - Relative mismatches: variations from device to device on one chip (0.5-1%)

- **Electrical control of frequency tuning**

- **System-level optimization and synthesis method**

---

**CT-ΣΔMs: Circuit element tolerances**

- **Direct synthesis method of CT cascade architectures [Tort06]:**
  - Optimum placement of poles/zeros of the NTF
  - Synthesis of both analog and digital part of the cascade CT ΣΔ Modulator
  - Reduced number of analog components
  - Reduced sensitivity to element tolerances

---

**DT-to-CT Method**

**Direct Method**
Direct synthesis of cascade architectures (I) [Tort06]

- Sensitivity to mismatch (gm,C)
- A 2-1-1 example

Direct synthesis of cascade architectures (II) [Tort06]
**CT-ΣΔMs: Circuit element tolerances**

- Synthesized cascaded CT ΣΔMs to cope with 12-bit@20-MHz

**CT-ΣΔMs: Synthesis Methods**

- A case study: A 12-bit@20MHz, 4-b, 2-1-1 CT ΣΔM (RC/Gm Integrators)

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>R_m, R_h</td>
<td>1kΩ</td>
</tr>
<tr>
<td>R_v</td>
<td>2.9kΩ</td>
</tr>
<tr>
<td>k_p1, k_p2</td>
<td>50µA/V</td>
</tr>
<tr>
<td>k_p3</td>
<td>500µA/V</td>
</tr>
<tr>
<td>k_p4</td>
<td>120µA/V</td>
</tr>
<tr>
<td>k_m2, k_m3, k_m4</td>
<td>450µA/V</td>
</tr>
<tr>
<td>C_1</td>
<td>7.5pF</td>
</tr>
<tr>
<td>C_2, C_3</td>
<td>1.075pF</td>
</tr>
</tbody>
</table>

![Frequency response graph]
CT-ΣΔMs: Integrator time-constant error

Integrator time-constant error (I)

\[ \text{ITF}(s) = \frac{A_0}{1 + sC(1 + \varepsilon_T)/G_0} \]
\[ \varepsilon_T = C_D/C \]

- Capacitor plate parasitic capacitances
- Parasitic capacitances of the interconnection lines
- Parasitic input capacitances of the circuits connected to the node
- Parasitic output capacitances of the circuits connected to the node

<table>
<thead>
<tr>
<th>RC ( \varepsilon_T )</th>
<th>MOSFET-C ( \varepsilon_T )</th>
<th>Gm-C ( \varepsilon_T )</th>
<th>Gm-MC ( \varepsilon_T )</th>
</tr>
</thead>
<tbody>
<tr>
<td>[ 1 + \frac{G}{C \cdot A_0 \cdot \omega_a} + \frac{C + C_T}{C \cdot A_0} ]</td>
<td>[ 1 + \frac{G_m}{C \cdot A_0 \cdot \omega_a} + \frac{C + C_T}{C \cdot A_0} ]</td>
<td>[ 1 + \frac{C_T}{C} ]</td>
<td>[ 1 + \frac{G_m}{C \cdot A_0 \cdot \omega_a} + \frac{C + C_T}{C \cdot A_0} ]</td>
</tr>
</tbody>
</table>

Optimum SNR for:

\[ \tau = 1/f_s \]

\[ \Delta P_{\text{SNR}} \equiv \frac{1}{A_0^2} + \frac{1}{(1 + \varepsilon_T)^2} \] (1st-order modulator)
\[ \frac{2}{3\pi^2} + \frac{10}{3\pi^2} \cdot \frac{(1 + \varepsilon_T)^2}{A_0^2} - M^2 + \frac{\varepsilon}{\pi A_0^4} M^4 \] (2nd-order modulator)
CT-ΣΔMs: Non-linear errors

- Non-linearity (I): Causes
  - Intrinsic non-linearity of the resistor material
  - Modulation of thickness of the conductive layer with resistor voltage

- V-I transformation in RC integrators

  - Ideally
    \[ i = R_0^{-1} \cdot v \]
    \[ g_{NL}(v) = R_0^{-1} \cdot \left[ a_2 \cdot v^2 + a_3 \cdot v^3 + o(v) \right] \]

- V-I transformation in Gm-C integrators

  - Normalized Large Signal Characteristic
    \[
    i(v) = \begin{cases} 
    -1 & v \leq -\sqrt{2} \\
    \frac{1}{2} v - \frac{1}{2} (v/2)^2 & |v| < \sqrt{2} \\
    1 & v \geq \sqrt{2} 
    \end{cases}
    \]
    \[ THD = HD_3 = \frac{g_m}{g_m} \frac{V_i^3}{V_i} \]

- Non-linearity (II): Effect on Gm-C CT-ΣΔMs [Bree01]

  - Linearization strategies

Source Degeneration of Basic Differential Pairs

Exploiting the Ohmic Region of MOSTs

MOST Saturated Transconductors
- Functional cancellation
- Squares-law functions combination

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CT-ΣΔMs: Non-linear errors

- Non-linearity (III) – Commonplace architecture
  - RC-active front-end integrator
  - Gm-C subsequent integrators

- Other sources of non-linearity
  - Multi-bit DACs
  - Linearity must be the same or lower than the required resolution
  - Corrected by same techniques as those employed in SC ΣΔMs
    - DEM
    - Calibration

- Circuit noise
  - Dominated by noise sources from the front-end integrator and DAC
  - Flicker noise reduced by proper sizing and/or chopper techniques
  - Unsampled noise – effect of sampling reduced by the loop gain

$$P_{Th} = \frac{kT}{4C(2L+1)} \frac{\pi^2}{2L+1}$$

CT-ΣΔMs: Comparator metastability

- Comparator metastability
  - Can be cancelled by using additional latches [Dagh04]
  - Modeled as a jitter noise [Cher00]
CT-ΣΔMs: Excess loop delay

Excess loop delay (I)

- Adds additional poles to STF/NTF
- Causes instability
- Stability condition:
  - 2nd-order \( \rho_d \leq \frac{g_2}{2g_1g_2} \)
  - Lth-order \( \rho_d \approx |H(f)|_{outband} \)

Excess loop delay (II) – an example of instability

 DAC transient response delay

\[ Y(f) = \frac{g_0g_1g_2}{(sT)^2 + g_0g_1g_2} X(f) \]

\[ X(f) = \frac{(sT)^2}{(sT)^2 + g_1g_2} E(f) \]
Excess loop delay (III) – cancellation techniques

- Extra feedback paths (DACs) with tunable gains [Cher00]
- Additional DAC and two latches [Yan04]

Excess loop delay (IV) – Digital compensation [Font05]

- Implemented in a 3rd-order single loop architecture with 5-level quantizer
  - 90nm CMOS
  - 74-dB SNDR-peak, 600kHz bandwidth
  - 6.0mW, 1.5V
- Excess loop delay compensated in the digital domain
- Half-a-clock-cycle delay
  - Relax comparators speed
  - Provide maximum isolation between quantizer and DAC switch events
Clock jitter (I)

- S/H
  - Shaped by the modulator NTF
  - Can be neglected
- DAC
  - Directly adds with the input
  - Increases the in-band noise power

Clock jitter (II) – White noise model approximation (NRZ/DAC) [Cher00][Zwan96]

- Standard deviation of jitter error: \( \sigma_j^2 = \sigma_{DAC}^2 \)
- SNR degradation:
  \[
  SNR_j = 10 \log \left( \frac{1}{16MB^2\sigma_j^2} \right)
  \]
  \[
  \frac{\sigma_j^{CT}}{\sigma_j^{DT}} = \left( \frac{\pi}{2M} \right)^2
  \]

CT-ΣΔMs are more sensitive to clock jitter than DT ΣΔMs

White noise model approximation (NRZ DAC) [Cher00][Zwan96]

CT-ΣΔMs: Clock jitter error
Clock Jitter (III) – lingering effect [Olia03a]

- Jitter-induced noise includes both white and shaped components
- State-space analysis of CT-ΣΔMs with RZ DAC shows that:

\[ S_e(x) = \frac{\sigma_e^2}{2} \left( \sum_{m_1=1}^{M_1} \sum_{j_1=1}^{N} \sum_{m_2=1}^{M} \sum_{j_2=1}^{N} a_{m_1 m_2} x_{j_1 j_2} \right) \]

Clock Jitter (IV) – Multi-bit NRZ DACs [Tort05]

- Commonly used in CT-ΣΔMs for broadband telecom applications
- Less sensitive to clock jitter

\[ \Delta Q(n) = \Delta I_{DAC} (n) \cdot \Delta T(n) \]

- Using state-space formulation of NTF:

\[ P_e = \frac{\sigma_e^2}{T_s^2} \left( \frac{T_s^2 \sigma_m^2}{2} + \frac{\lambda_{FS}^2}{6(2^M - 1)} \right) \cdot \psi(\bar{g}, \bar{p}, \bar{L}, L) \]

\[ \psi(\bar{g}, \bar{p}, \bar{L}, L) = 1 - \frac{\bar{g} \cdot \bar{p}}{2} \sum_{k=1}^{L} \sum_{l=1}^{L} g_k g_l \frac{\lambda_k^{-1} - \lambda_l^{-1}}{1 - \lambda_k^{-1} \lambda_l^{-1}} \]

\[ SNR_{\text{Jitter}} = \frac{A^2}{2 \cdot P_{\text{band}}} - \frac{2 \cdot B}{3(2^M - 1)} \left[ \frac{A^2 \omega_n^2}{f_s} + \frac{\lambda_{FS}}{f_s} \psi(\bar{g}, \bar{p}, \bar{L}, L) \right] \]
CT-ΣΔMs: Clock Jitter error

Clock Jitter (V): Comparison of [Tort05] with previous approaches

Assuming that $SNR_{jitter}$ is dominated by the signal-dependent term:

$$SNR_{MAX} = 10 \log \left( \frac{M}{4\pi^2 \sigma^2 \Delta T^2 B_w^2} \right)$$  
[Boser, JSSC, 1988]

If the modulator-dependent term dominates (single-bit quantization):

$$SNR_{jitter} = 10 \log \left( \frac{1}{16M\sigma^2 \Delta T B_w^2} \right)$$  
[Van der Zwan, JSSC, 1996]

Clock Jitter (VI) – Multi-bit NRZ DACs [Tort05]

Two cases:
- CTΣΔM1: $B=2$bit, $f_s=400\text{MHz}$
- CTΣΔM2: $B=5$bit, $f_s=160\text{MHz}$

CTΣΔM1

CTΣΔM2

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Clock Jitter (VII) – Compensation techniques

- Multi-bit quantization (non-linear DAC)
- Switched-capacitor DAC [Veld03]
  - Voltage-mode operation (proper for active RC integrators)
  - Slower than switched-current (current steering) DAC
- FIRDAC to generate a multilevel signal [Putt04]

Clock jitter error

130nm mixed-signal CMOS, 1P8M
Cascade 3-2 multi-bit (4b) CT ΣΔM
Gm-C loop-filter implementation
Current-steering feedback DACs + DEM
12-bit effective resolution
40MS/s output rate (20MHz bandwidth)
240MHz clock frequency
1.2V ± 10% analog/digital power supply
On-chip tuning of analog components
Estimated power consumption is 45mW

Loop-filter coefficients

<table>
<thead>
<tr>
<th>Coefficient</th>
<th>Expression</th>
</tr>
</thead>
<tbody>
<tr>
<td>$C_0$</td>
<td>3.65 pF, $k_C = 100$ μA/V</td>
</tr>
<tr>
<td>$C_1$, $C_2$, $C_3$, $C_4$, $C_5$, $C_6$, $C_7$, $C_8$</td>
<td>2C_u</td>
</tr>
<tr>
<td>$k_{i1}$</td>
<td>852 μA/V, $k_{i2} = 730$ μA/V</td>
</tr>
<tr>
<td>$k_{p0}$ = 2$k_u$, $k_{p1}$ = 4$k_u$, $k_{p2}$ = 2$k_u$, $k_{p3}$ = 5$k_u$</td>
<td></td>
</tr>
<tr>
<td>$k_{x1}$ = $k_{x2}$ = $k_{x3}$ = $k_{x4}$ = $k_{x5}$ = 7$k_u$</td>
<td></td>
</tr>
<tr>
<td>$k_{x6}$ = 5$k_u$, $k_{x7}$ = 6$k_u$</td>
<td></td>
</tr>
<tr>
<td>$k_{x8}$ = $k_{x9}$</td>
<td></td>
</tr>
</tbody>
</table>

Finite output impedance | 12MO
Settling Time | 500ps
CT-ΣΔMs: Case Study

Transistors
- Resistive source degenerated front-end transconductor
- Loop-filter transconductors based on quadratic term cancellation

Transistor-level performance

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>DC Gain</td>
<td>78.3 dB</td>
</tr>
<tr>
<td>Diff. Input Amplitude</td>
<td>0.3 V</td>
</tr>
<tr>
<td>Diff. Output Amplitude</td>
<td>0.3 V</td>
</tr>
<tr>
<td>HD3</td>
<td>-80 dB</td>
</tr>
<tr>
<td>Power consumption</td>
<td>8.3 mW</td>
</tr>
</tbody>
</table>

Current-steering DACs
- 2 360-μA P-type gain-boosted current sources
- 15 N-type regulated-cascode current cells

Current-steering DAC: Worst-Case Transistor-level performance

<table>
<thead>
<tr>
<th>Parameter</th>
<th>P-type cell</th>
<th>N-type cell</th>
</tr>
</thead>
<tbody>
<tr>
<td>Output Impedance</td>
<td>2MΩ</td>
<td>12MΩ</td>
</tr>
<tr>
<td>Unitary current</td>
<td>380μA</td>
<td>40μA</td>
</tr>
<tr>
<td>Current S/H Deviation</td>
<td>0.57%LSB</td>
<td>410ps</td>
</tr>
<tr>
<td>Setting Time</td>
<td>--</td>
<td>410ps</td>
</tr>
<tr>
<td>Power Cons. (μW)</td>
<td>0.48μW</td>
<td>0.1μW</td>
</tr>
</tbody>
</table>
Chip implementation

Front-End Transconductors
DAC1s
Clock latchs & DEM
Quantizers
M-i-M Capacitors
Transimpedance
Transconductors
Loop-Filter
DAC2s
Clock
Latches
& DEM
Quantizers

Transistor-level simulation results

SNDR = 75.3 dB (12.2 bits) @ 20-MHz bandwidth
Low-resistive bulk

- The deep-substrate is a low-impedance path for injected disturbances.
- Traditional layout techniques (guard rings, separation of blocks) have a limited effectiveness.

**Most Standard CMOS technologies**

Epitaxial process with heavily-doped bulk

Impact of the on-chip switching activity

- Lightly-doped low-conductive / high-resistive $p-$substrate
- Heavily-doped high-conductive / low-resistive $p^+$substrate

Dedicated analog and digital supplies:
- Analog core
- Digital core
- Digital output buffers

Open pad ring
- Common-centroid layout techniques
- Guard rings
- Increased distance among analog and digital blocks
- Dedicated analog, mixed, and digital supplies
- Guard rings with dedicated pad/pin
- Increased distance among analog and digital blocks
- Layout symmetry and common-centroid techniques
- Shielded bus for distributing the clock signals
- Extensive on-chip decoupling
- Pad ring divided blocking cells
- Multiple bonding techniques

Example: A $\Sigma\Delta$M in 0.25$\mu$m for ADSL/ADSL+

- CMOS 0.25$\mu$m
  - 2.78mm$^2$ w/o pads
  - 44-pin plastic QFP

The chip also includes other blocks pertaining to the final application:

- PLL (2x, 4x)
- Decimation filter (↓8, ↓16, ↓32)

Test Set-Up:

- $\Sigma\Delta$M
- PLL + $\Sigma\Delta$M + Filter

- Dedicated analog, mixed, and digital supplies
- Guard rings with dedicated pad/pin
- Increased distance among analog and digital blocks
- Layout symmetry and common-centroid techniques
- Shielded bus for distributing the clock signals
- Extensive on-chip decoupling
- Pad ring divided blocking cells
- Multiple bonding techniques
Double-bonding and multiple pins for supplies

Different pin assignment for analog, mixed and digital

- Novel tech (characterization not yet confirmed by silicon results)
- Two-layer PCB
  - Soldered samples (in order to avoid socket parasitics)
  - Anti-aliasing filter (passive, 1st order)
  - Independent control of amplifier bias currents
  - Decoupling
  - Impedance termination

Test Set-Up

- Workstation
  - Cancellation logic
  - 64k-sample FFT
- Digital test unit
- Low-distortion signal generator
- PCB
- Bit streams
- Clock supply, reference
DT-$\Sigma$Ms: References


References


