Supplemental Material: Doubling the mobility of InAs/InGaAs selective area grown nanowires

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S1. Substrate fabrication and growth details

As a template for SAG of InAs nanowires, [1-10]- and [100]-oriented growth windows are formed on semi-insulating GaAs(001) substrates covered with a 10-nm thin silicon dioxide

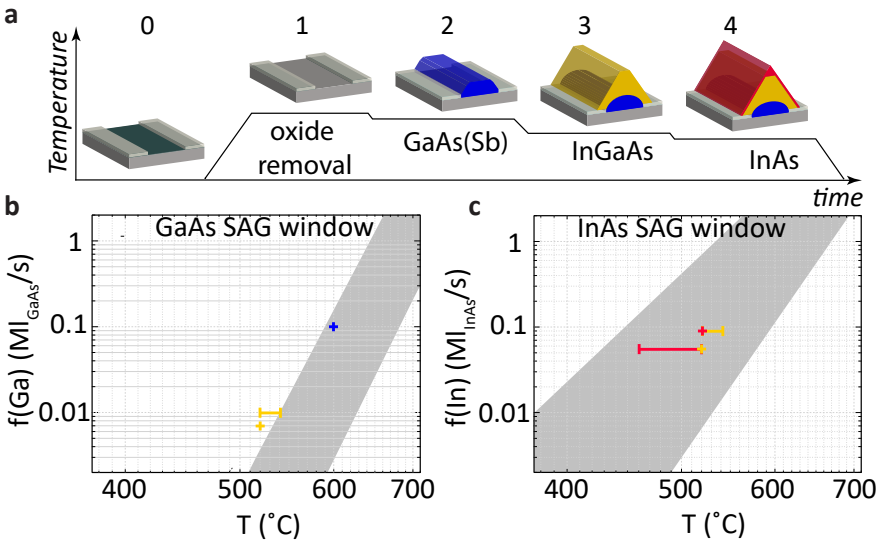

Figure 1: InAs/InGaAs/GaAs(Sb) SAG nanowires on GaAs(001) substrates. (a) Schematics of four growth steps as a function of temperature T used in this work: 1. native oxide removal, 2. GaAs(Sb), 3. InGaAs and 4. InAs layer growth. Selectivity windows for GaAs (b) and InAs (c) on GaAs(001) adapted from.[1] We mark growth conditions studied in the current work for the 2-4 growth steps using the same colors as in (a).

(SiO_2) layer (Fig. 1a). We use plasma enhanced chemical vapor deposition (PECVD) for oxide deposition and an electron beam lithography process for the patterning of growth windows. Different sizes of growth windows are exploited during this study. We use inductively coupled plasma with a mixture of tetrafluoromethane (CF4) and hydrogen (H2) gases to reveal the pattern. One of the advantages of the plasma etching as compa to the wet etching is insignificant surface roughness after the processing. The root-mean-square (rms) roughness of the GaAs surface at the bottom of the trenches increases insignificantly from 0.24±0.2 nm before the process to 0.31±0.11 nm after the plasma etching.

The aim of SAG is to restrict the deposition of material on the mask surface and to maintain the growth only within the mask openings (i.e. on the substrate). Growth parameters such as temperature and material fluxes are the key elements to control the selectivity. We grow GaAs(Sb) nanowires at 600 °C and 0.1 MLs^{-1} growth rate (equivalent to planar GaAs in monolayers per second, MLs^{-1}) to be within the selectivity window established earlier by Aseev et al.[1] (blue marker, Fig. 1b). For the ternary InGaAs buffer layer, we examine only

a narrow range of temperatures from 520 °C to 540 °C (yellow bar, Fig. 1b,c) as InAs and GaAs compounds have sufficiently different selectivity windows whose overlap is very narrow. We use 0.09 MLs^{-1} and 0.01 MLs^{-1} growth rates for InAs and GaAs, respectively. For the second set of samples, we fix the InGaAs buffer growth temperature to 520 °C (yellow marker, 1b,c) and the growth rates to 0.054 MLs^{-1} for InAs and 0.006 MLs^{-1} for GaAs. We study a 460-524 °C temperature range for the InAs layer (red bar, Fig. 1c).

S2. Degradation of surface topography after thermal oxide removal prior nanowire growth

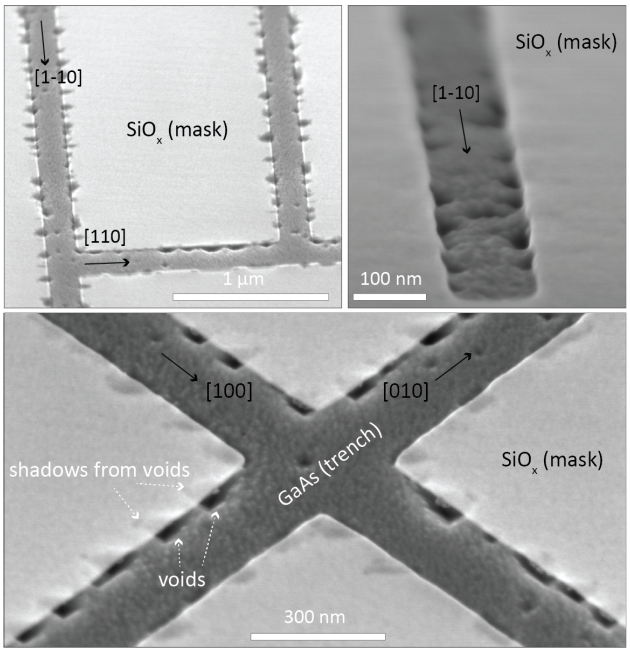

Figure 2: Degradation of the surface topography after native oxide removal from the bottom of GaAs growth windows via thermal annealing in MBE under As flux. SEM images (70° tilt) highlighting voids generally found at the periphery of trecnhes and their shadows visible through 10 nm thick SiO_2 mask. growth windows of different high-symmetry crystallographic orientations are shown, all having voids.

By implementing conventional thermal annealing of the native oxide at 620 °C for 2 min under a constant supply of 1.5×10^{-5} mbar As flux, we observed surface pits formed at the bottom of [110] and [1-10] oriented trenches with a density of 94±15 pits μm^{-2} and 140±20 pits μm^{-2}, respectively (Fig. 2). In general, these are formed at the periphery of the growth

windows and are often as deep as 30 nm. The pits continue underneath the oxide layer, forming pockets on the walls of the trench.

We find similar results for samples where As flux is increased to 3.0×10^{-5} mbar with otherwise identical annealing protocol. We measured density of 105±16 pits μm^{-2} for [110] and 110±17 pits μm^{-2} for [1-10] oriented trenches. The density is comparable to the one observed on planar GaAs(100) wafers after thermal annealing of the native oxide.[2] Our findings confirm that the GaAs surface degradation happens during thermal annealing of the native oxide independently on the As flux and the existence of the oxide mask.

As an alternative way of oxide removal, we used an atomic hydrogen treatment. The latter was performed at a substrate temperature of 350 °C in the MBE buffer chamber. The atomic hydrogen is produced by cracking molecular hydrogen with a tungsten filament heated to about 1600 °C.

The native oxide removal involving a-H proceeds via decomposition of the stable Ga_2O_3 into volatile Ga_2O:[3] $Ga_2O_3 + 4\,H \longrightarrow Ga_2O\uparrow + 2\,H_2O\uparrow$, and decomposition of arsenic oxides:[4] $12\,H + As_2O_3 \longrightarrow 3\,H_2O\uparrow + 2\,AsH_3\uparrow$. A survey of literature on surface hydrogenetaion shows that it reduces surface states and near-surface lattice defects improving electronic properties of GaAs-based devices.[4–6]

S3. Faceting of GaAs(Sb) vs GaAs nanowires

We use AFM to probe the topography across nanowires. The tip used has a nominal diameter of 4 nm and a 65-75° angle formed with respect to the flat (001) top facet of the nanowires, what allows us to measure angles of the facets with high accuracy.

Table 1: Angles derived by fitting a line to the side facets of GaAs(Sb) and GaAs nanowires and extracting its slope. Estimated side facets: {113} and {112} for the GaAs(Sb) nanowires and {113} and {111} for the GaAs nanowires.

Angle	(113)	(112)	(111)
(001)	23.29°	38.11°	51.10°
fitting error	0.63°	1.08°	1.05
STDEV	1.05°	3.39°	0.47°

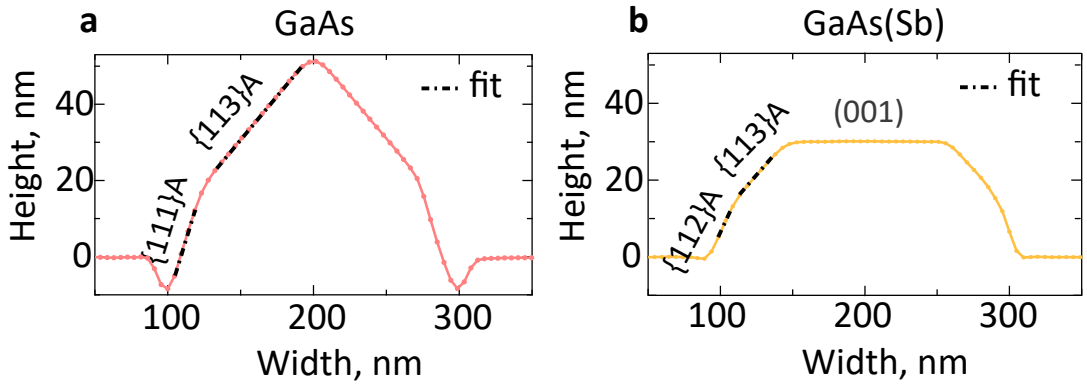

Figure 3: Faceting of GaAs (a) vs GaAs(Sb) (b) SAG nanowires grown in 220 nm wide [1-10]-oriented growth windows on GaAs(001). The growth parameters are identical between the samples, the only difference being Sb-surfactant added for sample (b). An example of a facet fitting is shown. GaAs(Sb) nanowires exhibit a flat top (001) facet which is not present for GaAs nanowires. The size of {113}A facets is greatly reduced for GaAs(Sb) nanowires as compared to GaAs. In addition, {111}A side facets for GaAs nanowires seem to change to {112}A facets for GaAs(Sb).

S4. The role of InGaAs growth temperature.

We grow six InAs/InGaAs/GaAs(Sb) samples at 520-540 °C (Fig. 4). In general, the morphology of nanowires does not change within the temperature range. On the contrary, the surface of the oxide mask evolves significantly: from being covered with parasitic bulk growth at 520 °C to mainly free of any crystals at the higher end of temperatures (above 530 °C) in agreement with Aseev et al.[1]

A typical [1-10]-oriented InAs/InGaAs/GaAs(Sb) nanowire along with its simulated atomic model is shown in Figure 5a,b.[7] Fig. 5c shows composition profiles of In (atomic percentage, relative to Ga) extracted along the (-1-11)A facet from EELS maps. Standard deviation as error bars are obtained by averaging over several composition profiles in the InAs channel.

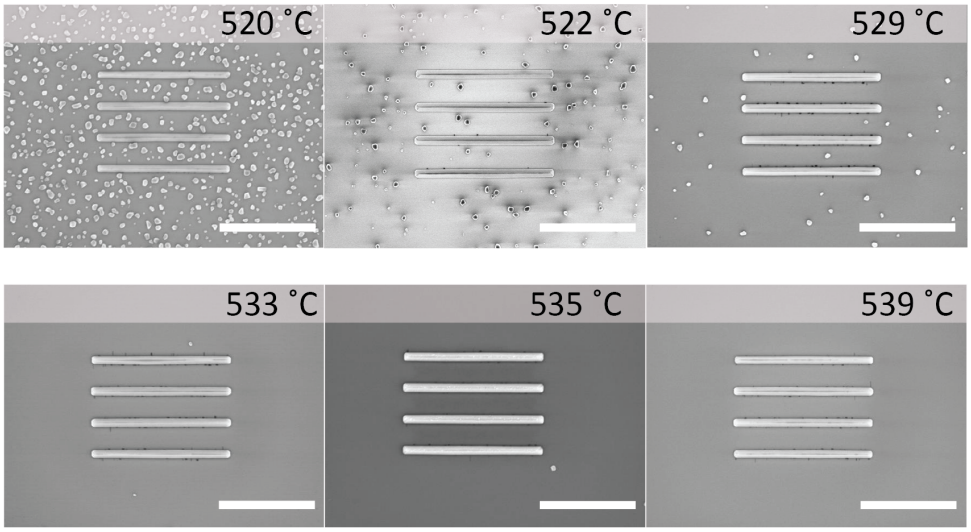

Figure 4: The role of InGaAs buffer growth temperature on the selectivity of InAs/InGaAs/GaAs(Sb) nanowires grown on GaAs(001) covered with a SiO_2 mask. SEM images (3 μm scale bar) highlighting evolution of the oxide mask with growth temperature for [1-10]-oriented nanowires. Note that some samples have been grown before we implemented the a-H procedure described above. That is why black stripes (voids underneath the mask) can be seen around nanowires.

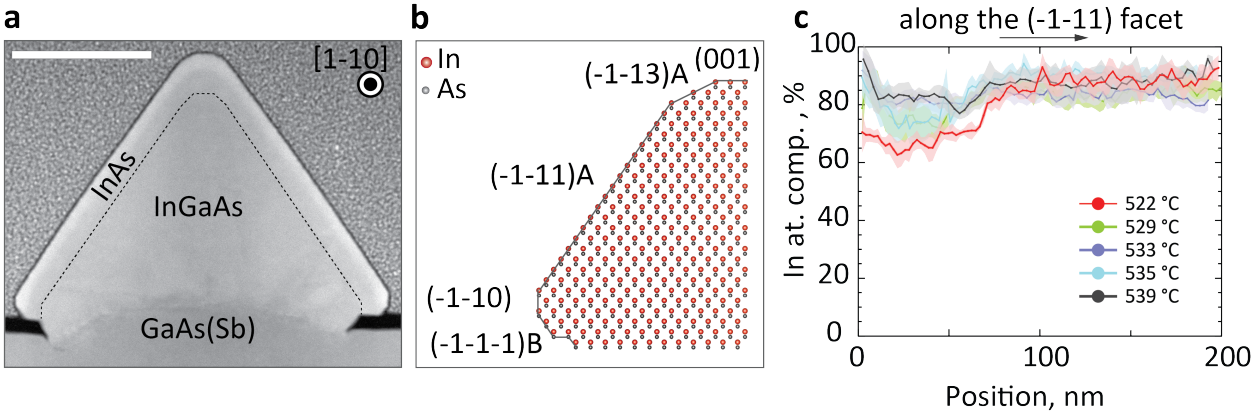

Figure 5: (a) Low magnification HAADF-STEM image (scale bar 100 nm) taken along the [1-10] viewing direction of a typical nanowire grown at 522 °C and (b) an atomic model representing the final faceting of the nanowire (only half is displayed thanks to the nanowire symmetry). (c) In compositional distribution (relative to Ga in atomic %, with standard deviation as error bars) extracted along the (-1-11)A facet in the InAs channel for samples grown at different InGaAs buffer growth temperatures.

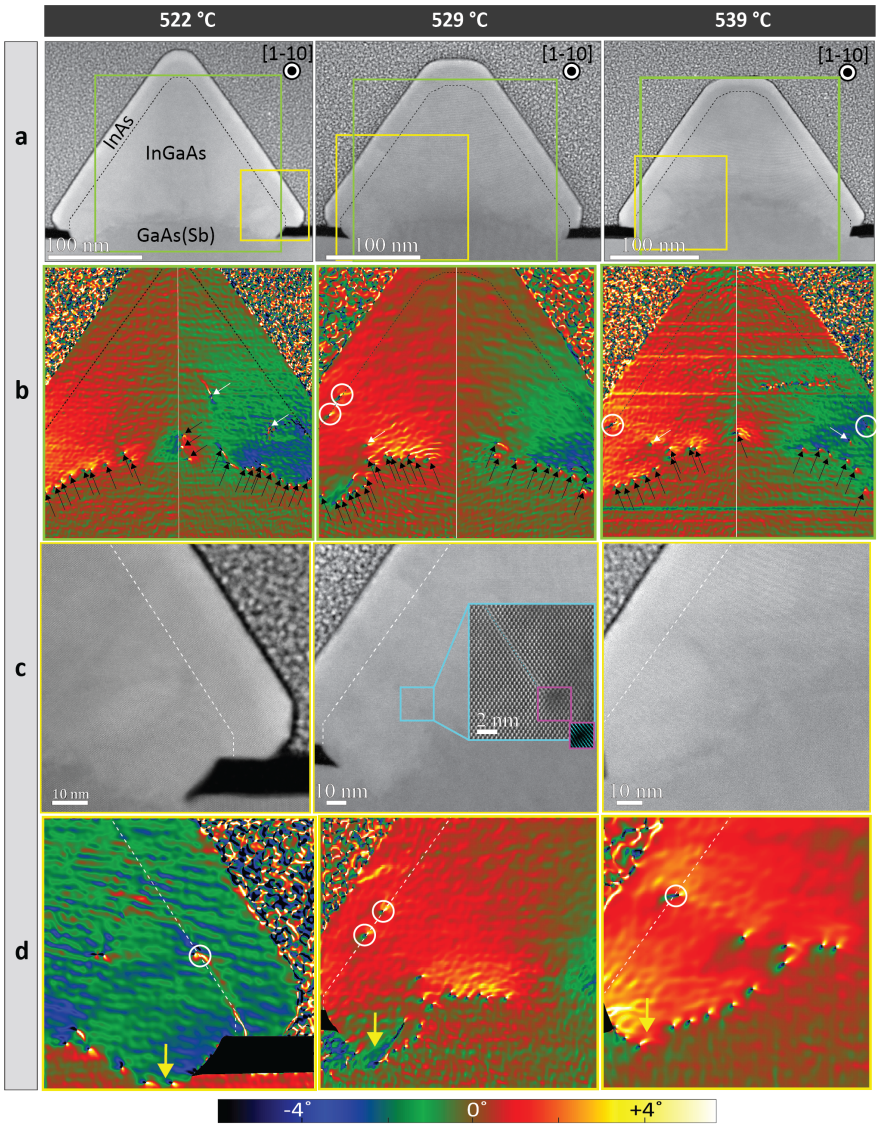

Figure 6: (a) Low magnification cross-sectional HAADF-STEM images of [1-10]-oriented InAs/InGaAs/GaAs(Sb) SAG nanowires grown at 522 °C (first column), 529 °C (second column) and 539 °C (third column) growth temperature of the InGaAs buffer layer. (b) GPA rotational maps of the central part of the nanowires from (a) (green box) highlighting misfit dislocations at the InGaAs/GaAs(Sb) buffers (black arrows), in the bulk of InGaAs (white arrows) and at the InAs/InGaAs interface (white circles). (c) HAADF-STEM images zoomed at the corners of nanowires from (a) (yellow box) and (d) their corresponding GPA rotational maps. The inset in (c) shows an example of a stacking fault which originates at the InGaAs/GaAs(Sb) interface in the vicinity of a misfit dislocation and propagates toward the InAs layer. The SiO_2 mask layer is marked in black in (d) to visualize the GaAs surface erosion as compared to the original substrate/mask interface.

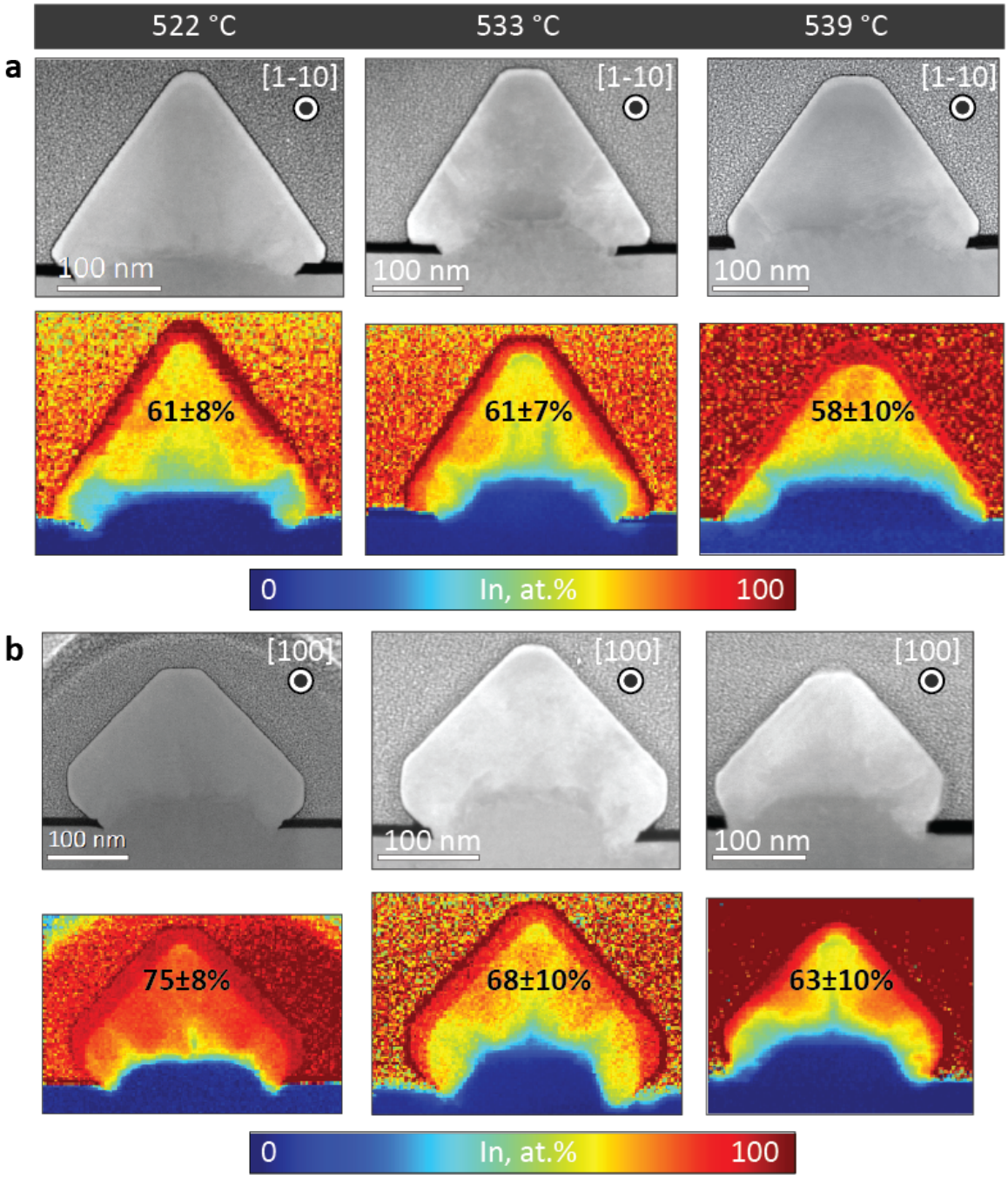

Figure 7: Low magnification HAADF-STEM images and corresponding chemical composition maps of [1-10]- (a) and [100]-oriented (b) InAs/InGaAs/GaAs(Sb) SAG nanowires grown at 522 °C (first column), 533 °C (second column) and 539 °C (third column) growth temperature of the InGaAs buffer layer. An average value of In atomic % in the InGaAs buffer layer for each nanowire is indicated as well.

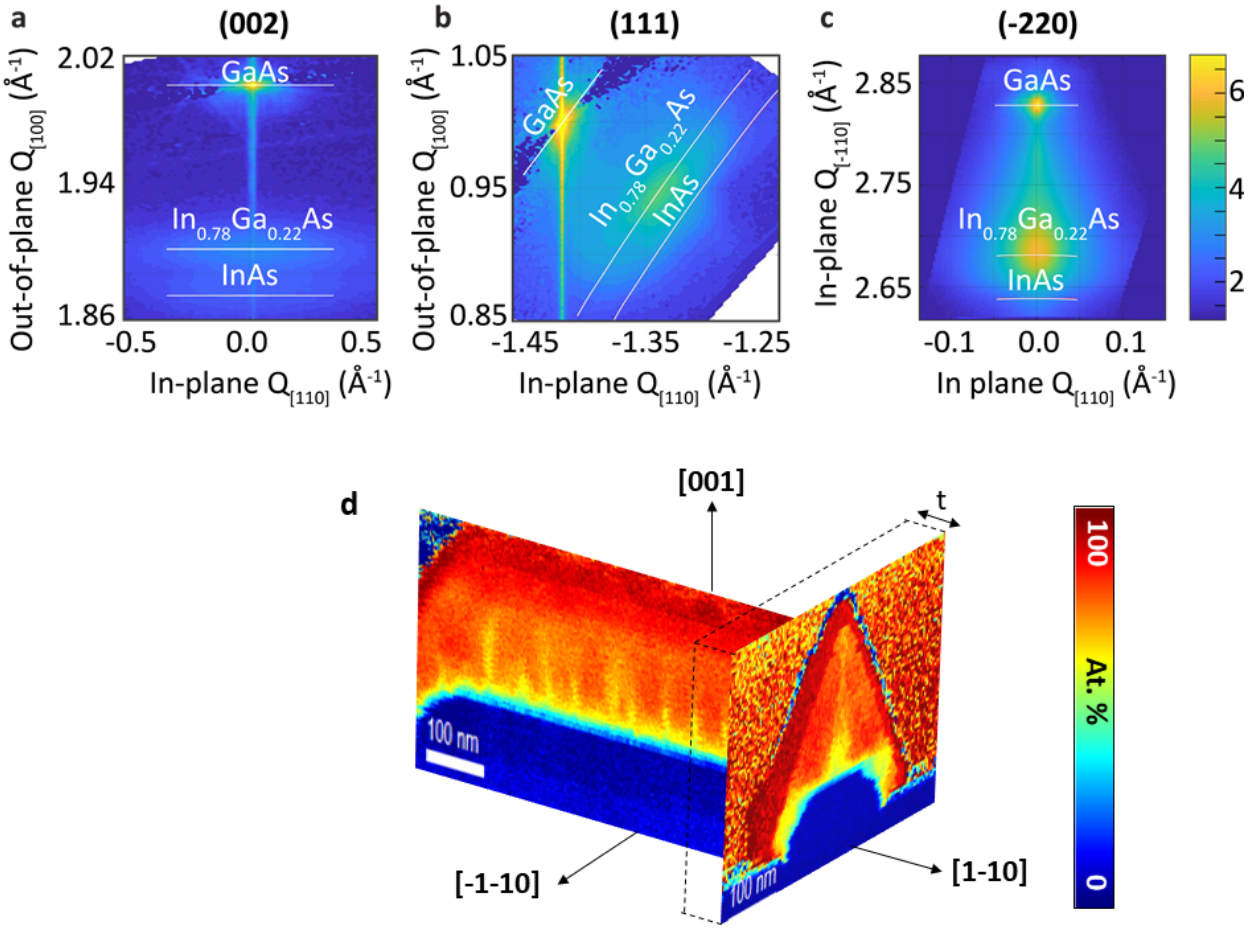

Figure 8: An example of typical XRD reciprocal space maps used to extract In composition x for [1-10]-oriented InAs/InGaAs/GaAs(Sb) SAG nanowires grown at 535 °C. Reciprocal maps around (002) (a), (111) (b) and (-220) (c) Bragg peaks. We highlight positions corresponding to pure GaAs, InAs and $In_xGa_{1-x}As$ with x=0.78. (d) Combined EELS chemical composition maps taken across and along a nanowire grown at 520 °C of the buffer (two identical nanowires are used). The thickness of a transversal lamella cut, t, is 50-100 nm only and thus represents a limited area of the buffer. Note also, that the InGaAs buffer layer has quasi-periodic Ga-rich flames along the nanowire. The position of the lamella cut through the length is the main factor controlling the average composition extracted with EELS.

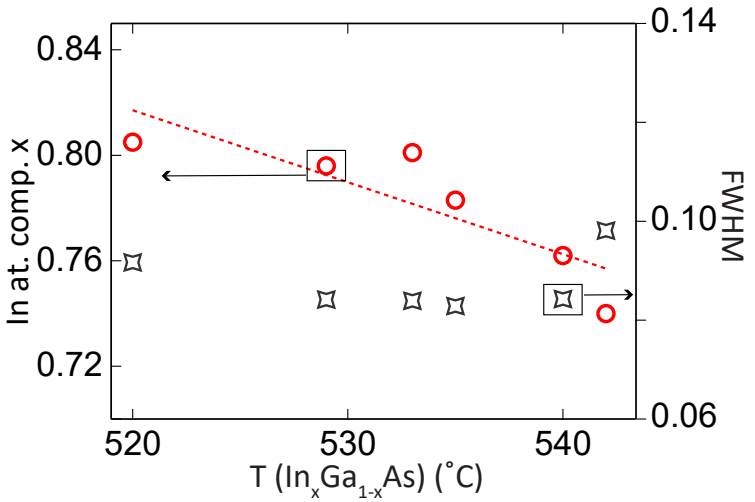

Figure 9: The role of InGaAs buffer growth temperature on the In composition x of [100]-oriented InAs/InGaAs/GaAs(Sb) SAG nanowires extracted from XRD. The peak broadening representative of the compositional variations in the buffer measured as full-width at half-maximum (FWHM) is plotted as well.

S5. The role of InAs growth temperature.

An SEM analysis reveals that the lowest temperature sample has a poor selectivity as compared to the other four samples (Fig. 10). This denotes that we are outside of the selectivity window at the chosen In flux and lower growth rates have to be considered instead.

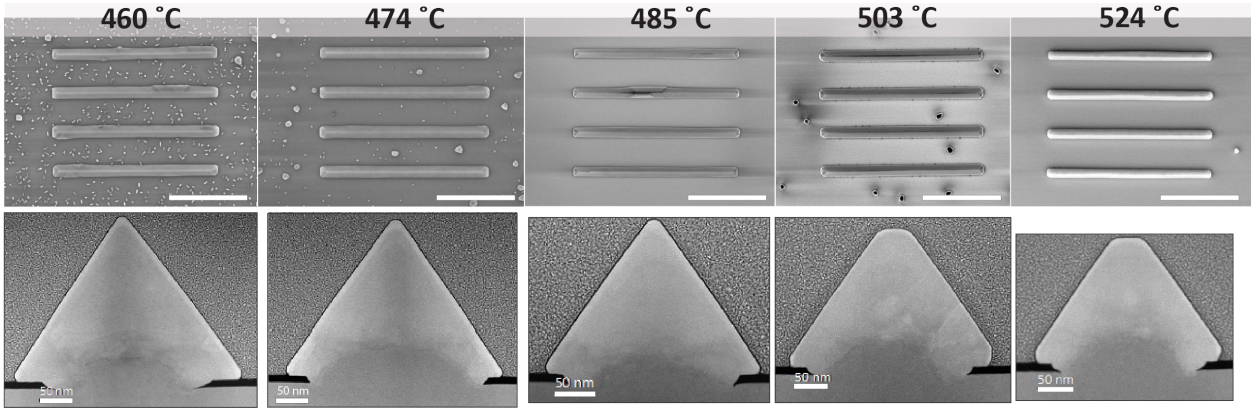

Figure 10: Upper raw: SEM images (2 μm scale bar) of [1-10]-oriented InAs/InGaAs/GaAs(Sb) nanowires grown at different InAs growth temperatures (highlighted above the images). Big crystals seen on the mask for all samples correspond to the InGaAs growth step (grown at 520 °C). Small crystals seen on the mask for low temperature samples correspond to the InAs growth step. Lower raw: low magnification cross-sectional HAADF-STEM images of the samples from the upper raw.

Table 2: List of growth parameters and number of observed misfit dislocations (MD) and stacking faults (SF) at the InAs/InGaAs interface (one nanowire per sample). (∗) InGaAs segment for this sample has been grown for a shorter time. This could explain the higher number of MD at the InAs/InGaAs interface.

Sample	A	B	C	D*	E
T_{InAs},°C	524	503	485	474	460
No. of MD	1	1	1	4-5	1
No. of SF	2	2	1	1	3

Figure 11 shows EELS maps used to extract In composition x across the InAs channel depending on the growth temperature. The growth temperature of the InGaAs buffer layer is fixed for all samples. We note that the sample grown at the lowest InAs growth temperature exhibits In-rich InGaAs buffer layer. The latter can explain why this sample has the smallest difference between the in-plane and out-of-plane component of the lattice constant

approaching the value of pure and relaxed InAs in Fig.4d of the main text.

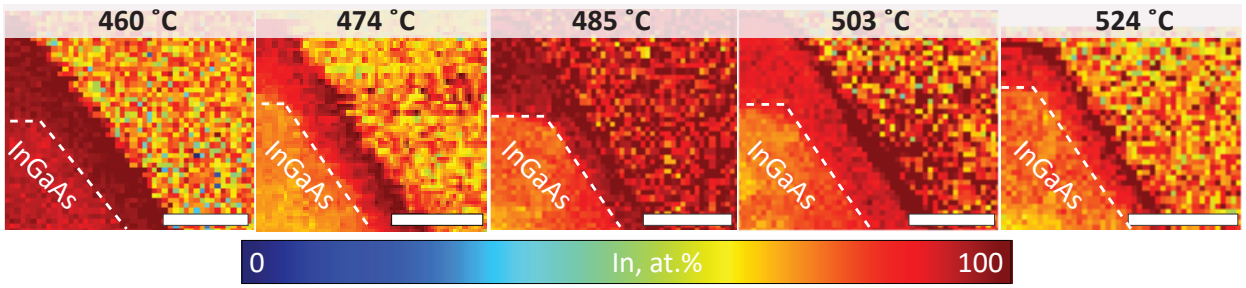

Figure 11: EELS In composition maps (zoom on the upper right corner showing a part of InGaAs and InAs, scale bar 50 nm) of the nanowires from Fig. 14 highlighting composition differences in the InAs channel with temperature.

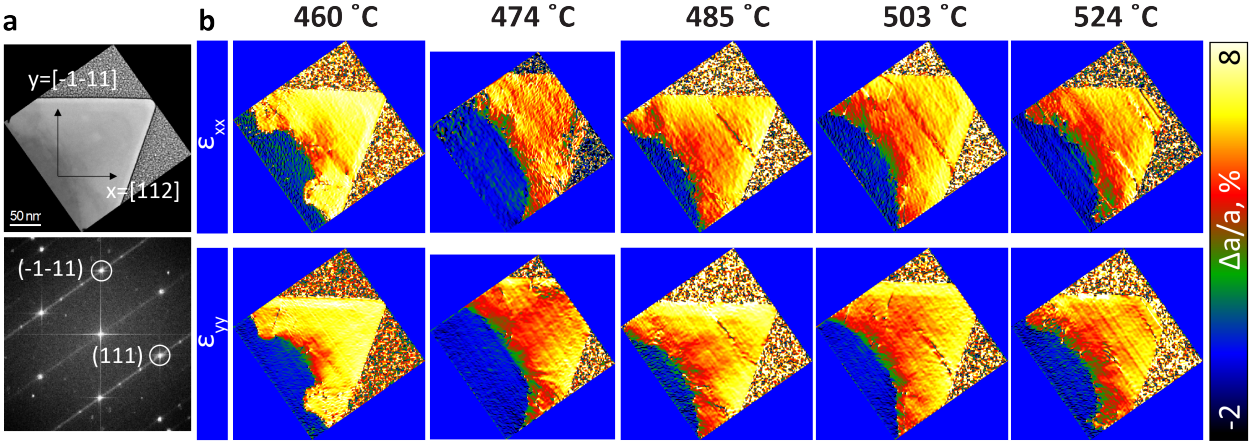

Figure 12: (a) An example of HAADF STEM image used to extract relative in-plane (ε_{xx}) and out-of-plane (ε_{yy}) lattice deformations in (b). GPA was simultaneously applied to (-1-11) and (111) planes. Then, components of the lattice mismatch were obtained by setting x direction rotated 54.75° with respect to the original direction (the new x-axis is parallel to the InAs/InGaAs interface, and thus to the [112] crystallographic orientation), the y-axis is parallel to the [-1-11] crystallographic orientation. Note, that for the sample grown at 474°C HR STEM images are taken on a nanowire which has been contacted and measured for transport properties first.

S6. InAs/InGaAs field effect mobility measurements: influence of the InGaAs buffer growth temperature.

The samples were measured in a cryogen-free DynaCool physical property measurement system (PPMS) with a base temperature of 1.7 K.

To fit differential conductance G as a function of the top gate voltage V_g and extract electron mobility μ, we use the following equation:[8,9]

$$G(V_g) = (R_s + \frac{L^2}{\mu C(V_g - V_{th})})^{-1} \tag{1}$$

where R_s is the contact resistance in a two-probe configuration, L is the channel length, C is the capacitance between the gate and the nanowire (we use the same capacitance simulations as in[10]), and V_{th} is the threshold voltage.

We fit the pinch-off curve in the high density region, which starts above the V_{gm} point at which the transconductance dG/dV_g is maximal (Fig. 13).

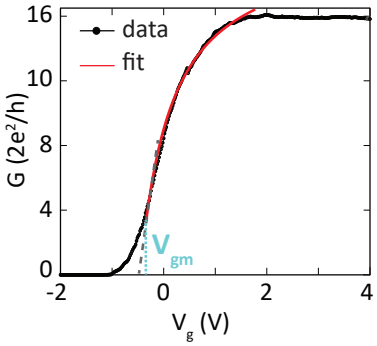

Figure 13: Differential conductance G, as a function of top-gate voltage V_g and the fitting line plotted with the use of the conductance equation (1).

Figure 14 shows G as a function of V_g. Independent of the nanowire position on the substrate, G is higher for nanowires grown at lower InGaAs growth temperatures. Note that the nanowire device grown at 520 °C has a tale in the conduction trace at negative gate voltages as opposed to the other nanowires (Fig 14b). Additional TEM lamellas of the sample shown in Fig 14d can shed light on this phenomenon. It occurs that in this sample,

the InAs thickness is often not homogeneous in the cross section: one side is markedly wider than the other side. We find that in the case of the highlighted nanowire, the InAs thickness at the left side changes from 62 nm at the corner to 40 nm at the top whereas on the right side it stays constant at around 15 nm. It is probable that one of the parasitic III-V clusters, which are formed at low InGaAs buffer growth temperatures on the oxide mask in the vicinity of nanowires, got merged with the nanowire. The cluster might provide a secondary conduction channel which changes the overall conduction trace explaining why the nanowire does not pinch off as expected.

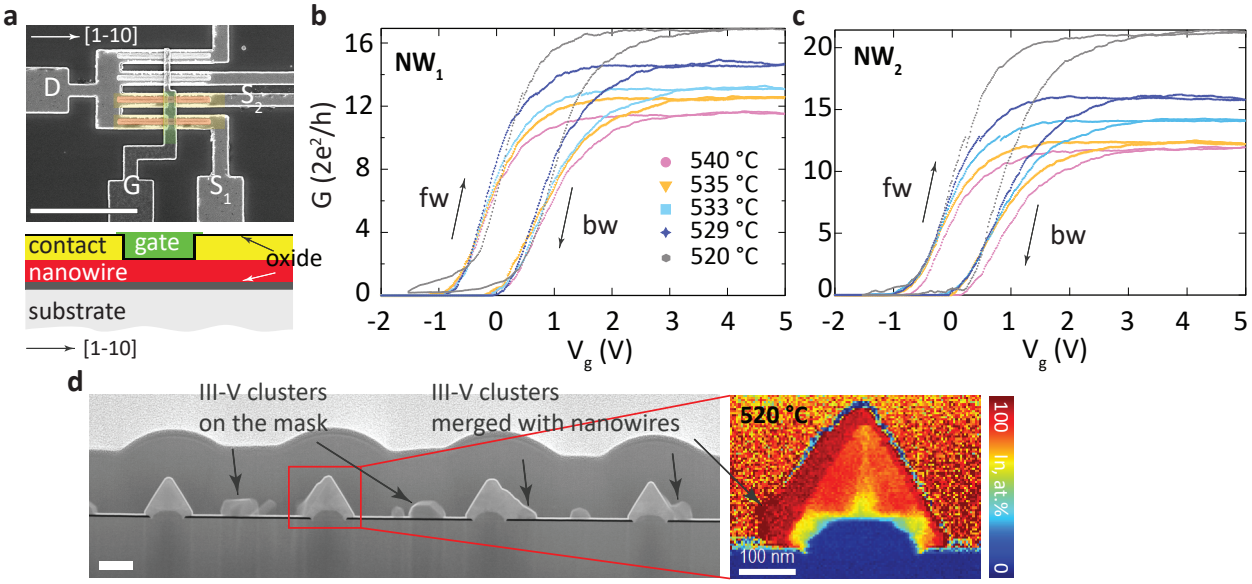

Figure 14: The role of InGaAs growth temperature on the electron mobility μ. (a) False-colored SEM image (5 μm scale bar) of a typical field effect device. D, G, S1 and S2 denote drain, gate, sources for the NW_1 and NW_2, respectively. A side-view sketch of the device (along the nanowire) is shown as well. Differential conductance G as a function of top-gate voltage V_g for NW_1 (b) and NW_2 (c). fw and bw near the curves indicate the forward and backward gate voltage sweep, respectively. (d) Low magnification HAADF-STEM image (scale bar 200 nm) of a lamella taken across [1-10]-oriented field-effect nanowires grown at 520 °C and an In atomic distribution EELS map (relative to Ga, in percentage) of the highlighted nanowire. Arrows indicate the position of III-V parasitic clusters which grow on the mask at low InGaAs growth temperature and sometimes merge with nanowires.

S7. InAs/InGaAs band structure simulations.

The conduction band energy levels and electron density distribution were simulated in 2D by solving self-consistently the Schrödinger–Poisson equations for 0, 5, 10, 15 and 20 nm InAs thickness (Fig. 15). In calculations, the InGaAs buffer layer has an In composition of x=0.8 and the InAs layer has x=0.9 as extracted from EELS on samples grown at high temperatures. Simulations were performed for a temperature of 5K with a surface charge density of 3×10^{12} $\mathrm{cm}^{-2}\mathrm{eV}^{-1}$.[11] Three gate voltages V_g were used for all simulations: -0.7 V, 0 V, and 5 V.

The simulations show that by increasing the InAs thickness from 0 to 20 nm, the bulk of conduction is confined to the InAs layer, with only a small part of the electron density tail overlapping into the InGaAs buffer.

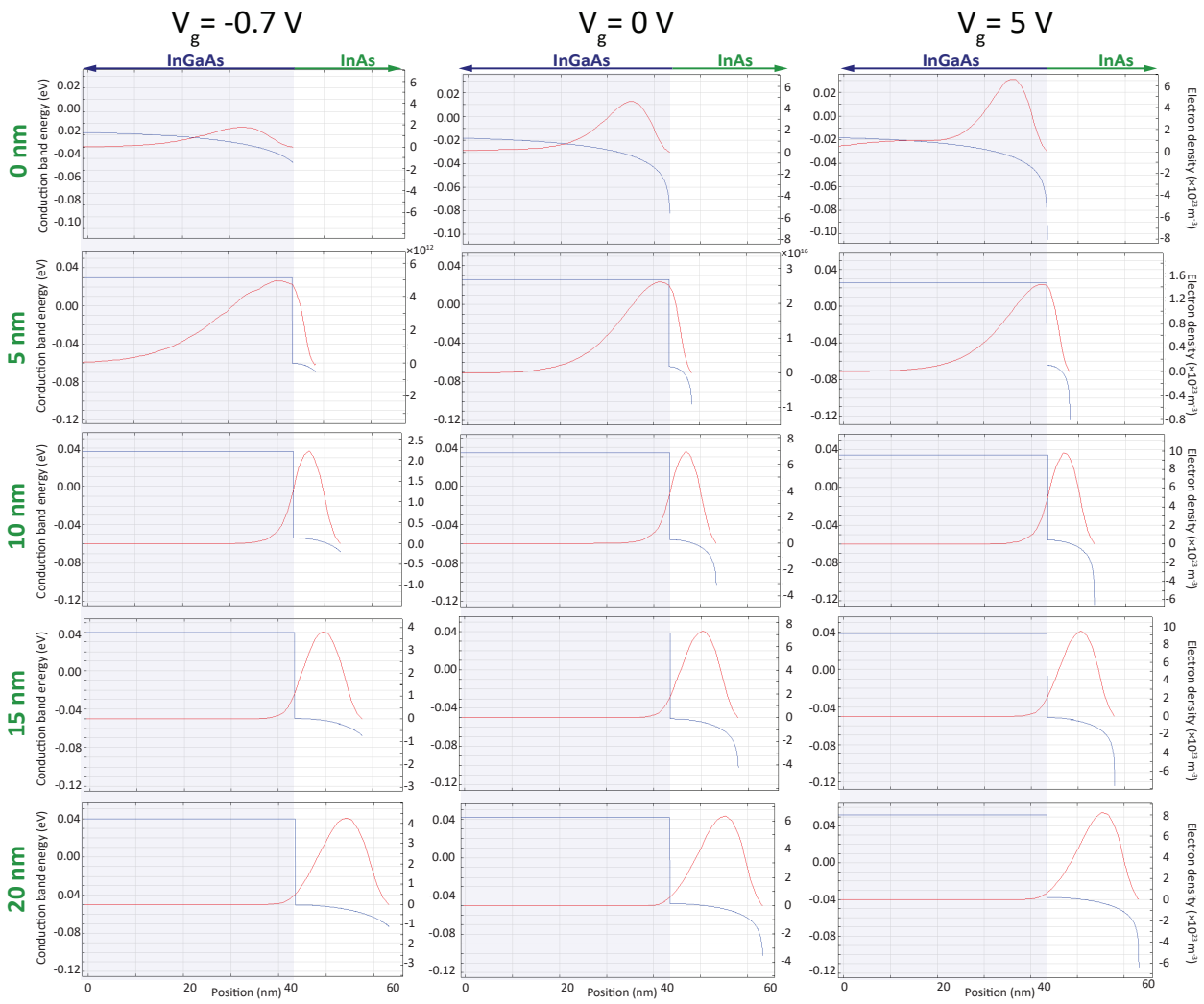

Figure 15: 2D self-consistent Schrödinger–Poisson calculations for the conduction band energy (left axis) and electron density (right axis) of the InAs/InGaAs SAG nanowires for 0, 5, 10, 15 and 20 nm thick InAs layer. Each column corresponds to three different gate voltages (indicated above the graphs).

S8. Transport measurements of InGaAs/GaAs(Sb) SAG nanowires without the InAs channel.

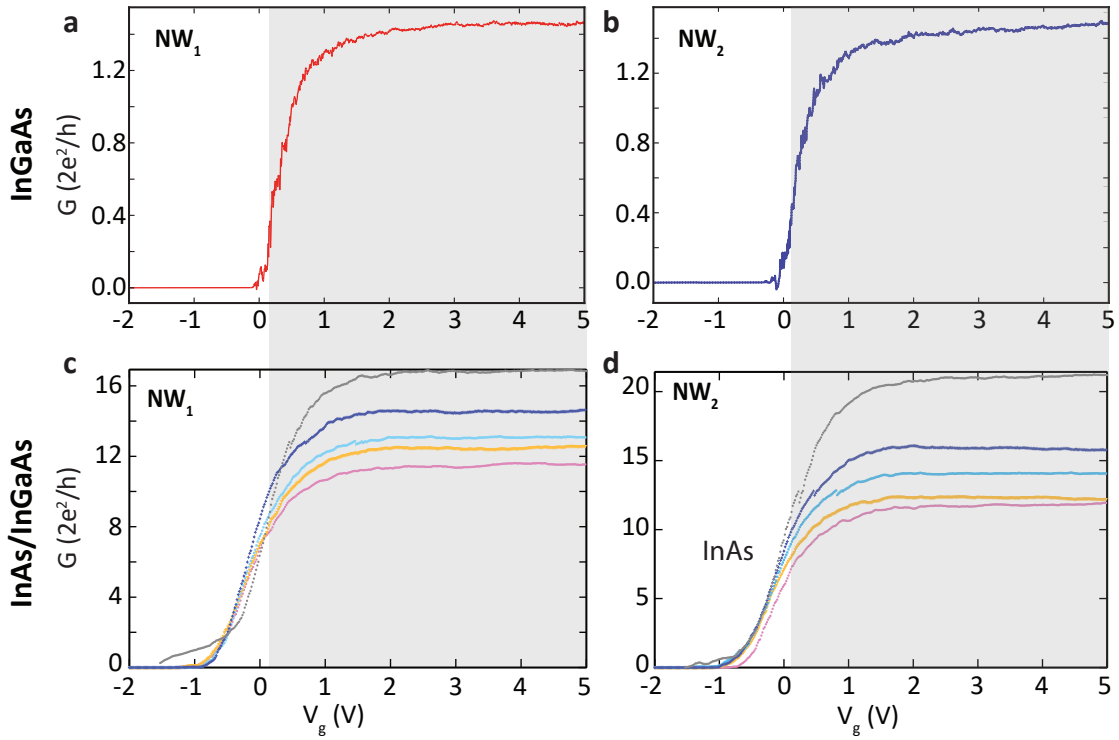

Figure 16: Comparison between conduction G traces of InGaAs/GaAs(Sb) nanowires without the InAs channel (a,b) and with the InAs channel on top (c,d). Forward traces are depicted for each of the case corresponding to two measured nanowires: NW_1 and NW_2. The region where InGaAs becomes conductive is shaded in grey. Different colors in (c,d) correspond to different growth temperature, for the details please refer to Fig. 14.

S9. InAs/InGaAs field effect mobility measurements: influence of the InAs growth temperature.

Fig. 17 displays conduction traces, G, as a function of the gate voltage, V_g, for samples E and F. Some spread in the traces is attributed to slight variations in the contact resistance, R_s, which limits the mobility at high V_g.

Table 3: List of growth parameters and transport data complementary to Table 1 in the main text. W, V_{th}, μ, n_{2D}, S_3 and S_4 denote nanowire width, threshold voltage, maximum electron mobility, carrier concentration, inner and outer nanowire, respectively. n is estimated at zero gate voltage V_g=0 via the formula $n_{2D} = C\Delta V/Ae$,[12] where C is the capacitance found with the finite element simulations as described in,[10] e is the elementary charge, $A = LW$ is the surface area, and ΔV=V_g-V_{th}.

Sample	T_{InGaAs}, °C	T_{InAs}, °C	W, nm		V_{th}, V		μ, $cm^2V^{-1}s^{-1}$		n_{2D}, 10^{12} cm^{-2}	
			S_3	S_4	S_3	S_4	S_3	S_4	S_3	S_4
E	520	520	290	290	-1.74	-2	9099	11448	7.78	8.95
F	520	470	250	250	-1.82	-1.82	7996	9655	9.48	9.48

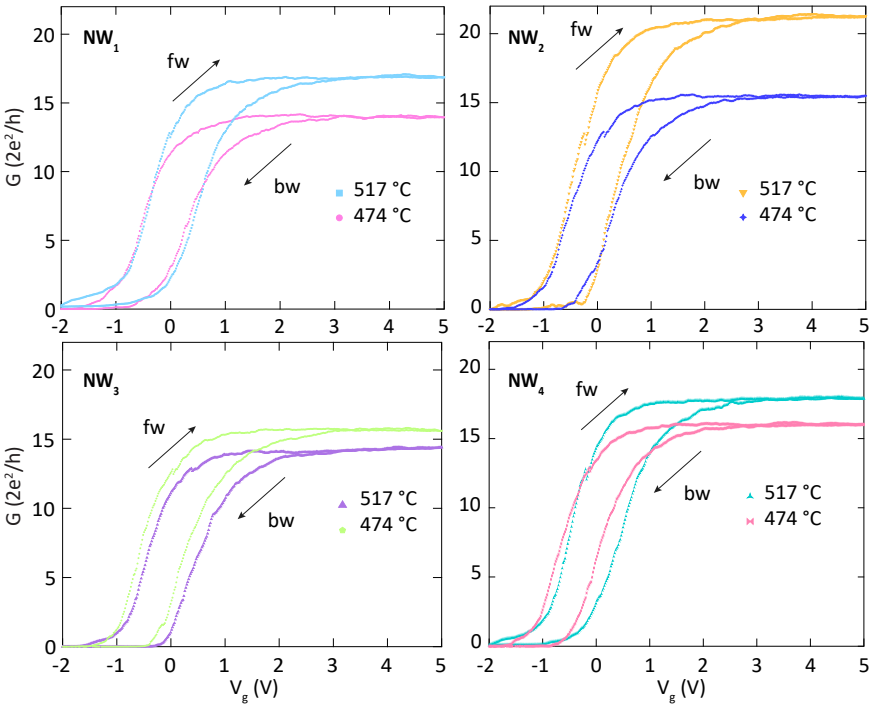

Figure 17: The role of InAs growth temperature on the electron mobility. Differential conductance G as a function of top-gate voltage V_g for NW_1 (a), NW_2 (b), NW_3 (c), and NW_4 (a) (graphs share the same x- and y-axis). Letters fw and bw near the curves indicate the forward and backward gate voltage sweep, respectively.

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