# A Compact Switched-Capacitor Multi-Bit Quantizer for Low-Power High-Resolution Delta-Sigma ADCs

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***Abstract*—This paper proposes a compact switched-capacitor (SC) multi-bit flash quantizer for low-power high-resolution delta-sigma modulators (ΔΣMs). First, a general power model for single-loop ΔΣMs is presented to show the importance of using multi-bit quantization when facing high-resolution specifications. In this context, a SC multi-bit quantizer circuit is proposed, which exhibits low-power operation, high modularity, single comparator design and compatibility with both multi-feedforward ΔΣM architectures and other SC low-power circuit techniques, like clocked comparators and switched OpAmps. A practical 50-kHz 16-bit ΔΣM design case is also presented.**

## I. Introduction

Portable smart sensing applications demand low-power high-resolution ADC circuits with a reduced bandwidth (typically below 1 MHz) but with dynamic range values exceeding 90 dB. Typically, ΔΣ modulators (ΔΣMs) are employed for these high-resolution data converters, as they relax the specifications for analog blocks at the expense of increasing signal oversampling ratios. However, their integration in modern CMOS technologies with increasing process variability and supply-voltage downscaling has become a real circuit design challenge. This fact can be noticed by the proportionally small number of circuit implementations above 15 ENOB reported in literature [1] compared to other areas of the ADC design space with similar figure-of-merit values.

A common choice to improve the dynamic range of single-loop ΔΣMs is the use of multi-bit quantization, as in the architecture example of Fig. 1(c). Compared to high-order noise shapers, which tend to introduce instability issues, or upscaled oversampling frequencies, with the corresponding increment of dynamic power consumption, the non-linearity associated with multi-bit quantization can be compensated in practice by digitally-assisted dynamic element matching (DEM) techniques at the feedback DAC. Classically, the signal summation and multi-bit quantization required in Fig. 1(c) is implemented separately at the cost of an active ladder and eventually a resistive-string for reference generation [2]. Alternatively, the use of capacitive summation based on passive charge sharing is an attractive solution because of its simplicity and low-power operation, although the corresponding signal attenuation may require pre-amplification or reference scaling [3]. Other trends in hybrid multi-bit ΔΣMs [4] replace the flash quantizer by another type of Nyquist-rate ADC, like pipeline, two-step flash, cyclic, tracking, integrating or synchronous/asynchronous successive-approximation register (SAR) [5]–[7]. In many cases, the overall ADC sensitivity and robustness against circuit non-idealities (e.g. latency) result impaired with respect to conventional ΔΣMs embedding flash quantizers. Finally, due to the supply voltage downscaling of modern CMOS technologies, it may be convenient to quantize signal amplitudes in the time/frequency domains, like the case of pulse width modulation (PWM) [8], time-encoding quantization [9], or more common voltage-to-frequency conversion by the means of voltage controlled oscillators (VCOs) [10], [11]. The latter also allows to increase the shaping order of the ΔΣM loop by simply using a phase detector instead of a frequency detector. Beside, they can be designed to automatically implement data weighted averaging (DWA) rotation on the thermometric code feeding the DAC. Unfortunately, the inherent non-linearity and process/temperature sensitivity of these schemes prevent their use in high-resolution ADCs.

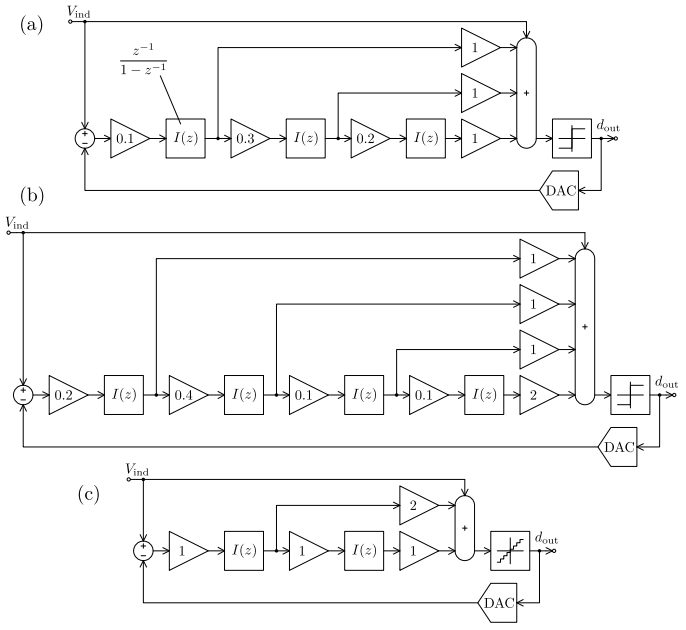


Figure 1. Comparative examples of high-resolution single-loop ΔΣMs: single-bit third-order (a), single-bit fourth-order (b) and 3-bit second-order architecture (c). Optimized coefficients obtained from [12].

This paper presents a compact switched-capacitor (SC) multi-bit flash quantizer topology for high-resolution ΔΣMs, which exhibits low-power operation, high modularity, single comparator design and compatibility with both multi-feedforward architectures and SC low-power circuit techniques, like clocked comparators and switched OpAmps [13].

## II. ΔΣ Modulator Power Model

Before introducing the new SC multi-bit quantizer circuit, this section presents a power consumption model for single-loop ΔΣMs to show the impact of architecture selection and illustrate the main trade-offs when optimizing for high resolution. For the benefit of generalization, circuit efficiency will be considered ideal, and only dynamic power consumption due to the signal processing itself will be evaluated.

In general, power consumption in a ΔΣM loop is dominated by the first integrator. Given a single-ended model clocked at $f_s$ with integrating capacitor $C_{i1}$ and supply voltage $V_{DD}$, the minimum dynamic power consumption due to the update of the state variable at the output of the first stage ($\Delta V_{out1}$) is:

$$P_{min} = \underbrace{C_{i1}\overline{|\Delta V_{out1}|}f_s}_{\overline{I_{DD}}} V_{DD} = \frac{C_{s1}}{a_1}\alpha_1 V_{DD}^2 \mathrm{OSR} f_{nyq} \qquad (1)$$
$$\alpha_1 \doteq \frac{\overline{|\Delta V_{out1}|}}{V_{DD}},$$

where $C_{s1}$ and $a_1$ are the sampling capacitor and integrator coefficient, respectively, OSR is the oversampling ratio, and the introduced parameter $\alpha_1$ indicates the normalized dynamics at the output of the first stage, which can be determined through high-level simulations.

Under a given $\mathrm{SNDR}_{peak}$ specification, and accounting for intrinsic modulator signal-to-quantization-noise ratio (SQNR), the following relations holds:

$$\mathrm{SNDR}_{peak}^{-1} = \mathrm{STNR}^{-1} + \mathrm{SQNR}^{-1}, \qquad (2)$$

$$\mathrm{STNR} = \frac{A_{peak}^2}{2}\frac{C_{s1}\,\mathrm{OSR}}{kT} = \frac{\alpha_{OL}^2 V_{DD}^2}{8}\frac{C_{s1}\,\mathrm{OSR}}{kT}; \qquad (3)$$

$$\alpha_{OL} \doteq \frac{2A_{peak}}{V_{DD}}, \qquad (4)$$

where STNR is the signal-to-thermal-noise ($kT/C$) ratio of the ΔΣM modulator determined by the input peak amplitude $A_{peak}$, which in turn can be related to the theoretical available input full-scale ($V_{DD}$) through the attenuation coefficient $\alpha_{OL}$ here also defined. As usual, $k$ stands for the Boltzmann constant and $T$ is the absolute temperature. Now equations (2)-(4) can be rewritten in order to determine $C_{s1}$:

$$C_{s1} = \frac{8kT\,\mathrm{SNDR}_{peak}}{\alpha_{OL}^2 V_{DD}^2\,\mathrm{OSR}\,(1-\alpha_{QN})}; \qquad \alpha_{QN} \doteq \frac{\mathrm{SNDR}_{peak}}{\mathrm{SQNR}} < 1. \qquad (5)$$

Modulator architecture and parameters must be chosen in order to have a SQNR larger than the expected resolution, formally expressed by the inequality in (5). A closer look at the same equation will also reveal that $\alpha_{QN}$ is a function of OSR through SQNR, indicating two things: sampling capacitor does not scales proportionally to the inverse of OSR; once a specific architecture is chosen, a minimum OSR must be adopted in order to satisfy the inequality in (5). Finally, the expression for the minimum dynamic power consumption can be derived once (5) is substituted into (1):

$$P_{min} = \mathrm{SNDR}_{peak}\, f_{nyq}\, 8kT\, k_{mod}, \qquad (6)$$

$$k_{mod} \doteq \frac{\alpha_1}{a_1\,\alpha_{OL}^2\,(1-\alpha_{QN})}. \qquad (7)$$

Basically, the above model lumps all the ΔΣM architecture details in the $k_{mod}$ coefficient (i.e. internal dynamics, capacitor scaling, input full-scale loss and quantization noise margin), while on the other side only standard ADC performance ($\mathrm{SNDR}_{peak}$ and $f_{nyq}$) and operative conditions ($kT$) are specified. In order to validate the above power model, four high-resolution ΔΣM design examples are evaluated with a common 50-kHz bandwidth and 16-bit $\mathrm{SNDR}_{peak}$ specification at room temperature: the single-bit third-order ΔΣM architecture of Fig. 1(a) running at ×128 oversampling ($L$=3, OSR=128, $N$=1) as a design reference; the still single-bit but fourth-order modulator of Fig. 1(b) operated at ×96 Nyquist rate ($L$=4, OSR=96, $N$=1); the 3-bit second-order ΔΣM loop of Fig. 1(c) when overclocked at ×128 ($L$=2, OSR=128, $N$=3); and the same multi-bit architecture but reducing its oversampling ratio down to ×96 ($L$=2, OSR=96, $N$=3). Fig. 2 to 4 show the results obtained from their behavioral simulation, while Table I summarizes the extracted coefficients for the power model.

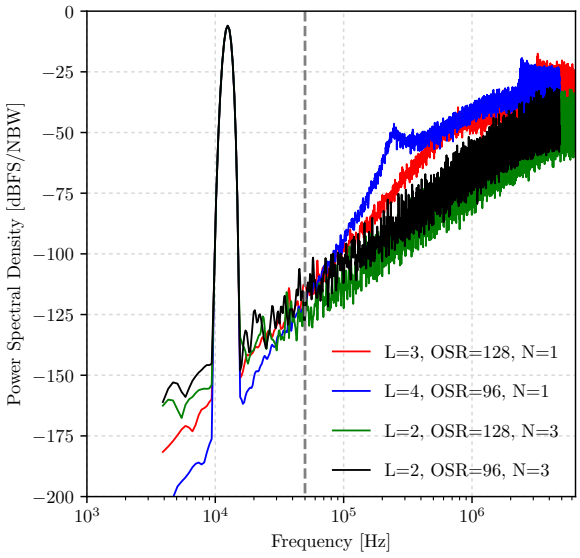


Figure 2. Output PSDs for the four ΔΣM design examples at $-6\mathrm{dB_{FS}}$ input.

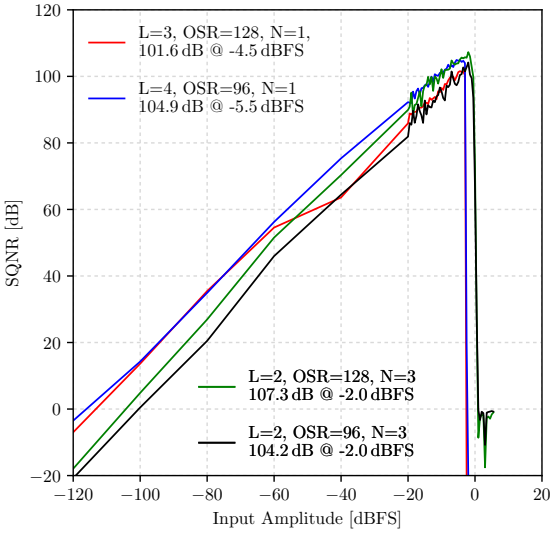


Figure 3. SQNR curves and peak values for the four ΔΣM design examples.

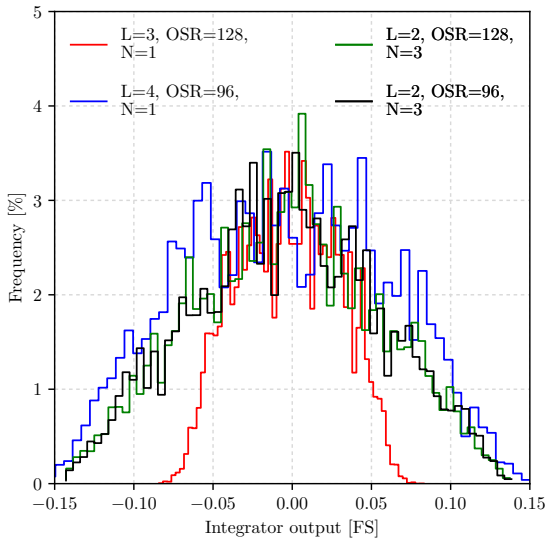


Figure 4. Histograms of the first-integrator occupancy ($V_{\text{out1}}$) for the four ΔΣM design examples. Note that these statistics do not apply for $\Delta V_{\text{out1}}$.

Table I. POWER MODEL (7) FOR THE FOUR ΔΣM DESIGN EXAMPLES.

| **Parameter** | $L$=3 OSR=128 $N$=1 | $L$=4 OSR=96 $N$=1 | $L$=2 OSR=128 $N$=3 | $L$=2 OSR=96 $N$=3 |
|---|---|---|---|---|
| $a_1$ | 0.1 | 0.2 | 1 | 1 |
| $\alpha_1$ | 0.0411 | 0.0859 | 0.0823 | 0.0821 |
| $\alpha_{\text{OL}}$ | 0.596 | 0.531 | 0.794 | 0.794 |
| $\alpha_{\text{QN}}$ | 0.449 | 0.206 | 0.120 | 0.246 |
| $k_{\text{mod}}$ | 2.103 | 1.921 | 0.148 | 0.173 |

According to the proposed ΔΣM power model, the combination of multi-bit quantization with low-order noise shaping and moderate oversampling ratios can save almost one order of magnitude on dynamic power consumption, regardless the particular CMOS circuit realization. This prediction is consistent with the simulation results of Fig. 5. Hence, it is clear the interest of multi-bit quantizer circuits when optimizing the power efficiency of high-resolution ΔΣMs.

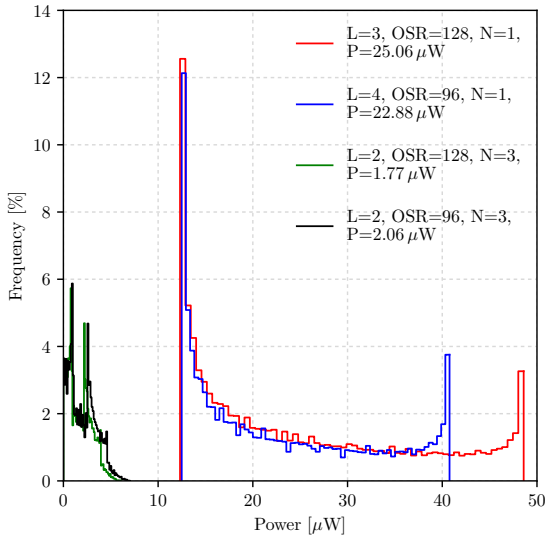


Figure 5. Histograms and averages of the first-integrator dynamic power consumption for the four ΔΣM design examples.

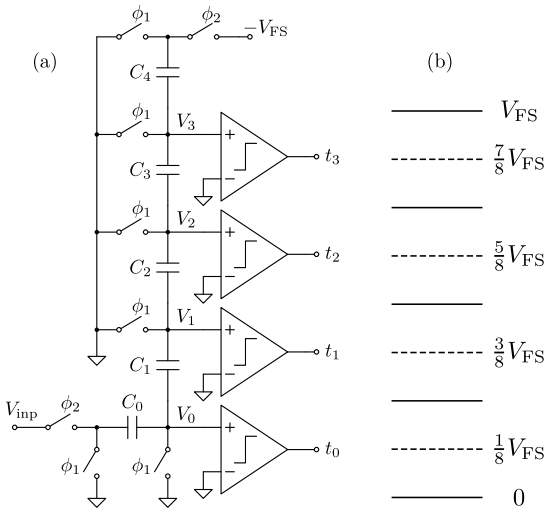


Figure 6. Half-circuit SC topology of the proposed multi-bit quantizer for the 9-level design case (a) and equivalent thresholds (b).

## III. COMPACT SC MULTI-BIT QUANTIZER

Fig. 6(a) shows the half-circuit SC topology of the new multi-bit quantizer for the 9-level design case. The proposed scheme incorporates a ladder network of matched capacitors $C_{0\cdots4}$ operated with non-overlapped clock phases $\phi_{1,2}$, where $V_{\text{FS}}$ stands for the input full scale of the half circuit and $t_{3\cdots0}$ is the generated thermal code. During $\phi_1$, all capacitors are reset. Once in $\phi_2$, $C_0$ samples the input signal $V_{\text{inp}}$ to be quantized and charge redistribution occurs in the ladder so the proper voltages $V_{0\cdots3}$ are established at the input of each comparator. For the purpose of implementing the quantization thresholds of Fig. 6(b), an specific capacitance ratio $C_j/C_0$ is required for each element $j$=1…4. Indeed, the design of the capacitive ladder network involves a linear system of $n$ equations, being $1+2n$ the number of quantization levels. It can be shown that the general solution follows:

$$\frac{C_j}{C_0} = \begin{cases} \dfrac{4(j+n)^2-1}{4n(1+2n)} & j \in [1\ldots n-1] \\ \dfrac{1}{(1+2n)\left(1-4n\sum\limits_{i=0}^{n-1}\frac{1}{4(j+n)^2-1}\right)} & j=n \end{cases} . \quad (8)$$

In the particular case of Fig. 6 ($n$=4), the exact matching ratios are $C_{1\cdots4}/C_0$={$\frac{11}{16}$,$\frac{143}{144}$,$\frac{65}{48}$,$\frac{5}{24}$}. In practice, such ratios can be rounded according to the layout convenience thanks to the robustness against technology mismatching exhibited in Fig. 7. One advantage of the proposed quantizer is its compactness and modularity that translates into low-power operation. Also, since all comparators of Fig. 6 latch at the same voltage threshold, a single CMOS circuit design can be reused. Furthermore, the proposed quantizer is compatible not only with other low-power SC techniques, like clocked comparators and switched OpAmps, but also with multiple-feedforward ΔΣM architectures, as shown in the design example of next section. In terms of signal attenuation, the maximum loss caused by the passive network of Fig. 6(a) corresponds to $V_{n-1}$ and equals $\frac{2n-1}{4n-1}$, which is around 6 dB. Finally, the effect of parasitic capacitance at the input of each comparator should be in principle neglectable according to the results of Fig. 8.

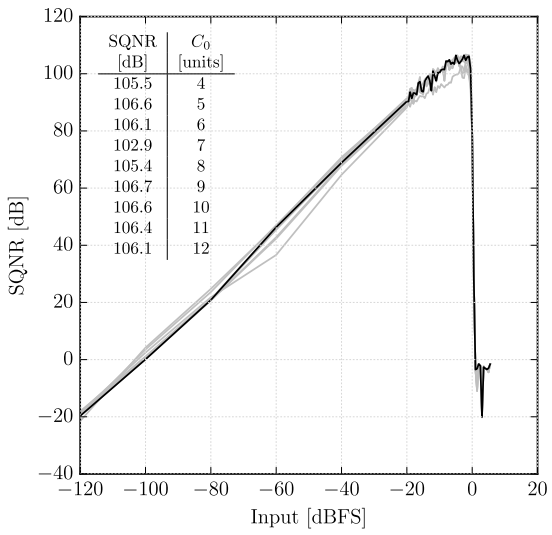


Figure 7. SQNR curves and peak values for the ΔΣM design example of Fig. 1(c) when using the proposed multi-bit quantizer of Fig. 6 as a function of the capacitance matching granularity in (8).

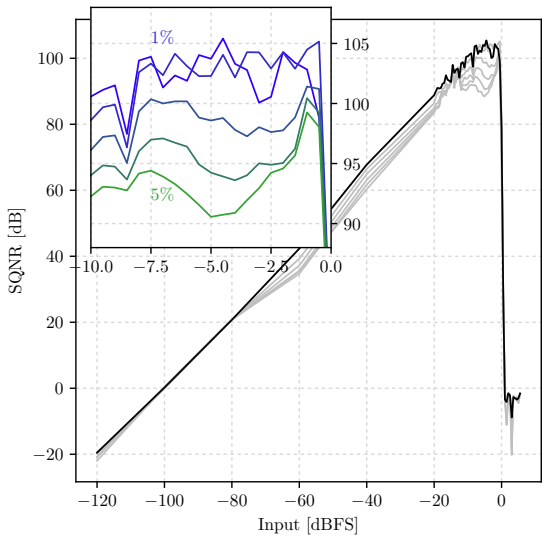


Figure 8. SQNR curves for the ΔΣM design example of Fig. 1(c) when using the proposed multi-bit quantizer of Fig. 6 as a function of the comparator parasitic capacitance normalized to the quantizer sampling capacitor $C_0$.

## IV. Design Example

In order to demonstrate the capabilities of the proposed multi-bit quantizer for high-resolution ΔΣMs, the 9-level circuit design example of Fig. 6 have been applied to the second-order architecture of Fig. 1(c) to achieve a target bandwidth and dynamic range of 50 kHz and 16 bit, respectively. The equivalent SC schematic is shown in Fig. 9 with 2-$V_{pp}$ differential full scale ($V_{lo}$=0.4V and $V_{hi}$=1.4V at 1.8-V supply) and 12.8-MHz sampling rate (OSR=128). In this case, switched OpAmps are also employed at the noise shaper to save power consumption, while bubble error correction (BEC) and DEM assisted techniques are used at the quantizer and the feedback DAC, respectively. The exact capacitance ratios from (8) have been simplified to $C_{1\cdots4}/C_0=\{\frac{11}{16},\frac{143}{144},\frac{65}{48},\frac{5}{24}\}\simeq\{\frac{3}{4},\frac{4}{4},\frac{5}{4},\frac{1}{4}\}$

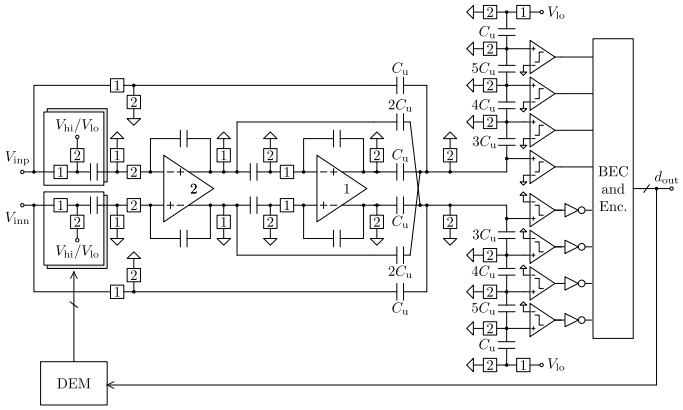


Figure 9. Simplified schematic of a 9-level second-order SC ΔΣM circuit using the proposed multi-bit quantizer of Fig. 6.

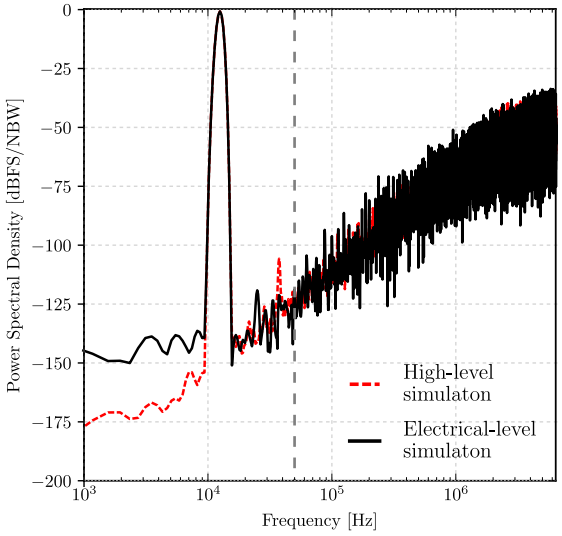


Figure 10. Output PSDs for the 9-level second-order SC ΔΣM circuit of Fig. 9 obtained from behavioral and electrical simulation at $-1\text{dB}_{\text{FS}}$ input.

with unitary capacitance $C_u$=0.5pF. In this sense, the 4-$C_u$ multiplicity of $C_0$ is also exploited in Fig. 9 to implement the weights of the nested feedforward paths of Fig. 1(c). The ΔΣM results obtained in Fig. 10 return good SQNR matching between behavioral and electrical simulations.

## V. Conclusions

A power model for single-loop ΔΣMs has been presented to show the importance of using multi-bit quantization when facing high-resolution ADC specifications. In this context, a compact SC multi-bit flash quantizer topology has been proposed, which exhibits low-power operation, high modularity, single comparator design and compatibility with both multi-feedforward ΔΣM architectures and SC low-power circuit techniques, like clocked comparators and switched OpAmps. A practical 50-kHz 16-bit ΔΣM design case has been presented to demonstrate the capabilities of the proposed multi-bit quantizer circuit. This work has been partially funded by European Commission H2020-FETPROACT-2016-732032 and supported by TecnioSpring+ TECSPR16-1-0056.

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