Solid-source molecular-beam epitaxy for monolithic integration of laser emitters and photodetectors on GaAs chips

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(Received 11 August 2000; accepted for publication 10 October 2000)

A solid-source molecular beam epitaxy has been used to grow Al-free InGaP/GaAs/InGaAs in-plane side emitting laser (IPSELS) devices on foundry available GaAs integrated circuits (IC) chips with integrated metal–semiconductor–metal photodetectors. The GaAs IC chips were cleaned at low temperature (470 °C) by monoatomic hydrogen prior to epitaxy. Br₂ reactive ion etching was used after growth to make laser facets and parabolic mirrors for vertical emission. Using these techniques, we obtained laser emission from the integrated IPSEL devices, suggesting that these devices may be an alternative approach to that offered by vertical cavity surface emitting lasers in the fabrication of optoelectronic integrated devices. © 2000 American Institute of Physics.

[S0003-6951(00)03250-2]

The integration of microelectronics and optoelectronic devices has been and still is an important goal in semiconductor technology. Devices that implement both light sources and light detectors with integrated electronics for self-control and signal processing in a single chip are interesting for a variety of applications ranging from optical communications to high performance sensors. Optoelectronic devices like light emitting diodes (LEDs) or laser diodes are typically made on compound semiconductors whereas high-density microelectronics like amplifiers, drivers, etc., are typically made on silicon. The differences in the properties and processing technologies between both types of semiconductors made it difficult to integrate optoelectronic devices with microelectronics. Some results have been obtained through the monolithic integration of III–V devices directly on silicon¹ or using hybrid integration of both materials.² More recently, wafer bonding techniques have been used to produce Si and GaAs compatible substrates for monolithic integration of III–V heterostructures.³ An alternative approach⁴ consists of using a single material for both types of devices, like GaAs, to integrate the electronic and optoelectronic devices monolithically on the same substrate. In this approach, the high-density GaAs integrated circuits (IC) chips are made in a foundry using a commercially available process.⁵ The chips hold integrated metal–semiconductor–metal (MSM) photodetectors and specially designed channels and windows for the epitaxial growth of the laser emitters based on our previous experience.^{6,7} A critical aspect is that the thin electrical interconnections inside the chip can not stand temperatures higher than 475 °C for a long time without exhibiting some degree of degradation.⁸ A procedure has been developed for the monolithic integration of resonant tunneling diodes⁹ and LEDs¹⁰ on very large scale

integrated-GaAs chips. In this letter, we show the feasibility of this method for the implementation of in-plane side emitting laser devices (IPSELS) with MSM photodetectors and high-density electronics on GaAs-IC chips.

Solid-source molecular-beam epitaxy (MBE) was used to grow, at a low temperature (470 °C), the semiconductor heterostructures for the laser emitting devices. Substrate cleaning prior to the epitaxy was achieved by means of a molecular beam of monoatomic hydrogen. After the growth by MBE, some polycrystalline material was deposited on top of the noncrystalline surface of the GaAs chips out of the channels and windows. This polycrystalline material is removed by bromine ion-beam assisted etching (Br₂-IBAE).¹¹ Br₂-IBAE was also used for the fabrication of the mirrors for the laser devices and for the parabolic mirrors that reflect the light for vertical emission upward. Metallic contacts were deposited on top of the devices.

GaAs-IC chips with size of $\sim 4 \times 4$ mm were received from foundry following our previous design as the substrate. The design implements regions designated for the growth of the laser devices, with the shape of windows and channels, where the SiO₂-based interconnect dielectric stack can be removed to reveal the underlying GaAs substrate. Fig. 1 shows the three different stages for the implementation of the laser emitters on the as received GaAs-IC chip. Fig. 1(a) shows a cross section of one of the channels after all the dielectric layers have been etched away to expose the bottom of the channel (foundry contacted n^+ implanted GaAs) to air. These dielectric layers separate the different metals (up to four) used for the electronics interconnections. The epitaxial growth by MBE will take place on the channels and windows right after the n^+ GaAs surface is exposed to air. Standard UV photolithography and wet etching with peroxide and buffered oxide etch (BOE) were performed on the GaAs chip to open the channels and windows. Wet etching with peroxide and BOE has shown to give a better surface quality for epitaxial growth than that obtained by dry etching. Once

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FIG. 1. Schematic views of the three stages needed for the implementation of the IPSEL structures. (a) shows a cross section of a portion of the chip with the channel for epitaxial growth of the IPSEL structures already exposed to air. (b) shows the stage after MBE growth of the $\text{In}_{0.48}\text{Ga}_{0.52}\text{P}/\text{GaAs}/\text{In}_{0.2}\text{Ga}_{0.8}\text{As}$ SQW laser structure. Material grows crystalline inside the channel and polycrystalline on top of the chip. (c) shows the device completed with etched mirrors and a parabolic deflector for vertical emission.

the channels have been exposed to air, the GaAs-IC chip and a control sample of regular GaAs (001) are mounted with indium on a 3 in. Si wafer and introduced into the MBE chamber. The GaAs control sample allows also the monitoring of the reflection high-energy electron diffraction pattern during MBE growth. We used a GaP decomposition source for the production of phosphorous and a thermal cracker for the production of atomic hydrogen needed for desorption of the surface oxide at low temperature (470 °C).

We selected for the laser emitters a single quantum well (SQW) heterostructure based on the ternary alloy $\text{In}_{0.48}\text{Ga}_{0.52}\text{P}$, which is lattice matched to GaAs. $\text{In}_{0.48}\text{Ga}_{0.52}\text{P}$ has a much lower trap concentration than $\text{Al}_x\text{Ga}_{1-x}\text{As}$ grown at the low temperature needed for the monolithic integration of the laser emitters (470 °C).^{12,13} $\text{In}_{0.48}\text{Ga}_{0.52}\text{P}$ presents also an interface recombination velocity lower than $\text{Al}_x\text{Ga}_{1-x}\text{AsGaAs}$,¹⁴ a larger band gap and is Al-free, which increases device lifetimes.^{15,16} For reference SQW laser diode heterostructures with $\text{In}_{0.48}\text{Ga}_{0.52}\text{P}$ for the barriers and GaAs/ $\text{In}_{0.2}\text{Ga}_{0.8}\text{As}$ for the active region with cleaved facets had been previously grown on GaAs at low temperature (470 °C) in our MBE system.¹⁷ Figure 2 shows the complete laser structure, with 1 μm InGaP barriers and a 60 Å $\text{In}_{0.2}\text{Ga}_{0.8}\text{As}$ SQW. We have grown on the GaAs-IC chips similar laser structures at 470 °C, but with a thicker (4.2 μm) buffer layer of Si-doped GaAs in order to completely fill up

FIG. 2. Schematic drawing of the $\text{In}_{0.48}\text{Ga}_{0.52}\text{P}/\text{GaAs}/\text{In}_{0.2}\text{Ga}_{0.8}\text{As}$ SQW laser structure grown at low temperature (470 °C) by solid-source MBE.

the channels and to obtain a planar surface on top of the device. Special care was taken when increasing or decreasing the temperature of the chips inside the MBE since fast variations of the substrate temperature can produce damage in the electronics due to thermal stress.

Figure 1(b) shows the cross section after the MBE growth has been performed. Single-crystal epitaxial material is deposited along the channels and windows prepared for this purpose, whereas polycrystalline material has grown on top of the chip. Removing the polycrystalline material is achieved by deposition of a SiO_2 mask by plasma-enhanced chemical vapor deposition to protect the epitaxial areas and dry etching with $\text{Br}_2\text{-IBAE}$ at 200 °C. Another photolithography step is needed to etch the SiO_2 mask with buffered HF. The surface of the chip is then planar and ready for the fabrication of the side facets of the laser devices which act as mirrors of the Fabry-Perot cavity. $\text{Br}_2\text{-IBAE}$ is used to straight etch the side facets and the parabolic mirrors (on one side of the laser devices only) that deflect the light coming from the sides of the IPSELS upward. The parabolic shape of

FIG. 3. Two Nomarsky photomicrographs of the 4×4 mm GaAs chip. Panel on the left-hand side shows the chip immediately before MBE growth with the channels and windows exposed to air. Panel on the right-hand side shows the final view of the chip after the IPSEL devices have been implemented on it.

FIG. 4. I - L curve of an IPSEL device with a size of $250 \times 50 \mu\text{m}$ under pulsed current at 7°C . Pulse width was $1 \mu\text{s}$ with a duty cycle of 0.1%. Laser threshold density current calculated is $\sim 4.3 \text{ kA/cm}^2$.

the mirrors is achieved by using a computer controlled tilting platform inside the reactive ion etching (RIE) machine.¹¹ Ti-Au angle evaporation is used to make the p -type contacts on top of the IPSELS, meanwhile covering the parabolic side of the mirror with metal will enhance reflection. Finally CF_4/O_2 RIE dry etch was used to open the chip bond pads that connect the top of the chip with the n -type GaAs implanted along the bottom of the channels and windows. Fig. 1(c) shows the final aspect of the IPSEL device as previously described.

Figure 3 shows two Nomarsky pictures of the GaAs chip. The left-hand side one corresponds to the stage immediately prior to the MBE growth [the stage indicated by Fig. 1(a)]. The right-hand side one corresponds to the final stage after the MBE growth and the rest of fabrication process [stage indicated by Fig. 1(c)]. Despite the high number of fabrication steps involved, the final chip exhibits a surface free of defects or breaking features. 12 IPSEL devices with sizes ranging from 250×50 to $1000 \times 100 \mu\text{m}$ are defined along channels and 10 more on windows, with more than 30 smaller side emitting devices. Figure 4 shows the I - L curve obtained from a $250 \times 50 \mu\text{m}$ device at 7°C on a temperature controlled platform, providing 4.3 kA/cm^2 for threshold current under pulsed operation with a pulse width of $1 \mu\text{s}$ and a duty cycle of 0.1%. This threshold current is higher than that obtained from the previously cleaved laser devices.¹⁷ (in the

order of 0.3 kA/cm^2). The lower-than-expected performance may be due to the use of etched side facets made by dry etching and/or the presence of dislocations along the sides of the semiconductor material grown in the channels and windows. Further work is needed to study and solve these critical issues.

In summary, we have shown that solid-source molecular-beam epitaxy at low temperature is a suitable technique for the monolithic integration of laser emitters on GaAs-IC chips. Dry etching has been used for the definition of the side facets and reflective parabolic mirrors of the devices. Further improvement of the devices is needed to achieve a higher yield and lower threshold currents.

One of the authors P.A.P. would like to acknowledge the support of a M.E.C. Postdoctoral Fellowship from the Spanish Ministry of Education.

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