Hot carrier reliability in deep-submicrometer LATID NMOSFETs

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Abstract

The hot-carrier degradation of Large Angle Tilt Implanted Drain (LATID) NMOSFETs of a 0.35µm CMOS technology is analysed and compared to the degradation behaviour of standard LDD devices. LATID NMOSFETs are found to exhibit a significant improvement in terms of both, current drivability and hot-carrier immunity. By means of I-V characterisation and charge pumping measurements, the different factors which can be responsible for this improved hot-carrier resistance are investigated. It is shown that it must be attributed to a reduction of the maximum lateral electric field along the channel, but not to a minor generation of physical damage for a given electric field or to a reduced I-V susceptibility to a given amount of generated damage.

1. Introduction

The problems associated with hot carriers have been recognised as one of the major constraints in Si MOS scaling. Hot carriers are generated by the high electric fields existing near the drain MOSFETs junction and may attain sufficient energy to cause damage in this region, which leads to a gradual degradation of transistor characteristics [1].

In the past years, many works have focused on gate insulators reliability, so as to achieve a reduction of electron trapping and interface state generation. However, with the high quality of state-of-the-art gate dielectrics, new directions, such as the reduction of the maximum lateral electric field along the channel, E_m, have been investigated. In this way, Lightly Doped Drain, LDD, devices make use of a lightly doped region (n^-) between the channel and the drain n^+ region [2].

In recent years, Large Angle Tilt Implanted Drain, LATID, devices have been reported to increase the hot-carrier reliability of submicrometer MOSFETs [3]. This hot-carrier improvement is thought to arise from the longer overlapping between the gate and the n^- region, which leads to a smaller value for E_m, together with a deeper drain current path, which can contribute to diminish the hot-carrier degradation rate and the susceptibility to generated damage [4]. However, to our knowledge, the influence of these different factors on the hot-carrier reliability of LATID NMOSFETs has not been specifically analysed.

In this paper, the hot-carrier degradation of LDD and LATID NMOS transistors of a 0.35µm CMOS technology is analysed and compared by means of I-V and charge pumping measurements. A significant difference in terms of hot-carrier reliability is observed between these two different architectures and the ultimate reasons giving rise to this behaviour are analysed.

2. Devices and experimental procedure

The n-channel MOSFETs used in this work were fabricated using a 0.35µm CMOS technology

with LDD and LATID architectures. The specific dimensions of the transistors under study were: L=0.25-0.85μm, W=40μm, 8nm-thick SiO_2 gate dielectric and 0.12μm-long oxide spacers.

Previous to the study of device degradation, an electrical characterisation was carried out, so as to evaluate the most representative aspects of drain (I_d) and substrate (I_{sub}) characteristics (Figs. 1 and 2). For a fixed bias condition, a lower drivability (I_d) and a higher I_{sub} for the LDD transistors was observed, furthermore, the gate voltage leading to maximum substrate current was determined to be at $V_g \approx V_d/2$-0.75V (Fig. 2).

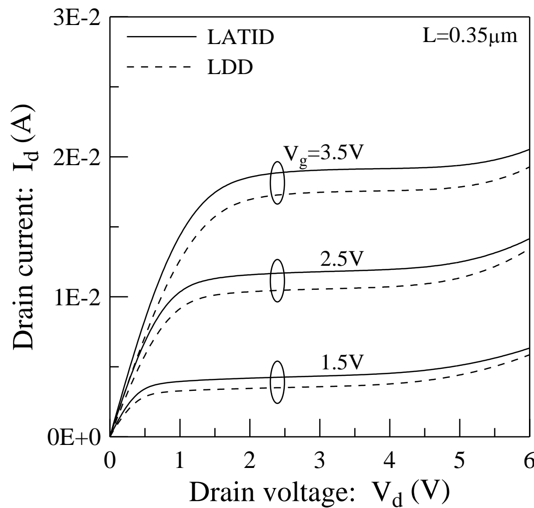

Fig. 1. I_d vs. V_d characteristics measured for L=0.35μm LDD and LATID devices.

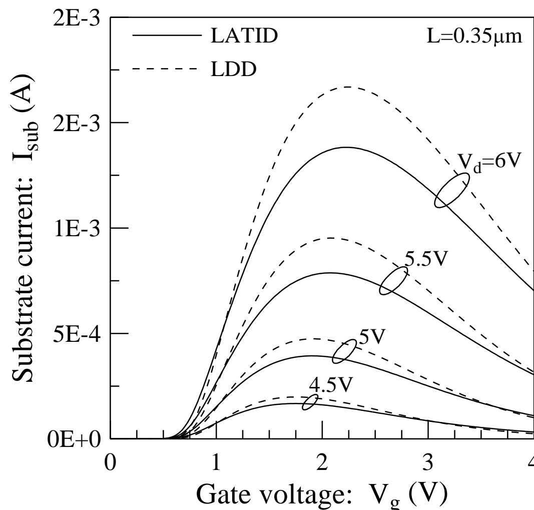

Fig. 2. I_{sub} vs. V_g characteristics measured for L=0.35μm LDD and LATID devices.

For the hot-carrier degradation analysis, the transistors were stressed at constant-voltage stress condition, with V_d ranging between 4.5 and 7V and V_g corresponding to the maximum substrate current condition, which was experimentally found to give rise to the most severe degradation.

In order to evaluate device degradation, I_d vs. V_g at V_d=0.1V characteristics were regularly measured between different stress phases. From these curves, threshold voltage ($V_{th} \equiv V_g$ @I_d=0.01W/L μA), maximum transconductance (G_{mmax}) and linear drain current measured at V_g=3.3V (I_{dlin}) were obtained and used as the primary degradation monitors. Device lifetime (τ) was then defined as the time required to reach 10% degradation of any of the two last parameters. In addition, charge pumping measurements were carried out and the charge pumping current increase at a frequency of 250kHz, ΔI_{cp}, was adopted as the indicator for interface state generation after each hot-carrier stress phase.

The fully automated experimental set-up used for both, the electrical characterisation and the stress experiments, consisted of an HP 4142B modular DC source/monitor, an HP 4085A switching matrix and a Wentworth automatic wafer prober. A Keithley 3940 pulse generator and a 485 picoammeter were used for the charge pumping measurements. All experiments were carried out in a light-proof and electrically shielded probe station.

3. Results and discussion

3.1 Device degradation: LDD vs. LATID

During the aging experiments, no significant threshold voltage shifts were registered, whereas device degradation was evaluated through the evolution of I_{dlin} and G_{mmax}. Fig. 3 shows an example of the stress time evolution of I_{dlin} and G_{mmax} degradation for 0.35 μm devices subjected to two different aging biases. For LDD and LATID transistors with similar drive current and effective channel length, stressed at identical voltage conditions, less degradation is always registered in LATID devices.

In the case of Fig. 3 results, LATID devices exhibit an improvement of about one decade of time at V_d=5V in both, I_{dlin} and G_{mmax} degradations, compared to LDD devices. Following this trend, by means of hot-carrier aging experiments carried out

throughout the whole V_d range (Fig. 4), it has been estimated a maximum drain voltage for 10 years lifetime of 3.5 and 3.75V for 0.35μm LDD and LATID devices, respectively.

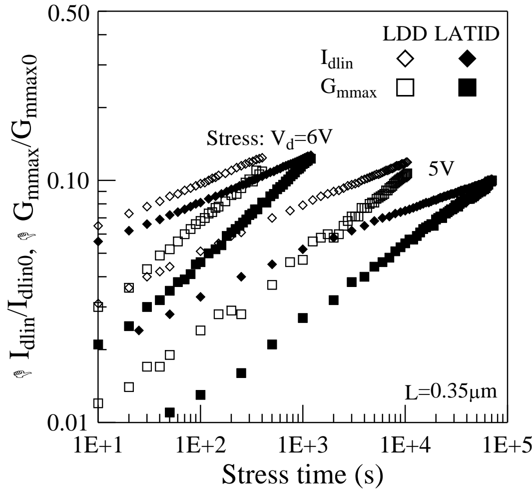

Fig. 3. I_{dlin} and G_{mmax} relative degradation ($\Delta I_{dlin}/I_{dlin0}$ and $\Delta G_{mmax}/G_{mmax0}$) vs. aging time for 0.35μm LDD and LATID devices stressed at two different biases.

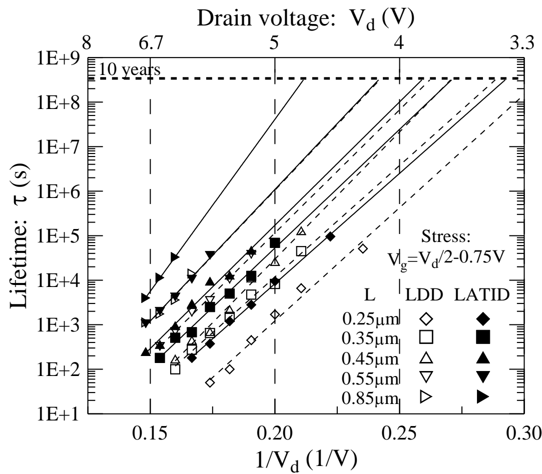

Fig. 4. τ vs. $1/V_d$ plot and 10 years lifetime extrapolation for LDD and LATID devices of different gate lengths stressed under maximum substrate current condition.

3.2 Hot carrier reliability analysis

In view of these results, a detailed investigation was carried out, so as to determine the ultimate reasons giving rise to the hot-carrier reliability improvement shown by the LATID devices.

Three possible contributions to the LATID improved hot-carrier resistance can be distinguished [5]: (a) smaller electric fields for identical bias conditions, (b) a smaller amount of physical damage for a given lateral electric field and (c) a smaller impact of a given amount of damage on the I-V characteristics.

Regarding to the first contribution (a), the fact that for a fixed bias condition the relation of substrate to drain current ($I_{sub}/I_d \equiv$multiplication factor) is higher for the LDD devices is indicative of the existence of a higher value for the maximum lateral electric field near the drain junction for these transistors [1]:

$$\frac{I_{sub}}{I_d} \approx C \cdot e^{-\phi_i / q\lambda E_m}$$

Being C a weak function of E_m and device parameters [1], λ the hot-electron mean-free path and ϕ_i the minimum energy that a hot electron must have in order to create an impact ionisation event.

In this way, the fact that for a given amount of hot-carrier-induced impact-ionisation events (I_{sub}) LDD devices exhibit shorter lifetimes (Fig. 5) is interpreted as being the result of the higher electric field, resulting in a more important generation of damage. Nevertheless, (b) and (c) contributions should be also evaluated.

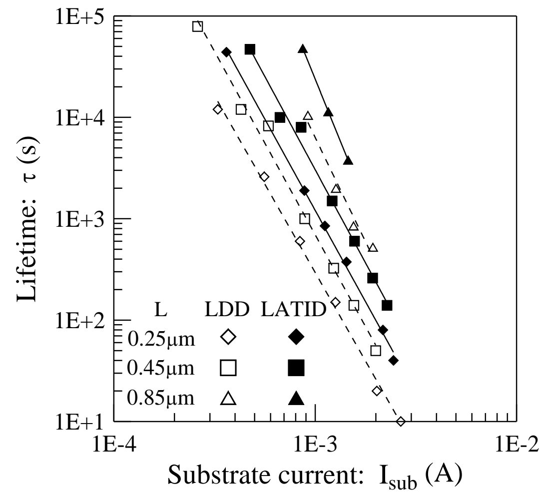

Fig. 5. Lifetime vs. substrate current plot for LDD and LATID devices of different gate lengths.

In this respect, the amount of charge flowing through the channel for a given electric field gives an indication of how prone is the device to the generation of physical damage. Since the product $\tau \cdot I_d$ is related to the charge flow and the ratio I_{sub}/I_d

to the lateral electric field, in Fig. 6 a comparison of the obtained results is plotted. As shown in this figure, no significant difference between the two types of devices is registered, indicating the same generation of physical damage for a given electric field.

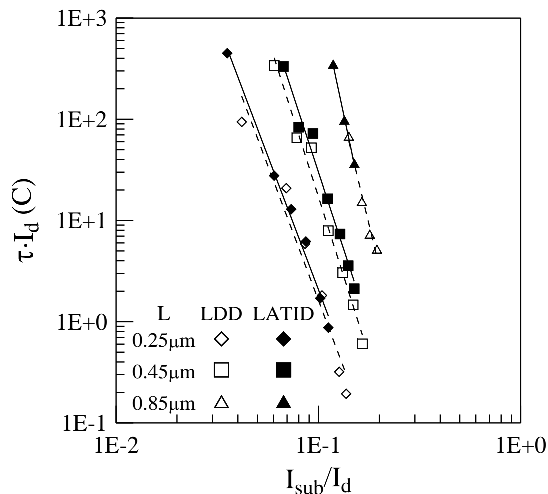

Fig. 6. $\tau \cdot I_d$ vs. I_{sub}/I_d plot for the results corresponding to the LDD and LATID stressed devices of Fig. 5.

Finally, in order to evaluate the susceptibility of I-V characteristics to a determined amount of generated damage, I_{dlin} degradation results were plotted against their corresponding charge pumping current increase values in Fig. 7.

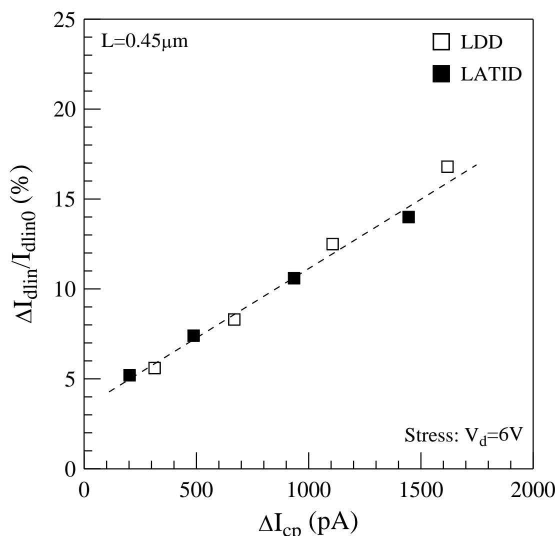

Fig. 7. I_{dlin} degradation vs. charge pumping current increase plot for L=0.45μm LDD and LATID stressed devices.

In this way, the existence of a linear relationship between $\Delta I_{dlin}/I_{dlin0}$ and interface state generation (ΔI_{cp}) is interpreted as a clear proof that device degradation is mainly determined by the total amount of interface states and that there is no different degree of susceptibility to the generated damage between the two different studied architectures.

4. Conclusions

In view of the obtained results, we can conclude that the improved hot-carrier reliability registered by LATID with respect to LDD devices is mainly achieved because of a reduction of the maximum lateral electric field along the channel, but not to a minor generation of physical damage for a given electric field or to a reduced I-V susceptibility to a given amount of generated damage.

Acknowledgements

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