**Impact of Gate Tunneling Floating Body Charging
on Drain Current Transients of
0.10 μm -CMOS Partially Depleted SOI MOSFETs**

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Abstract

In this paper, the impact of majority carriers introduced into the film by gate-body Electron Valence Band (EVB) tunneling in ultrathin gate oxide (2.5 nm) PD SOI MOSFETs is studied by analyzing “switch-off” drain current (I_d) transients measured with different front gate voltage steps and drain bias (V_d) conditions.

A change in the I_d transients shape from undershoot to overshoot is appreciated at low V_d for sufficiently high “on” gate voltages, which enable gate-body EVB tunneling to introduce majority carriers into the film. The shape and the transition time of these EVB-induced I_d overshoots have been found to be in good agreement with conventional (EVB-free) “switch-on”-type transients, which enable the extraction of the majority carrier recombination lifetime. It has been found that the magnitude of the EVB-induced I_d overshoot decreases with increasing V_d , finally resulting in an undershoot for sufficiently high V_d . In order to characterize the effect of the charges introduced into the film during the different “switch-off” conditions, an effective gate voltage overdrive (ΔV_{geff}) has been defined and extracted for all I_d transients. It has been found that the transition from overshoot to undershoot can be explained by means of a body potential increase associated with the high V_d condition, which results in a lower gate-to-film voltage drop and a reduced EVB majority carriers injection into the film.

1. Introduction

Owing to device integration requirements and intrinsic resistance constraints, no film contacts are generally provided in advanced Silicon On Insulator (SOI) technologies. If body contacts are not present, so-called Floating-Body Effects (FBEs) arise, especially in Partially Depleted (PD) SOI MOSFETs, leading to some detrimental effects on device performance [1]. Among them, a “kink” or excess of drain current due to impact ionization is well known to occur for sufficiently high drain voltages (V_d), in which majority carriers are injected into the film, lowering the threshold voltage (V_{th}) of the MOSFETs. Moreover, after switching “on” or “off” the front gate, there is no substrate current to quickly adjust the majority carrier density and equilibrium has to be reached through generation and recombination processes. Since early times, it is known that drain current (I_d) transients are observed under these conditions [2] and their potential impact on circuit performance has been a matter of concern [3]. Originating from generation and recombination processes, I_d transients can be also a valuable tool for assessing the quality of the starting material, process-induced defects or contamination. Different techniques have been proposed to extract the generation or recombination lifetimes from “switch-off” or “switch-on” I_d transients, respectively [4-8]. Furthermore, recently some interesting potential applications of the FBEs have been also suggested [9].

With the aggressive shrinking of gate oxide thickness (t_{ox}), a new type of FBEs associated with gate-body direct tunneling has been identified in linear operation (low V_d) of SOI n- and p-channel MOSFETs. They have a similar influence on device and circuit operation as the classical impact ionization related “kink” effect. The main difference is that for ultra-thin gate oxides (t_{ox} as thin as 2-2.5 nm), Electron Valence Band (EVB) tunneling, occurring for a

sufficiently large front gate voltage (V_g) [10-12] supplies the necessary majority carriers to charge the film and forward bias the source-body junction, inducing a “kink” on the linear I_d - V_g characteristics and a second peak in the derived transconductance [13-17]. Associated with this effect, an increase of the low-frequency noise [18,19] and a change of I_d transients shape [13,20] have been also reported. The presence of these Gate-Induced FBEs (GIFBEs) [13], leading to history and memory effects, could be an important limitation for PD SOI CMOS circuits operation.

In this contribution, the impact of majority carriers introduced into the film by EVB tunneling in ultrathin gate oxide PD SOI MOSFETs is analyzed by means of “switch-off” I_d transients performed with different V_g steps and V_d conditions. The shape of the EVB-induced I_d overshoot is found to be in good agreement with “switch-on”-type transients, which enable the extraction of the majority carrier recombination lifetime. The magnitude of the EVB-induced I_d overshoot is found to decrease with increasing V_d , finally resulting in an undershoot for sufficiently high V_d .

In order to characterize the effect of the charges introduced into the film during the different “switch-off” conditions, an effective gate voltage overdrive (ΔV_{geff}) is defined and extracted for all I_d transients. It is found that the transition from overshoot to undershoot can be explained by means of a film potential increase associated with the high V_d condition, which results in a lower gate-to-film voltage drop and a reduced EVB majority carriers injection into the film.

2. Devices and experimental details

The PD SOI MOSFETs used in this study were fabricated in a 0.1 μm -CMOS process using a PELOX isolation scheme, a 2.5 nm Nitrided gate Oxide (NO), a 150 nm polysilicon gate and 80 nm nitride spacers. Processing was performed on 200 mm diameter UNIBOND wafers, resulting in a final film thickness of 100 nm. The buried oxide thickness was 400 nm. The devices received a halo implantation, in order to control the short channel effects (SCE). To investigate its impact on the I_d transients, MOSFETs without halo (abbreviated No Halo) were also included in the study. The latter show more pronounced SCE for V_{th} .

The test structures have common gate and source configuration with separate drain pads. There is no film contact. N- and p-channel transistors with gate lengths (L) and widths (W) ranging from 0.08 to 10 μm and 0.3 to 10 μm , respectively, were studied for this work. However, in order to avoid short and narrow device geometry effects on I_d transients, only results from long ($L = 10 \mu\text{m}$) and wide ($W = 10 \mu\text{m}$) transistors are reported in this contribution. Moreover, the results shown in this work focus on the n-channel devices, but similar results were found for their p-channel counterparts.

All I_d transients were measured using an HP-4156 Parameter Analyzer. During a conventional “switch-off” experiment, the front gate is switched at $t = 0$ s from an ‘on’ gate bias (V_{gon}) above V_{th} to an ‘off’ gate bias (V_{goff}) in weak inversion. The back gate was grounded for all measurements. Care was taken for the duration of the bias ‘on’ level, as well as for the conditions between two transient measurements, so that there were no device history

(memory) effects. All experiments were carried out in a controlled temperature room with a light-proof and electrically shielded probe station.

3. “Switch-off” I_d transients: Depletion charges and EVB-introduced charges

In the case of an NMOSFET where the gate is switched from above to below V_{th} , holes have to be generated to replenish the space-charge region between the maximum depletion width (x_{dmax}) corresponding to the V_{gon} bias and the steady-state depletion width ($x_{d\infty}$) associated to the V_{goff} condition (Fig. 1(a)). At low V_d , these holes can be supplied by four main mechanisms: bulk generation in the space charge region, source/drain to film space-charge regions, and generation at front and back interfaces [21,22]. In the case of long- and wide-channel PD SOI devices subjected to low V_d , bulk generation in the space charge region can be regarded as the dominating mechanism and the carrier generation lifetime can be estimated from the measured I_d transient time [21-23]. Thus, I_d transients can be a valuable tool for assessing the quality of the SOI material, process-induced defects or contamination.

Figure 2 shows the measured I_d transients normalized to the steady-state current level ($I_d(t=\infty)$) for an $L=W=10\text{ }\mu\text{m}$ NMOSFET after “switching-off” its front gate from V_{gon} values ranging from 0.1 V to 1.5 V to a fixed $V_{goff}=0.1\text{ V}$. From the figure, for V_{gon} values up to the threshold voltage of this long channel device ($V_{th}=0.35\text{ V}$) an I_d undershoot arises. In this way, I_d is significantly suppressed immediately after the negative V_g step and it gradually increases towards the steady-state value with time. The magnitude of the transients increases with higher negative gate voltage steps due to the difference in depletion charge between the two bias conditions and the floating body nature of the device.

For V_{gon} values between 0.4 V and 1 V the inversion channel is already created and no significant changes in x_{dmax} are introduced by the different V_{gon} conditions, resulting in similar I_{d} transients for all those V_{gon} values.

However, for $V_{\text{gon}} > 1.1$ V a change in the shape of Fig. 2 transients is clearly appreciated. Under this situation, released holes associated with EVB tunneling from the film to the gate are introduced into the film. The accumulation of these positive charges in the film (Fig. 1(b)) raises the film to source potential (V_{bs}), being responsible for a *body-effect* reduction of V_{th} and a second peak in the transconductance (G_{m}) versus V_{g} characteristics [13,17]. The introduced positive charges at $V_{\text{gon}} > 1.1$ V conditions are also responsible for a reduction of x_{dmax} in comparison to the one that would correspond to the case in which no EVB tunneling was present. If x_{dmax} corresponding to V_{gon} is smaller than $x_{\text{d}\infty}$ corresponding to V_{goff} , an I_{d} overshoot transient is measured.

To validate the above hypothesis, the shape of the I_{d} overshoot has been found to be in good agreement with a “switch-on”-type transient, in which the gate is pulsed from a V_{goff} to a V_{gon} condition (Fig. 3). Under this situation, the V_{goff} step is responsible for generating a shallow depletion region, which spreads with time towards its steady-state width corresponding to V_{gon} as holes recombine in the film. These “switch-on” transients enable the extraction of the hole recombination lifetime [8].

As previous results reported in the literature for similar experimental conditions and conventional “switch-off” and “switch-on” experiments [24], the transients associated with a

recombination process ($|V_{\text{gon}}| > 1.1 \text{ V}$) are found to be significantly faster than the ones originated from a generation process ($|V_{\text{gon}}| < 1 \text{ V}$) (Fig. 2).

4. “Switch-off” I_d transients: Effective gate voltage overdrive (ΔV_{geff})

In order to characterize the impact of the charges introduced into the film by the EVB tunneling mechanism, “switch-off” I_d transients were measured with different V_g steps and V_d conditions. It was expected that by applying a sweep on the V_{gon} and V_{goff} conditions it could be possible to evaluate the relative magnitude of the involved film charges. Moreover, extending the transient studies to higher V_d values is interesting to understand the EVB-induced second peak of the G_m - V_g curves, being less pronounced in I_d - V_g characteristics measured at higher V_d conditions.

Taking from the I_d - V_g characteristics measured at different V_d the subthreshold (eq. (1)) or the linear or saturation conduction (eq. (2)) in the vicinity of the V_g corresponding to the final level of the gate pulse (V_{goff}), an effective gate voltage overdrive (ΔV_{geff}) has been defined as the effective V_g shift that would be responsible for the measured I_d excursion in comparison with the steady-state drain current level ($I_d(t=\infty)$) (Fig. 2):

$$\text{Subthreshold region: } \Delta V_{\text{geff}} \equiv SS \cdot \text{Log}_{10} \left(\frac{I_d(t=0)}{I_d(t=\infty)} \right) \quad SS \equiv \left(\left[\frac{d(\text{Log}_{10} I_d)}{dV_g} \right]_{V_{\text{glow}}} \right)^{-1} \quad (1)$$

$$\text{Linear or saturation region: } \Delta V_{\text{geff}} \equiv \frac{I_d(t=0) - I_d(t=\infty)}{\left[\frac{dI_d}{dV_g} \right]_{V_{\text{glow}}}} \quad (2)$$

Following this approach, Fig. 4 shows the extracted ΔV_{geff} values for different “switch-off” transients measured on n- and p-channel MOSFETs with and without halo drain architecture. The existence of two regions, one corresponding to the excess depletion charges ($\Delta V_{\text{geff}} < 0$ for NMOSFETs and $\Delta V_{\text{geff}} > 0$ for PMOSFETs) and another one dominated by the EVB released charges ($\Delta V_{\text{geff}} > 0$ for NMOSFETs and $\Delta V_{\text{geff}} < 0$ for PMOSFETs) is clearly evident. In this way, ΔV_{geff} values corresponding to undershoot-like I_d transients are obtained for $|V_{\text{gon}}|$ values up to around 1 V, where the EVB-introduced majority carriers start to be appreciable and, finally, lead to overshoot-like I_d transients for $|V_{\text{gon}}| > 1.1$ V conditions, associated with a change of sign in ΔV_{geff} .

5. “Switch-off” I_d transients: EVB-introduced charges and V_d dependence

The potential of the floating body of a PD SOI device (V_{bs}) in steady-state conditions is dictated by the film charges and boundary conditions [25]. In the case of an NMOSFET, four main contributions are expected to introduce or release majority carriers into the body (I_{in} in eq. (3)): impact ionization (I_{impact}), EVB-released holes (I_{EVB}), reverse junction leakage (I_{leakage}) and gate induced drain leakage (I_{GIDL}):

$$I_{\text{in}} = I_{\text{impact}}(V_{\text{ds}}, V_{\text{gs}}) + I_{\text{EVB}}(V_{\text{gb}}) + I_{\text{leakage}}(V_{\text{db}}) + I_{\text{GIDL}}(V_{\text{gd}}) \quad (3)$$

with $V_{ds} \equiv V_d - V_s$, $V_{gs} \equiv V_g - V_s$, $V_{gb} \equiv V_g - V_b$, $V_{db} \equiv V_d - V_b$, $V_{gd} \equiv V_g - V_d$.

For the studied experimental conditions and from measurements on bulk n-channel devices corresponding to the same process (allowing substrate current measurements), I_{GIDL} is only observed for negative V_g values. On the other hand, for V_d higher than about 1.1 V a substrate current associated with impact ionization starts to be measurable. However, sub-bandgap impact ionization and its effects on I_d transients has been reported for V_{ds} values down to 0.75 V [26-28].

Under eq. (3) situations, the body to source potential (V_{bs}) rises and the source junction becomes slightly forward biased. Equilibrium is reached when the number of introduced holes (I_{in}) equals the number leaving at the body-source junction (I_{out}), which, in first approximation, can be modeled by [25]:

$$I_{out} = W_{eff} \cdot (t_{Si} - x_d) \cdot J_0 \cdot \left(e^{\frac{qV_{bs}}{nKT}} - 1 \right) = I_0 \left(e^{\frac{qV_{bs}}{nKT}} - 1 \right) \quad (4)$$

where W_{eff} is the effective body-source junction width, t_{Si} the silicon film thickness, x_d the channel depletion width near the source, J_0 the reverse saturation current density (dependent on film minority carrier concentration), I_0 the reverse saturation current and n the junction ideality factor.

In order to distinguish between the effects caused by the conventional “switch-off” depletion charges and the majority carriers released into the film by the EVB tunneling at a high $|V_g|$

condition, “switch-off” I_d transients from $|V_{gon}| = 1.5$ V to various $|V_{goff}|$ values were performed at different V_d conditions. In this way, Fig. 5 shows the normalized I_d transients measured at different V_d values for an $L=W=10$ μm NMOSFET after “switching-off” its front gate from $V_{gon} = 1.5$ V to $V_{goff} = 0.1$ V. From the figure, the magnitude of the EVB-induced overshoot is found to decrease for $V_d \geq 200$ mV. In this way, the shape of the transients becomes nearly flat for $V_d \approx 450$ mV and finally results in an undershoot for sufficiently high V_d .

In order to investigate this phenomenon, different V_{goff} values were used and the results are given in Figs 6 and 7. From the figures, for all V_{goff} cases, the EVB-induced I_d overshoot ($I_d(t=0) > I_d(t=\infty)$, i.e. $\Delta V_{geff} > 0$) is only observed for low V_d values. In this way, the results from the V_d study carried out in both, n- and p-channel MOSFETs, have revealed the existence of a critical V_d value ($V_{d_ \Delta V_{geff}=0}$), increasing with V_{goff} , for which the transient shape changes from the EVB-induced I_d overshoot to an undershoot ($\Delta V_{geff} < 0$ cases in Fig. 7). These results indicate that for low V_d conditions the reduced x_{dmax} , because of the positive charges released during the $V_{gon} = 1.5$ V condition, is smaller than the $x_{d\infty}$ associated with the different V_{goff} cases studied.

Furthermore, from Figs 6 and 7, it is observed that for low V_d conditions ($V_d < 200$ mV) the magnitude of the positive ΔV_{geff} increases with V_{goff} values below V_{th} ($V_{goff} = 0.1$ V to 0.4 V), for which the depletion region increases. On the other hand, no significant differences in ΔV_{geff} are observed for V_{goff} values above V_{th} ($V_{goff} = 0.4$ V to 0.9 V), among which no significant changes in the depletion region are expected between these V_{goff} conditions.

In order to support the above interpretation of Fig. 7 results, the estimated space charge widths (x_d) corresponding to $V_g = 0.1, 0.2$ and 0.4 V conditions were extracted from C-V measurements on MOS capacitors fabricated with the same process but on bulk wafers (allowing C-V measurements). From the x_d values, the corresponding V_{bs} differences (ΔV_{bs}) associated with the difference in x_d between the three V_g conditions were calculated according to eq. (5) [22]:

$$\Delta V_{bs} = -\frac{qN_a}{2\epsilon_{Si}}(x_{d1}^2 - x_{d2}^2) \quad (5)$$

with N_a an estimated average uniform doping concentration ($5.5 \cdot 10^{17} \text{ cm}^{-3}$) and ϵ_{Si} the silicon permittivity.

The impact of ΔV_{bs} on V_g was then calculated following eq. (6) [29]:

$$\Delta V_g = -\frac{\Delta V_{bs} \cdot C_d}{C_{ox}} \quad (6)$$

with C_d and C_{ox} the space-charge region and oxide capacitances per unit area, respectively.

Table 1 shows the results obtained for the ΔV_g (from eq. (6)) associated with the difference in x_d between the three V_g conditions. A reasonable agreement is found with the difference in ΔV_{geff} values between $V_{goff} = 0.1, 0.2$ and 0.4 V curves in the low V_d region ($V_d < 200$ mV) of Fig. 7.

For intermediate V_d voltages in Fig. 7 ($250 \text{ mV} < V_d < 700 \text{ mV}$), the I_d overshoot ($\Delta V_{\text{geff}} > 0$) associated with the positive charges released into the film under the $V_{\text{gon}} = 1.5 \text{ V}$ condition is found to monotonously decrease with V_d , however, $\Delta V_{\text{geff}} > 0$ I_d transients are found to survive up to higher V_d according to the different V_{goff} conditions. From Fig. 7 results, the critical V_d value for which the transients shape changes from the EVB-induced I_d overshoot to an undershoot ($V_{d_ \Delta V_{\text{geff}}=0}$) has been found to be correlated with the drain saturation bias ($V_{\text{dsat}} \approx V_g - V_{\text{th}}$), giving in first approximation the following relationship:

$$V_{d_ \Delta V_{\text{geff}}=0} \approx V_{\text{dsat}} + 0.75 \text{ V} \approx V_g - V_{\text{th}} + 0.75 \text{ V} \quad (7)$$

$\Delta V_{\text{geff}} < 0$ values corresponding to undershoot-type I_d transients are obtained for all V_{goff} conditions at sufficiently high V_d voltages. This behavior bears some resemblance to a similar change in shape from overshoot to undershoot observed for classical “switch-on” transients, where the change to an undershoot is explained in terms of a trigger of an impact ionization enhancement of I_d after switching on the device [30,31]. The latter phenomenon has been observed for V_d voltages down to sub-bandgap values around 0.75 V [26]. Furthermore, the effect of impact ionization on I_d “switch-on” transients has been used as a very sensitive technique to measure the substrate current down to the sub-bandgap regime [27].

Finally, it should be commented that for V_d voltages higher than about 1.1 V , where substrate current associated with impact ionization starts to be measurable on bulk n-channel devices corresponding to the same process, the transients become too fast to be properly measured with a parameter analyzer [31].

6. “Switch-off” I_d transients between $V_g = 1.5$ V, 0.7 V and 0.1 V conditions

An additional attempt to evaluate the effects associated with the positive charges introduced by the EVB tunneling and the “switch-off” excess depletion charges is shown in Fig. 8, corresponding to the ΔV_{bs} (calculated by means of eq. (6)) vs. V_d analysis of three different “switch-off” conditions. It was expected that the ΔV_{bs} associated to the recombination of holes on $V_{gon} = 1.5$ V to $V_{goff} = 0.1$ V “switch-off” conditions could be derived from the recombination of holes under $V_{gon} = 1.5$ V to $V_{goff} = 0.7$ V conditions and their generation in the $V_{gon} = 0.7$ V to $V_{goff} = 0.1$ V case.

From Fig. 8, the results corresponding to the switch-off conventional transients ($V_{gon} = 0.7$ V to $V_{goff} = 0.1$ V) show a more or less constant level of ΔV_{geff} for V_d up to around 0.8 V, where the impact ionization phenomenon is expected to introduce positive charges into the film, drastically reducing the magnitude and transition times of the transients. This level of ΔV_{geff} should be associated with the depletion charges difference between $V_{gon} = 0.7$ V and $V_{goff} = 0.1$ V conditions. Moreover, the small V_{bs} increase registered for V_d values up to about 0.35 V may be associated with the fact that for those conditions the device is still in linear regime under the $V_{gon} = 0.7$ V condition, whereas for $V_{goff} = 0.1$ V it is already in saturation, with a supposed higher V_{bs} due to drain leakage current (eq. (3)).

Taking the $V_{gon} = 1.5$ V to $V_{goff} = 0.7$ V and $V_{gon} = 0.7$ V to $V_{goff} = 0.1$ V curves of Fig. 9, an attempt to approximate the $V_{gon} = 1.5$ V to $V_{goff} = 0.1$ V curve was done. In this way, it was expected that subtracting the number of holes that have to be recombined to go from $V_{gon} = 1.5$ V condition to $V_{goff} = 0.7$ V from the corresponding to go from $V_{gon} = 1.5$ V to $V_{goff} = 0.1$ V

should give the contribution associated with the excess depletion charges between $V_g = 0.7$ V and $V_g = 0.1$ V conditions. The results found show some disagreement with the above hypothesis in all the V_d region up to 0.6 V (Fig. 8). So, a second-order analysis or interpretation of the phenomena could still be needed.

7. “Switch-off” I_d transients: V_d modeling approach

In order to explain the results shown in Figs 5 to 8, indicating that the introduction of EVB-holes decreases for higher V_d values, it was envisaged that the drain to body junction leakage current could play a determinant role in increasing the film potential at high V_d conditions, which would limit the EVB gate-body tunneling injection.

Opposite to what happens in the case of the conventional body effect, in which the substrate to source junction is biased in reverse, leading to an increased V_{th} , the V_{bs} originated by the majority carriers introduced by the drain leakage current at high V_d conditions is expected to be responsible for a split of the quasifermi potentials in a way that less voltage drop in the semiconductor is needed to get a same level of channel conduction (Figs 9(a) and (b)).

In order to evaluate this possibility, V_{th} values were extracted from I_d - V_g characteristics measured at different V_d conditions, the results are shown in Fig. 10. From the V_{th} shift, and using the body factor given by eq. (6), the estimated value of V_{bs} that would be responsible for the measured V_{th} lowering was calculated as a function of V_d (Fig. 10). Finally, the estimated V_{bs} vs. V_d values were used to model the measured ΔV_{geff} values obtained from different “switch-off” transients sweeping on different V_{gon} , V_{goff} and V_d conditions.

Following Fig. 9 sketch for the silicon energy band diagram, under high V_d conditions giving rise to a non-negligible V_{bs} (Fig. 9(b)), there is no need for a deep depletion region, because a V_{bs} voltage drop is already accommodated by the split of the quasifermi potentials. So, the depletion width (x_d) associated to a given gate voltage (V_g) can be approximated by the one that would exist at $V_g - V_{bs}$ gate voltage when $V_{bs} = 0$.

Making the first-order assumption of a fixed V_{bs} value for a given V_d value, regardless of the different V_{gon} and V_{goff} conditions, the “switch-off” transients at high V_d conditions can be estimated from the ones observed at low V_d values by considering that they are performed between $V_{gon} - V_{bs}$ and $V_{goff} - V_{bs}$ levels (Figs 11 and 12). The subtraction of the film potential V_{bs} is also very important for the EVB mechanism, because the gate-to-film voltage drop is reduced and, consequently, also the EVB majority carriers injection into the film.

From Figs 11 and 12 results, showing a reasonable trend between the measured and the modeled I_d transients results it may be concluded that the increase in V_{bs} with increasing V_d plays a dominant role on the transients behavior and on the reduction of the EVB introduced charges into the film.

Note that in case of high V_d , because of the vertical electric field reduction near the drain, the EVB charge injection could not take place in the whole channel, but mainly near the source region. However, the extent of this region with reduced EVB injection is not expected to be relevant in the case of long channel devices, specially under the high V_{gon} conditions giving rise to the EVB tunneling injection, which in its turn further increase the saturation condition ($V_d > V_g - V_{th}$) due to the EVB-induced V_{th} lowering

Although EVB tunneling current in ultrathin gate oxide PD SOI CMOS devices can be a limitation for common gate circuits like amplifiers or memories that are sensitive to the device history, recently, it has been reported that gate-to-body tunneling currents can also provide some benefits at circuit level [32]. However, the significance of these effects is expected to diminish in scaled PD SOI CMOS circuits because of the reduced power supply [32] and/or the introduction of alternative gate dielectrics.

8. Conclusions

The impact of the majority carriers introduced into the film by electron valence band (EVB) tunneling in ultrathin gate oxide PD SOI MOSFETs has been analyzed by performing “switch-off” drain current (I_d) transients with different gate voltage steps and drain bias (V_d) conditions. The shape of the EVB-induced I_d overshoots has been found to be in good agreement with “switch-on”-type transients, which enable the extraction of the majority carriers recombination lifetime. The magnitude of the EVB-induced I_d overshoot has been found to decrease with increasing V_d , finally resulting in an undershoot for sufficiently high V_d .

In order to characterize the effect of the charges introduced into the film during the different “switch-off” conditions, an effective gate voltage overdrive (ΔV_{geff}) has been extracted for all I_d transients. It has been found that the transition from overshoot- to undershoot-type I_d transients can be explained by means of the body film potential increase associated with the

high V_d condition, which results in a reduced gate-to-film voltage drop and EVB majority carriers injection into the film.

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FIGURE CAPTIONS

- Fig. 1:** Sketch of a PD-SOI NMOSFET in a “switch-off” gate pulse experiment at low V_d . (a) With $V_{th} < V_{gon} < \sim 1.1$ V. x_{dmax} and $x_{d\infty}$ represent the maximum (V_{gon}) and steady state (V_{goff}) space charge widths, respectively. (b) In the case of $V_{gon} > \sim 1.1$ V, electron valence band tunneling into the gate is responsible for positive charging of the semiconductor film (release of holes).
- Fig. 2:** Normalised I_d “switch-off” transients from different V_{gon} values to $V_{goff} = 0.1$ V measured for an $L=W= 10$ μm NMOSFET at $V_d = 25$ mV. ($I_d(t=\infty)$ = steady state I_d current level at $V_{goff} = 0.1$ V).
- Fig. 3:** Comparison between an I_d “switch-off” transient from $V_{gon} = 1.5$ V to $V_{goff} = 0.7$ V and an I_d “switch-on” transient from $V_{goff} = 0.1$ V to $V_{gon} = 0.7$ V, measured for an $L=W= 10$ μm NMOSFET at $V_d = 25$ mV. ($I_d(t=\infty)$ = steady state drain current level at $V_g = 0.7$ V).
- Fig. 4:** Extracted effective gate voltage overdrive (ΔV_{geff}) as a function of V_{gon} for different V_{gon} to V_{goff} “switch-off” transients measured at $|V_d| = 25$ mV on $L=W= 10$ μm n- and p-channel MOSFETs, some of them without Halo drain architecture.
- Fig. 5:** Normalised I_d “switch-off” transients from $V_{gon} = 1.5$ V to $V_{goff} = 0.1$ V measured at different drain biases (V_d) for an $L=W= 10$ μm NMOSFET.
- Fig. 6:** $I_d(t=0)$ and $I_d(t=\infty)$ values for “switch-off” transients from $V_{gon}=1.5$ V to different V_{goff} values as a function of V_d , measured for an $L=W= 10$ μm NMOSFET.

- Fig. 7:** Extracted effective gate voltage overdrive values (ΔV_{geff}) corresponding to Fig. 7 data.
- Fig. 8:** Extracted body to source effective potential increase ΔV_{bs} (from eq. (6)) as a function of V_d for I_d transients from $V_{\text{gon}} = 1.5 \text{ V}$ to $V_{\text{goff}} = 0.7 \text{ V}$, $V_{\text{gon}} = 1.5 \text{ V}$ to $V_{\text{goff}} = 0.1 \text{ V}$ and $V_{\text{gon}} = 0.7 \text{ V}$ to $V_{\text{goff}} = 0.1 \text{ V}$, measured for an $L=W=10 \text{ }\mu\text{m}$ NMOSFET. (Empty squares curve correspond to subtracting filled circles from filled triangles data).
- Fig. 9:** Sketch of the silicon energy band diagram corresponding to the onset of weak inversion regime when (a) $V_{\text{bs}}=0$ and (b) $V_{\text{bs}}>0$.
- Fig. 10:** Extracted V_{th} for an $L=W=10 \text{ }\mu\text{m}$ NMOSFET (defined at a fixed current level of $I_d = 5 \cdot 10^{10} \text{ A}$) as a function of V_d and corresponding calculated *body effect* film potential (V_{bs}) (from eq. (6)).
- Fig. 11:** Effective gate voltage overdrive (ΔV_{geff}) for I_d “switch-off” transients from $V_{\text{gon}} = 1.5 \text{ V}$ to different V_{goff} values. (a) Measured at different V_d on an $L=W=10 \text{ }\mu\text{m}$ NMOSFET. (b) Calculated for different V_d voltages according to the proposed model and $V_d = 25 \text{ mV}$ data.
- Fig. 12:** Effective gate voltage overdrive (ΔV_{geff}) for I_d “switch-off” transients from different V_{gon} values to $V_{\text{goff}} = 0.1 \text{ V}$. (a) Measured at different V_d on an $L=W=10 \text{ }\mu\text{m}$ NMOSFET. (b) Calculated for different V_d voltages according to the proposed model and $V_d = 25 \text{ mV}$ data.

TABLE CAPTIONS

Table 1: Estimated values for ΔV_{bs} and ΔV_g (according to eqs. (5) and (6), respectively) associated with the difference in space charge widths (x_d) between $V_g = 0.1, 0.2$ and 0.4 V conditions.

Fig. 1(a)

Fig. 1(b)

Fig. 2

Fig. 3

Fig. 4

Fig. 5

Fig. 6

Fig. 7

Fig. 8

Fig. 9

Fig. 10

Fig. 11

(a)

(b)

Fig. 12

V_g (V)	x_d (nm)	ΔV_{bs} (mV)	ΔV_g (mV)
0.1	42.1	-76	16
0.2	44.2		
0.2	44.2	-120	24
0.4	47.3		

Table 1