Impact of Hot-Carrier Stress on Gate-Induced Floating Body Effects and Drain Current Transients of Thin-Gate-Oxide Partially Depleted SOI nMOSFETs

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Abstract

The impact of hot-carrier (HC) stress on thin gate oxide PD SOI nMOSFETs is investigated by analyzing the front and back channel current-voltage characteristics and the switch-off drain current transients.

A particular hot-carrier degradation mode, characterized by a turn-around behavior for front gate threshold voltage degradation, is analyzed for devices with different geometries, bias conditions and source/drain architecture. A significant positive back gate threshold voltage shift is also observed after long HC stress. The maximum hot-carrier degradation (HCD) is obtained for the highest front gate biases, corresponding to the conditions of maximum electron valence band injection of majority carriers into the floating body. The presence of the HCD is found to reduce both the generation and the recombination switch-off drain current transient times. Unbiased thermal annealing in the range of 200°C to 250°C significantly reduces the hot-carrier induced damage affecting the back channel characteristics.

Whereas front gate direct tunnel stress is not causing any significant degradation for stress biases up to about two times the power supply for this technology node and reasonably short stress times, for the highest stress conditions the drain current transients are found to be progressively faster till front gate dielectric breakdown occurs.

1. Introduction

In recent years, silicon on insulator (SOI) technologies have emerged as a serious competitor to bulk silicon technology. Owing to device integration requirements and intrinsic resistance constraints of the thin film layers, no film contacts are generally supplied in advanced SOI technologies. If the body is not grounded, so-called floating body effects (FBEs) arise, especially in partially depleted (PD) SOI MOSFETs, leading to some detrimental effects on device performance [1].

In particular, after switching “on” or “off” the front gate, there is no substrate current to quickly adjust the majority carrier density and equilibrium has to be reached through generation-recombination processes. Under these conditions, drain current (I_D) transients are observed [1-3], and, originating from generation and recombination processes, these can be a useful tool for assessing the quality of the starting material, process-induced defects or contamination.

With the marked decrease in front-gate-oxide thickness, a new type of FBEs associated with gate-body direct tunnelling have been identified in linear operation (low drain voltage (V_D)) of SOI n- and p-channel MOSFETs [4,5]. They have a similar influence on device and circuit operation as the classical impact ionization related “kink” effect. The main difference is that for thin gate oxides (as thin as 2-2.5 nm), electron valence band (EVB) tunnelling, occurring for a sufficiently large front-gate voltage (V_{FG}) [6] supplies majority carriers that charge the film and forward-bias the source-body junction, inducing a “kink” in the linear I_D - V_{FG} characteristics and a second peak in the

derived front gate transconductance (g_{mf}) [4,5]. Associated with this effect, a change in the I_D transients shape [4,5,7] and an increase of the low-frequency noise [8,9] are also observed. The presence of these gate-induced FBEs (GIFBEs) [4] leading to history and memory effects, could be a limitation for PD SOI CMOS circuit operation [10].

The problems associated with hot carriers (HC) have been recognised as one of the major constraints in silicon MOS scaling. Hot carriers are generated by the high lateral electric fields near the drain MOSFETs junction and may attain enough energy to overcome the Si-SiO₂ barrier, causing damage in this region, which leads to a gradual degradation of transistors current-voltage characteristics [11,12]. The damage is commonly believed to result in charge trapping in the gate dielectric and interface-state generation at the Si/dielectric interface.

In spite of the fact that FB SOI MOSFETs have been considered to be more resistant to HC degradation (HCD) than their bulk counterparts, what has been mainly attributed to a lower channel electric field [13], the presence of two different gates and their corresponding different interfaces makes HCD in SOI MOSFETs a more complex subject. In particular, opposite channel injection phenomena may occur [14,15], and, with the reduction in film thickness and fully depleted (FD) operation [16], coupling effects between the damage generated at the different gates [17,18].

Moreover, the traditional worst-case gate bias regime for HCD corresponding to maximum substrate current condition in bulk and long nMOSFETs [11] may be replaced by different gate voltage regimes in the case of FB devices, where the impact

of the body potential on HCD can play an important role [19,20]. In particular, high HCD rates have been reported for low gate bias conditions, where the effects of parasitic bipolar action may lead to enhanced HC degradation [21,22].

More recently, with the introduction of very thin (below around 2.5 nm) SiO₂-based gate oxides, the high gate bias regimes have been shown to suffer from enhanced HCD [23-25], what has been attributed to the impact of the EVB direct tunneling injection phenomena, where the majority carriers introduced into the floating film have been reported to be responsible for this enhanced HCD [26,27].

In this contribution, the impact of constant voltage hot-carrier stress on thin gate oxide PD SOI nMOSFETs is investigated by analyzing the front and back channel current-voltage characteristics and the front gate switch-off I_D transients. A particular hot-carrier degradation mode characterized by an initial positive front gate threshold voltage shift with a turn-around behavior for longer HC stress is analyzed for devices with different geometries, bias conditions and source/drain architecture. A significant positive back gate threshold voltage shift is also found after long HC stress.

For the studied experimental conditions, the maximum HCD is observed for the highest V_{FG} stress regimes ($V_{FG} \approx V_D$), corresponding to the conditions of maximum EVB injection of majority carriers into the floating body. The presence of the HCD is found to reduce the switch-off transient times for V_{FG} above and below the V_{FG} threshold for body to gate EVB tunneling, whereas the steady-state I_D levels ($I_D(t=\infty)$) are found to

consistently evolve according to the registered front gate threshold voltage (V_{Tf}) degradation.

In addition, some measurements were repeated a few weeks after hot-carrier stress to check any possible unbiased room temperature annealing effects of the HC damage and some sample was subjected to constant temperature annealing in the range of 140 °C to 250 °C. It has been observed that the HCD is significantly reduced with unbiased thermal annealing, indicating the detrapping or neutralization of part of the HC-induced damage.

The effect of front gate direct tunnel stress is investigated on long channel devices by analyzing the front and back channel I-V characteristics and the front gate switch-off I_D transients. No significant degradation of I-V curves and transient times is observed for stress biases up to about two times the power supply for this technology node (V_{DD} = 1.5 V) and reasonable stress times. For higher front gate direct tunnel stress conditions, the transient times are progressively reduced till front gate dielectric breakdown occurs.

2. Devices and experimental details

The PD SOI MOSFETs used in this study were fabricated in a 0.1 μ m-CMOS process using a PELOX (polysilicon-encapsulated LOCOS) isolation scheme, a 2.5 nm nitrided gate oxide (NO), a 150 nm polysilicon gate and 80 nm nitride spacers. Processing was performed on 200 mm diameter UNIBOND wafers, resulting in a final film thickness of

100 nm. The buried oxide (BOX) thickness was 400 nm. In order to control the short channel effects (SCE), the devices received a halo implantation. To investigate its impact on the hot-carrier degradation, MOSFETs without halo (abbreviated no-halo) were also included in the study. The latter show more pronounced SCE for V_{Tf} .

The test structures have common gate and source configuration with separate drain pads. There is no film contact. N- and p-channel transistors with polysilicon gate lengths (L) ranging from 0.08 to 10 μm and fixed width ($W = 10 \mu\text{m}$) were studied. However, the results shown in this study focus only on the n-channel devices, which showed significant and interesting degradation after hot-carrier stress.

For the hot-carrier degradation analysis, the transistors were stressed at constant-voltage stress, with drain voltages (V_D) ranging from the power supply voltage ($V_{DD} = 1.5 \text{ V}$) up to 3.5 V for the longest transistors ($L = 10 \mu\text{m}$) and under different front gate stress regimes from $V_{FG} \approx V_{Tf}$ to $V_{FG} = V_D$. The effect of the electric stress on the devices was mainly evaluated through the analysis of front and back channel input (I_D vs. V_{FG} and I_D vs. V_{BG}) and output (I_D vs. V_D) characteristics, which were regularly measured between the different stress phases. Owing to the floating body nature of the devices under study, special attention was paid to ensure that steady-state conditions were reached before performing the measurements after the different hot-carrier stress phases. A set of different front and back channel parameters, among them the front and back gate threshold voltages (defined as $V_{Tf} \equiv V_{FG} @ I_D = 0.01 \text{ W/L } \mu\text{A}$ and $V_{Tb} \equiv V_{BG} @ I_D = 10^{-11} \text{ A}$), were used as primary degradation monitors.

All current-voltage measurements and switch-off I_D transients were measured using an HP-4155 Parameter Analyzer. During a conventional weak inversion single-gate switch-off experiment, the front gate is switched at $t = 0$ s from an ‘on’ gate bias (V_{FGon}) above V_{Tf} to an ‘off’ gate bias (V_{FGoff}) in the subthreshold regime [28]. Care was taken with the duration of the ‘on’ bias level, as well as for the conditions between two transient measurements, so that there were no device history (memory) effects. Unless, the contrary is indicated, the back gate was grounded and the drain bias was kept in the linear operation regime ($V_D = 25$ mV) for all measurements. All experiments were carried out in a lightproof and electrically shielded setup.

3. Hot-carrier degradation under $V_{FG} = V_D$ regime

3.1 Degradation of front channel characteristics

A set of transistors were subjected to hot-carrier stress under $V_{FG} = V_D$ regime, which has been recently reported to arise as the worst V_{FG} case for HCD on devices of comparable technology conditions [25]. In accordance with the above already reported results, the HC-induced degradation is found to be initially dominated by a positive shift of V_{Tf} (Fig. 1(a)). In some cases, a significant attenuation of the 2nd g_{mf} peak is observed, which can be attributed to a higher recombination after HC stress of the EVB excess carriers introduced into the film [25]. As a consequence of the initial HC-induced positive ΔV_{Tf} , a clear tendency to overlap between the conventional mobility-related 1st g_{mf} peak and the EVB-induced 2nd g_{mf} peak is observed, making it difficult to

distinguish between the above two g_{mf} peaks for the curves with the highest positive ΔV_{Tf} (Fig. 1(a)). Moreover, in accordance with the registered ΔV_{Tf} , a significant change in the subthreshold slope of the front gate I_D vs. V_{FG} characteristics (SS_f) is also observed (Fig. 1(b)).

In contrast with the previous reported results, a clear turn-around behaviour for ΔV_{Tf} is noticed under our experimental conditions after sufficiently long HC stress (Fig. 2(a)). This turn-around behaviour is also followed by SS_f and the I_D measured during the different HC stress phases ($I_{Dstress}$) (Figs 2(a) to 2(c)). As expected, this HCD mode is found to be accelerated for reduced L and increased stress bias conditions (Figs 2(a) to 2(c)).

3.2 Degradation of back channel characteristics

Another important characteristic of the HCD of these devices is given by the appearance of a significant positive back gate threshold voltage shift (ΔV_{Tb}) after sufficient long HC stress (Fig. 3(a)), pointing to an effective negative charge trapping in the silicon/BOX interface or near the BOX/PELOX isolation edges.

Figure 3(b) shows ΔV_{Tb} results as a function of HC stress time for different nMOSFETs stressed under $V_{FG}=V_D$ conditions. The results corresponding to some devices with no-halo drain architecture are also plotted for comparison, showing higher HCD in the case of these short channel devices with increased drain current drivability due to short

channel effect V_{Tf} lowering. As expected, this back channel HCD is also found to be accelerated for reduced L and increased stress bias conditions (Fig. 3(b)).

In order to assess the hot-carrier-induced degradation in the back channel characteristics under different HC stress conditions, a device lifetime criterion associated with the back channel degradation was defined at $\Delta V_{Tb} = 0.5$ V. Fig. 3(b) insets give the back channel device lifetime versus stress $1/V_D$ plots for $L = 0.12$ μm halo and $L = 0.14$ μm no-halo devices, showing a characteristic HCD exponential dependence on $1/V_D$ [29].

This effective negative charge trapping affecting the back channel threshold voltage appears to saturate for ΔV_{Tb} values around 5 V. Assuming a HC-induced uniform effective density of negative trapped charges placed in the buried oxide and near the film interface (N_{OXBG}), a value around $2.7 \cdot 10^{11}$ charges/ cm^2 can be estimated for this saturation N_{OXBG} (with $N_{\text{OXBG}} = \Delta V_{Tb} \cdot \epsilon_{\text{BOX}} / t_{\text{BOX}}$, where t_{BOX} and ϵ_{BOX} are the involved back gate oxide thickness and permittivity, respectively). Although there is no straightforward reason for the saturation behaviour observed, it is thought that it may be related to the build-up of HC-induced charges in the region close to the back channel/field isolation edges.

3.3 Degradation of switch-off I_D transients

The analysis of the I_D transients observed on PD SOI MOSFETs when switching off one of the two gates is nowadays a well-established technique for the estimation of

silicon film generation and recombination lifetimes [2,3,30-32]. In order to avoid short and narrow device geometry effects on I_D transients [2,33], long and wide channel transistors (with L and W in the range of $10\text{ }\mu\text{m}$) are normally used for such lifetime extraction. After switching-off the device, an increase of I_D is generally observed for several tens of seconds until the I_D steady state value ($I_D(t=\infty)$) is reached [28]. It has been shown that for a fixed temperature the measured I_D transient time (defined, for example, as the time to reach 90% of $I_D(t=\infty)$) can be used to extract the effective film generation lifetime (τ_{geff}) of PD SOI MOSFETs, by means of an approximated linear relationship [30]. Using this procedure, a τ_{geff} around $0.2\text{ }\mu\text{s}$ has been extracted for the devices under study in this work [28,34]. These values are in the range of the data published in the literature for similar good quality SOI material and conditions [1,30-32]. In fact, the absolute lifetime value is not so important, but it arises as a useful parameter for comparison between different starting material, processing or contamination conditions.

In the past, similar transient techniques were applied to characterize different SOI material technologies [30-32], as well as to study the impact of radiation on the bulk and surface generation lifetime components [34-36]. Of course, the impact of HCD on I_D transients has not been a primary interest, probably due to the inherent use of short L devices with increased small geometry leakage components, making them not suitable for accurate film lifetime extraction.

In spite of the above, in our present study we were interested in the I_D transients of such short channel devices, not for film lifetime extraction purposes, but just to investigate

the possible impact of HCD, specially when taking into account the fact that for this FB devices with a thin front gate oxide, EVB injection is responsible for a change of their shape from undershoot to overshoot when V_{FGon} is above the V_{FG} threshold for EVB tunnelling ($V_{FGon} = 1.5$ V data in Fig. 4). In fact, this probes the injection of majority carriers into the substrate [4,5] which have to disappear after switching off the device. The shape of these transients has been found to fit well with conventional (EVB-free) switch-on type transients [28], which enable the extraction of the majority carrier recombination lifetime in large area devices [32]. Since carrier recombination is usually faster than generation [32,37], in such long channel devices, the transients in the EVB tunnelling regime ($V_{FGon} = 1.5$ V) are normally faster compared with the conventional switch-off ones ($V_{FGon} = 0.7$ V) [28,34].

In order to investigate the impact of HCD on generation and recombination I_D transients, single gate switch-off I_D transients were measured for the nMOSFETs before and after HCD, using V_{FG} voltages above and below the threshold voltage for body to gate EVB tunneling. A particular characteristic observed for the I_D transients of such short channel devices has been their short duration compared to the ones measured for their longer channel counterparts (which will be analyzed later for the front gate direct tunnel stress studies). Moreover, for this short channel nMOSFETs of HC interest, similar transition times for generation and recombination processes have been found (Fig. 4), what is interpreted as the result of junction leakage components dominating these generation and recombination I_D transients.

As can be observed from $V_{FGon} = 0.7\text{ V}$ and 1.5 V results in Fig. 4, both, the switch-off transients below and above the V_{FG} threshold for body to gate EVB tunneling, become much faster after HCD, which can be attributed to a HC-induced degradation of the effective film generation and recombination lifetimes by means of an increase of the surface contribution [35,36]. At the same time, the steady-state I_D levels ($I_D(t=\infty)$) have been found to consistently evolve according to the registered V_{Tf} degradation.

4. Hot-carrier degradation under different V_{FG} regimes

Up to now, the hot-carrier reliability analysis has been limited to the $V_{FG} = V_D$ condition. However, it is well-known that the degradation mechanism can be governed by the gate stress condition. In particular, for the case of nMOSFETs of conventional bulk technologies, the most important hot-carrier degradation mechanism, determining their device lifetime, is widely recognized to be associated to interface state generation [11,12,38], which, for a given V_D stress bias, is usually found to peak for gate voltages near to the maximum substrate current condition ($V_{FG} \approx V_D/2$) [11,12,39]. Moreover, in the case of SOI FB devices, high HCD rates have been reported for low gate bias conditions, where the effects of parasitic bipolar action may lead to enhanced HC degradation [21,22].

From the above, in order to evaluate in more detail the mechanisms leading to hot-carrier degradation on the studied PD SOI nMOSFETs, the whole range of V_{FG} -stress regimes was considered. In this way, Figs 5(a) and 5(b) show degradation results for the

front and back gate threshold voltages, respectively, corresponding to different $L = 0.12$ μm nMOSFETs stressed under a fixed V_D and different V_{FG} conditions. From the figures, it is clear that the highest V_{FG} conditions lead to a faster progress of the HC degradation. In particular, from Fig 5(b) results, under V_{FG} conditions below the threshold voltage for EVB majority carrier injection into the film ($V_{FG} \sim 1.1\text{-}1.2$ V), no significant ΔV_{Tb} is registered for reasonable short HC stress times. In this way, these results are in agreement with previous studies pointing to an enhanced HCD under the conditions giving rise to maximum EVB injection of majority carriers into the film [23,25,27].

In the Fig. 5(b) inset the corresponding device lifetime associated with the back channel degradation versus stress V_{FG} plot is given, showing an exponential dependence of HCD lifetime on stress V_{FG} (lifetime $\propto e^{-\alpha V_{FG}}$). The slope of this strong V_{FG} dependence ($\alpha \approx 5$) is in the range of recent front channel HCD results reported for devices of a comparable technology in similar V_{FG} conditions with EVB injection of majority carriers into the film [25].

5. Thermal annealing effects

In the cases of generation of damage by radiation [40] or electric stress [41,42], it is well-known that part of the trapped charges in SiO_2 dielectrics can be annealed by bias annealing performed at room temperature, where the tunnelling mechanism is dominant, or thermal annealing performed at elevated temperatures, where the thermal process

eventually becomes dominant. In the same way, for the case of hot-carrier-induced damage, the injection of opposite type of charges or detrapping of trapped carriers may lead also to partial recovery of the degraded parameters [43]. Very recently, thermal annealing results of radiation-induced damage on the 2nd g_{mf} peak of PD SOI nMOSFETs of a similar technology have been reported [44].

In order to gain better insight into the HC-induced damage observed in the devices under study and evaluate its thermal stability, a thermal annealing experiment was carried out by applying different constant temperature annealing phases up to 250 °C to a previously HC-stressed nMOSFET. During the thermal anneals, the device terminals were left floating and care was taken in order to get enough cooling of the samples down to room temperature before the measurements were performed. Table 1 describes the details about the HC-stressed device and the different heating phases performed, the corresponding front and back gates input characteristics are given in Figs 6(a) and 6(b), respectively.

A first characteristic of Figure 6(a) results is the fact that the measurements carried out on a stressed device several weeks after its electric stress were found to exhibit no appreciable differences on front channel characteristics compared with the ones performed just at the end of the electric stress. On the other hand, a slight recovery of the damage was observed for the back channel characteristics (in the range of 0.5 V for ΔV_{Tb} , Fig. 6(b)), thus indicating the presence of some appreciable room temperature annealing for the case of the back channel HCD.

When the HC-stressed device was heated during 5 min at 140 °C, no appreciable additional recovery was observed. By applying a thermal anneal at higher temperature (15 min at 200 °C), a back gate threshold voltage recovery in the range of 1 V was registered (Fig. 6(b)), whereas no significant changes were observed in both, the front channel characteristics above V_{Tf} (Fig. 6(a)) and the subthreshold slope region (not shown here). A subsequent anneal of 15 min at 200 °C resulted in no additional recovery of the damage. However, when the annealing temperature was increased, an additional back gate threshold voltage recovery in the range of 1 V was registered after 15 min at 240 °C (Fig. 6(b)). These results show the presence of a thermal detrapping or neutralization process affecting part of the back channel HC-induced damage. On the other hand, no significant changes in front channel characteristics were observed (Fig. 6(a)).

6. Nature and localization of the damage

In view of the above HCD mode characterized by a turn-around behavior for ΔV_{Tf} coinciding in stress time with a significant effective negative charge trapping affecting the back channel characteristics (Figs 2, 3 and 5), different additional studies were carried out to evaluate any possible impact of back channel degradation on front channel characteristics. In this way, it has been recently pointed out that the transistors of a PD SOI technology in terms of film thickness, may behave as FD for the shortest channel lengths, due to the proximity of source and drain junctions reducing the apparent doping seen from the gate and making full depletion easier [45].

In order to evaluate this possibility, front channel input and output characteristics were measured not only with the back gate grounded but also applying a negative accumulation bias. In this way, Fig. 5(a) shows some results obtained for ΔV_{Tf} when measuring I_D - V_{FG} characteristics with $V_{BG} = -20$ V bias condition. From these results and from similar ones obtained for different front channel parameters and characteristics, no apparent gate coupling between front and back channel HC-induced damage is observed. Moreover, this is in agreement with the fact that no appreciable gate coupling effects between front and back channels are observed when measuring front gate characteristics at different V_{BG} conditions on non-stressed long and short channel devices.

More importantly, owing to the fact that under the ΔV_{Tf} turn around conditions the sign for the changes in V_{Tf} and V_{Tb} are different, it is thought that any possible gate coupling between the front and back channel HCD should not happen in our studies [16].

Moreover, this is supported by the fact that under certain stress conditions the ΔV_{Tf} turn around behavior is already observed without the presence of any appreciable ΔV_{Tb} (Figs 5(a) and 5(b)).

Following the above observations, it has to be mentioned that similar HCD modes were already observed in the past in FB SOI nMOSFETs stressed under high V_D hot-carrier conditions [46,47]. In those works, similar turn-around behaviours for V_{Tf} were attributed to a hole injection mechanism becoming dominant in front channel degradation after certain HC stress time. At the same time, significant opposite sign V_{Tb}

shifts were also registered and they were attributed to interface trap generation and electron trapping in the back gate [46].

In view of this particular hot-carrier degradation mode, both, front and back channel input (I_D vs. V_{FG} and I_D vs. V_{BG}) and specially output (I_D vs. V_D) characteristics were measured before and after HC stress experiments, both, interchanging and without interchanging the source for the drain relative to the configuration in which the stress was performed. It was expected that if the hot-carrier induced damage occurred in a localised region close to the drain junction, their electrical effects would be masked by the drain depletion region, making the device asymmetric to source-drain interchange after HCD [48]. However, no appreciable asymmetry was observed in the input and output front and back channel characteristics before and after HCD.

In spite of the above source to drain symmetry results, it has to be also mentioned here that quite often the back gate transconductance characteristics after HC stress have been found not only to shift according to the registered ΔV_{Tb} , but also to slightly increase its maximum value (Fig. 3(a)). It is thought that this could be due to a parasitic back channel/isolation edge component. A similar effect has been attributed to the impact of a localized hot-carrier-induced negative charge trapping near the back channel drain junction, giving rise to a local increase of V_{Tb} and an overshoot in the measured g_{mb} , which has been explained in terms of a two- V_{Tb} model and the exchange of the dominant role between the damaged and the undamaged portions of the back channel [49,50].

7. Front gate direct-tunnel stress

Finally, in view of the observed HC degradation reported in previous chapters, a last step in our study was to check the response to electric stress of the longest transistors (L in the range of $10\text{ }\mu\text{m}$). In this way, some long channel nMOSFETs were subjected to both, HC stress under the worst-case V_{FG} condition ($V_{FG}=V_D$) and front gate direct tunnel stress. The degradation effects were investigated by the analysis of the front and back channel I-V characteristics and the front gate switch-off I_D transients. From this study, no significant degradation of the nMOSFETs I-V curves and I_D transients was observed for realistic stress biases up to about two times the power supply associated to this technology (i.e., up to about $2 \times (V_{DD}= 1.5\text{ V})= 3\text{ V}$) and reasonable stress times (in the range of a few thousands of seconds).

If the front gate direct tunnel stress conditions were further increased, no significant changes were registered for either, front or back channel characteristics (as shown in Table 2 and Fig. 7 results), but the generation and recombination I_D transient times were progressively degraded (Fig. 8). Finally, front gate dielectric breakdown occurred, causing an important increase in gate current and loss of front gate control on the front channel inversion charge (Fig. 7(a)). Under these conditions, the I_D transients disappeared (Fig. 8).

8. Conclusions

The impact of hot-carrier stress on thin gate oxide PD SOI nMOSFETs has been investigated by studying the front and back channel current-voltage characteristics and the switch-off drain current transients.

A particular hot-carrier degradation mode characterized by a turn-around behavior for front gate threshold voltage degradation has been observed for devices with different geometries, bias conditions and source/drain architecture. A significant positive back gate threshold voltage shift has been also observed after long HC stress. The maximum hot-carrier degradation has been found to be produced under the highest front gate biases, corresponding to the conditions of maximum electron valence band injection of majority carriers into the floating body. The presence of the HCD has been found to reduce both, the generation and the recombination switch-off drain current transient times. Unbiased thermal annealing in the range of 200°C to 250°C has been found to significantly reduce the hot-carrier induced damage affecting the back channel characteristics.

Whereas front gate direct tunnel stress is not found to cause any significant degradation for stress biases up to about two times the power supply associated to this technology and reasonably short stress times, for the highest stress conditions the drain current transients have been found to be progressively faster till front gate dielectric breakdown occurs.

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FIGURE CAPTIONS

Fig. 1: (a) Drain current (I_D) and corresponding front gate transconductance (g_{mf}) characteristics measured from accumulation to inversion V_{FG} sweep for an $L=0.13 \mu m$ nMOSFET before hot-carrier degradation and after different stress times at $V_D=V_{FG}=2 V$ stress bias condition. (b) Corresponding I_D versus V_{FG} characteristics in the subthreshold region.

Fig. 2: (a) Front gate threshold voltage shift (ΔV_{Tf}), (b) subthreshold slope change (ΔSS_f) and (c) degradation of I_D measured during stress ($\Delta I_{Dstress}/I_{Dstress0}$) versus hot-carrier stress time for different nMOSFETs stressed under $V_{FG}=V_D$ conditions. (where $\Delta I_{Dstress}=I_{Dstress}-I_{Dstress0}$ and $I_{Dstress0}$ corresponds to the $I_{Dstress}$ value just at the beginning of the HC stress).

Fig. 3: (a) Drain current (I_D) and corresponding back gate transconductance (g_{mb}) characteristics for an $L=0.12 \mu m$ nMOSFET before hot-carrier degradation and after different stress times at $V_D=V_{FG}=2.25 V$ stress bias condition. (b) Back gate threshold voltage shift (ΔV_{Tb}) versus hot-carrier stress time for different nMOSFETs stressed under $V_{FG}=V_D$ conditions. In the inset there are given the back channel device lifetime (defined as the time to reach $\Delta V_{Tb}=0.5 V$) versus stress $1/V_D$ plots for $L=0.12 \mu m$ halo and $0.14 \mu m$ no-halo devices.

Fig. 4: Switch-off I_D transients measured for two V_{FGon} conditions (above (1.5 V) and below (0.7 V) V_{FG} threshold for EVB direct tunnel majority carrier injection into the floating film) for Fig. 1 nMOSFET after different stress times at $V_D=V_{FG}=2 V$.

Fig. 5: (a) Front gate threshold voltage shift (ΔV_{Tf}) and (b) back gate threshold voltage shift (ΔV_{Tb}) versus hot-carrier stress time for different $L = 0.12 \mu\text{m}$ nMOSFETs stressed under a fixed V_D stress bias and different V_{FG} conditions. In the inset it is given the corresponding back channel device lifetime (defined as the time to reach $\Delta V_{Tb} = 0.5 \text{ V}$) versus stress V_{FG} plot.

Fig. 6: (a) Front gate and (b) back gate drain current (I_D) and corresponding transconductance (g_{mf} and g_{mb} , respectively) characteristics measured for an $L = 0.12 \mu\text{m}$ nMOSFET according to the the sequence of hot-carrier stress and thermal annealing phases reported in Table 1.

Fig. 7: (a) Front gate and (b) back gate drain current (I_D) and corresponding transconductance (g_{mf} and g_{mb} , respectively) characteristics measured for an $L = 10 \mu\text{m}$ nMOSFET before and after the sequence of front gate direct tunnel stress phases reported in Table 2.

Fig. 8: (a) Front gate switch-off I_D transients, normalized to V_{FGoff} steady-state level ($I_D(t=\infty)$), measured for two V_{FGon} conditions (above (1.5 V) and below (0.7 V) V_{FG} threshold for EVB majority carrier injection into the floating film) for Fig. 7 $L = 10 \mu\text{m}$ nMOSFET before and after the different electric stress phases reported in Table 1. (b) Corresponding I_D generation transient times (defined as the time to reach 90% (undershoot) of $I_D(t=\infty)$) extracted from $V_{FGon} = 0.7 \text{ V}$ to $V_{FGoff} = 0.1 \text{ V}$ data.

TABLE CAPTIONS

Table 1: Description of the sequence of thermal anneal phases applied to the HC-stressed long nMOSFET under study in figures 6(a) and 6(b).

Table 2: Description of the sequence of electric stress phases applied to the long nMOSFET under study in figures 7 and 8.

Fig. 1(a)

Fig. 1(b)

Fig. 2(a)

Fig. 2(b)

Fig. 2(c)

Fig. 3(a)

Fig. 3(b)

Fig. 4

Fig. 5(a)

Fig. 5(b)

Fig. 6(a)

Fig. 6(b)

Fig. 7(a)

Fig. 7(b)

Fig. 8(a)

Fig. 8(b)

Thermal anneal phases	
Virgin	Virgin device
HC-stressed	After 18000 s hot-carrier stress @ $V_{FG}=V_D= 2.25$ V
"1"	Re-measured after 20 weeks at room temperature
"2"	+300 s @140°C
"3"	+900 s @200°C
"4"	+900 s @200°C
"5"	+900 s @240°C

Table 1

Electric stress phases	
Virgin	Virgin device
"1"	1100 s @ $V_{FG} = 3.75$ V ($V_D = V_S = V_{BG} = 0$ V)
"2"	6100 s @ $V_{FG} = 3.75$ V ($V_D = V_S = V_{BG} = 0$ V)
"3"	11100 s @ $V_{FG} = 3.75$ V ($V_D = V_S = V_{BG} = 0$ V)
"4"	+300 s @ $V_{FG} = 4$ V ($V_D = V_S = V_{BG} = 0$ V)
"5"	+300 s @ $V_{FG} = 4.25$ V ($V_D = V_S = V_{BG} = 0$ V)

Table 2