Hot-carrier-induced degradation of drain current hysteresis and transients in thin gate oxide floating body partially depleted SOI nMOSFETs

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Abstract

The impact of hot-carrier degradation on drain current (I_D) hysteresis and switch-off I_D transients of thin gate oxide floating body PD SOI nMOSFETs is analyzed. An extended characterization of these floating body effects (FBEs) is carried out for a wide range of transistor geometries and bias conditions. The results show a link between the hot-carrier-induced damage of the front channel and the reduction of the FBEs. This is further supported by unbiased thermal annealing experiments, which are found to give rise to a partial recovery of the hot-carrier induced damage and FBEs.

1. Introduction

In recent years, silicon on insulator (SOI) technologies have emerged as a serious competitor to bulk silicon technology. Owing to device integration requirements and intrinsic resistance constraints of the thin film layers, no film contacts are generally supplied. If body contacts are not present, so-called floating body effects (FBEs) arise, specially in partially depleted (PD) SOI MOSFETs, leading to some detrimental effects on device performance [1]. In particular, after switching on or off the front gate, there is no substrate current to quickly adjust the majority carrier density and equilibrium has to be reached through generation and recombination processes. Under these conditions, drain current (I_D) transients [1] are observed, and these can be a useful tool for assessing the quality of the starting material, process-induced defects or contamination.

More recently, with the marked decrease in front-gate-oxide thickness, a new type of FBEs associated with gate-body direct tunneling has been identified [2,3]. For thin gate oxides (as thin as 2-2.5 nm), electron valence band (EVB) tunneling, occurring for a sufficiently large front-gate voltage (V_{FG}) supplies majority carriers that charge the film and forward-bias the source-body junction, inducing a "kink" in the linear I_D-V_{FG} characteristics and a second peak in the derived transconductance (g_{mf}) [2,3]. Associated with this effect, a change in the I_D transients shape is also observed [2,3]. The presence of these gate-induced FBEs (GIFBEs) [2] leading to history and memory effects, could be a limitation for partially depleted (PD) SOI CMOS circuit operation [4].

The problems associated with hot carriers (HC) have been recognized as one of the major constraints in silicon MOS scaling. Hot carriers are generated by the

high lateral electric fields near the drain MOSFETs junction and may attain enough energy to overcome the Si/dielectric barrier, causing damage in this region, which leads to a gradual degradation of transistors current-voltage characteristics [5]. The damage is commonly believed to result in charge trapping in the gate dielectric and interface-state generation at the Si/dielectric interface.

In spite of the fact that FB SOI MOSFETs have been considered to be more resistant to HC degradation (HCD) than their bulk counterparts, what has been mainly attributed to a lower channel electric field [6], the presence of two different gates and their corresponding different interfaces makes HCD in SOI MOSFETs a more complex subject. In particular, opposite channel injection phenomena may occur [7], and, with the reduction in film thickness and fully depleted (FD) operation, coupling effects between the damage generated at the different gates [1]. More recently, with the introduction of very thin (below around 2.5 nm) SiO_2-based gate oxides, the high gate bias regimes have been shown to suffer from enhanced HCD [8,9], what has been attributed to the impact of the EVB direct tunneling injection phenomena, where the majority carriers introduced into the floating film have been reported to be responsible for this enhanced HCD [10].

In this study, we analyze the impact of hot-carrier degradation on drain current (I_D) hysteresis and switch-off I_D transients of thin gate oxide floating body PD SOI nMOSFETs. An extended characterization of these floating body effects is carried out for a wide range of transistor geometries and bias conditions. The results show the existence of a link between the hot-carrier-induced damage of the front channel and the reduction of the FBEs. This is further supported by unbiased thermal annealing experiments in the range of 150ºC-250ºC, which are found to give rise to a partial recovery of the hot-carrier-induced damage and FBEs.

2. Devices and experimental details

The PD SOI nMOSFETs used in this study were fabricated in a 0.1 μm-CMOS process using a PELOX (polysilicon-encapsulated LOCOS) isolation and 2.5 nm nitrided gate oxide (NO). Processing was performed on 200 mm diameter UNIBOND wafers, with a final film thickness of 100 nm. The buried oxide (BOX) thickness was 400 nm. There is no film contact. Transistors with mask gate length (L) ranging from 0.08 μm to 10 μm and width (W) from 0.2 μm to 10 μm were studied.

For the hot-carrier degradation experiments, the transistors were stressed at constant-voltage conditions and the degradation was mainly evaluated through the analysis of front and back channel input characteristics (I_D vs. V_{FG} and I_D vs. V_{BG}, respectively), which were regularly measured between the different stress phases. Owing to the floating body nature of the devices under study, special attention was paid to ensure that steady-state conditions were reached before performing the measurements after the different hot-carrier stress phases. A set of different front and back channel parameters, among them the front gate threshold voltage (defined as $V_{Tf} \equiv V_{FG}$ @I_D= 0.01 W/L μA), were used as primary degradation monitors.

All current-voltage measurements and switch-off I_D transients were measured using an HP-4155B Parameter Analyzer. During a conventional weak inversion single-gate switch-off experiment, the front gate is switched at t= 0 s from an 'on' gate bias (V_{FGon}) above V_{Tf} to an 'off' gate bias (V_{FGoff}) in the subthreshold regime [11]. Care was taken with the duration of the 'on' bias level, as well as for the conditions between two transient measurements, so that there were no device history (memory) effects. Unless, the contrary is indicated, the back gate (chuck contact to wafer substrate) was grounded and the drain bias was kept in the linear operation regime (V_D= 25 mV). All experiments were carried out in a lightproof and electrically shielded setup.

3. I_D hysteresis characterization

Figure 1 shows I_D–V_{FG} and the derived g_{mf}–V_{FG} characteristics corresponding to a floating body PD-SOI nMOSFET when V_{FG} is swept from both, accumulation to inversion (V_{FG} sweep > 0) and inversion to accumulation (V_{FG} sweep < 0). It is known that I_D hysteresis appears in these conditions, which is related to the floating body nature of the devices. The hysteresis can be defined as the I_D difference between accumulation to inversion and inversion to accumulation V_{FG} sweeps (Figure 1) [12].

The first peak in the I_D hysteresis curve (positive hysteresis peak for V_{FG} around V_{Tf} ~ 0.5 V in Figure 1) is associated with the body potential difference between the switch-on and switch-off conditions present during the accumulation to inversion and inversion to accumulation V_{FG} sweeps, respectively [1,11]. In the case of an nMOSFET, when V_{FG} is swept from accumulation to inversion, holes have to be recombined to increase the space-charge depletion region for the new

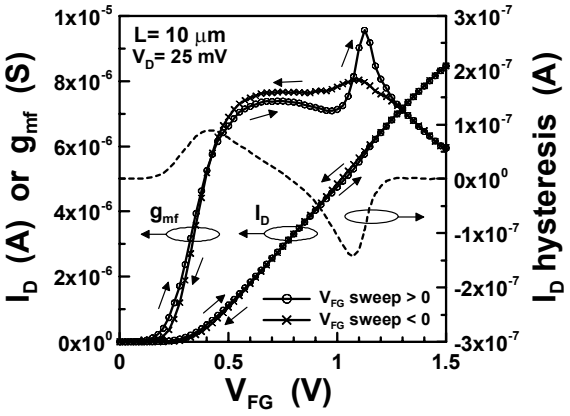

Figure 1. I_D and g_{mf} vs. V_{FG} measured from accumulation to inversion (V_{FG} sweep > 0) and inversion to accumulation (V_{FG} sweep < 0) for an L=10μm nMOSFET. The corresponding I_D hysteresis between the two sweep directions is also shown.

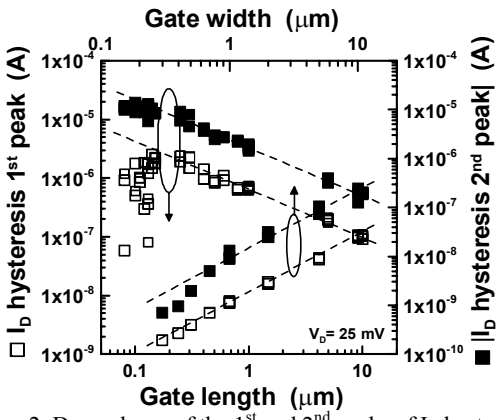

Figure 2. Dependence of the 1st and 2nd peaks of I_D hysteresis (positive and negative, respectively) on transistor gate L and W.

V_{FG} condition. While this recombination process occurs, the V_{Tf} of the device is slightly lower than the one that would correspond to such a V_{FG} in steady state conditions. On the other hand, when V_{FG} is swept from inversion to accumulation, holes have to be generated to replenish the space-charge region, during this generation process, V_{Tf} is slightly higher than the one corresponding to steady state conditions [1,11].

The second peak observed in the I_D hysteresis curve (around V_{FG}=1.1 V in Figure 1) is originated by the EVB tunneling phenomenon, which is characteristic of these thin gate oxide FB devices, and supplies majority carriers (holes) that charge the film and forward-bias the source-body junction, reducing V_{Tf} and inducing a "kink" in the linear I_D-V_{FG} characteristics and the 2nd peak in the derived g_{mf} [2,3]. In previous studies, the influence of different sweeping time steps on the GIFBEs [2,3], as well as the temperature dependence of the I_D hysteresis peaks [12], have been pointed. Since time step issue is a critical point for FB devices, unless the opposite is indicated, a fixed 20 ms integration time was kept for all the I_D double sweeps, which where performed at fixed room T conditions.

Originating from generation and recombination processes, the I_D hysteresis, as well as the I_D transients [11], can be a useful tool for assessing the quality of the starting material, process-induced defects, or contamination. An extended characterization of I_D hysteresis was carried out for a wide range of transistor geometries (L and W) and bias conditions. The behavior of both, the conventional positive 1st peak of I_D hysteresis, as well as the EVB-induced negative 2nd peak of I_D hysteresis were studied. Figure 2 shows the dependence of both I_D hysteresis peaks on transistor gate L and W. From the figure, it is appreciated an overall linear dependence of their magnitudes with L and W, thus corroborating their expected scaling with channel current. In spite of the above general trends, the 1st peak of I_D hysteresis is found to be more sensitive to short channel effects, while the 2nd peak of I_D hysteresis seems to be more sensitive to narrow channel effects.

The decrease of the 1st I_D hysteresis peak values for L below 0.20 μm is thought to be originated by the influence of the corresponding nearby high negative 2nd I_D hysteresis peak. The fact that these devices received a halo (or pocket) source/drain extensions implantation (to suppress short channel effects) makes their V_{Tf} to slightly increase for the shorter L (reverse short channel effect). In this way, V_{Tf} of an L= 0.1 μm nMOSFET is about 0.2 V higher than the corresponding value for an L=10 μm device [13]. The higher position of V_{Tf}, as well as the increasing magnitude of the EVB-related negative 2nd peak of I_D hysteresis, is thought to lead to some impact on the values for the 1st peak of I_D hysteresis in the shorter devices (L < ~ 0.2 μm). In fact, as it will be shown later, this phenomenon can be also observed in the case of HC-stressed short L devices, in which a HC-induced positive ΔV_{Tf} can also lead to a higher degree of overlap between the two I_D hysteresis peaks. From the above, it is inferred that the 1st peak of I_D hysteresis may not be a very suitable parameter for assessment of FBEs degradation in short-L nMOSFETs.

It should be also commented that the sensitivity to narrow channel effects of the EVB-related 2nd peak of I_D hysteresis can be associated with the higher generation/recombination rates expected near the isolation, which leads to reduced FBEs [1]. Regarding to

the other remaining L and W dependences, only a saturation of the 2nd I_D hysteresis peak is observed in the short L region, which is also observed for the g_{mf} peaks [14]. On the other hand, the narrow channel effects seem not to affect the conventional 1st peak of I_D hysteresis, as they also do not do for V_{Tf}.

4. Hot-carrier degradation

A set of transistors were subjected to constant-voltage HC stress under different V_D and V_{FG} conditions. A particular HCD mode, characterized by a positive front gate threshold voltage shift with a turn-around behavior for long term stress was observed [9]. A significant negative charge trapping in the back gate was also observed after long HC stress. However, in this study, we concentrate on the investigation of the degradation of two main FBEs, which are the I_D hysteresis and the switch-off I_D transients. For this purpose, the results shown in this chapter will mainly refer to the first phases of the HCD (that is, for low stress conditions that correspond to either low stress voltages or times and/or longer channel devices), in which the damage is mainly limited to the front channel [9]. For harder stress conditions, the damage also affects the back channel and a more dedicated analysis is needed, in particular, under such higher damage conditions the switch-off I_D transients rapidly vanish [9].

4.1. Hot-carrier degradation of I_D hysteresis

Figure 3 shows a typical example of the I_D hysteresis measured for an nMOSFET after different HCD stress times. A clear decrease of the magnitude of the positive and negative I_D hysteresis peaks is observed. Moreover, a significant V_{FG}-shift is observed for the conventional positive I_D hysteresis peak, which can be associated with the HC-induced ΔV_{Tf} experimented by the devices. However, no such a behavior is observed for the case of the EVB-related 2nd peak of the I_D hysteresis, thus leading to a higher degree of overlap between the two I_D hysteresis peaks after hot-carrier degradation.

In the case of FB SOI MOSFETs under low V_D conditions, it is considered that the dominating generation and recombination mechanisms can occur in four main regions: the channel space-charge and film region, the source and drain junctions, and the front and back channel interfaces [15].

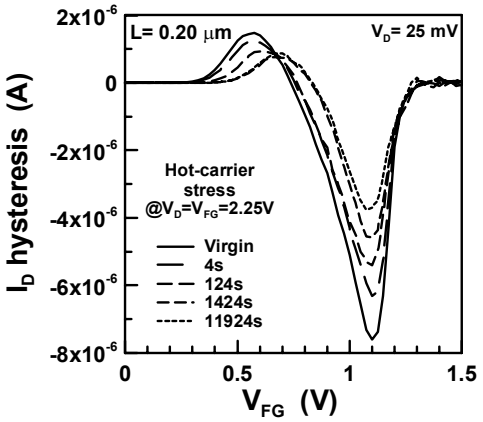

Figure 3. I_D hysteresis measured for an nMOSFET before hot-carrier degradation and after different stress times.

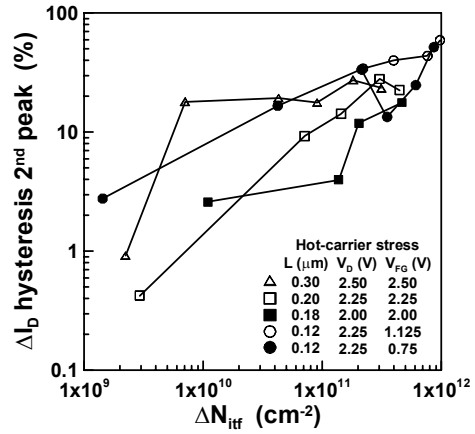

Figure 4. Degradation of 2nd peak of I_D hysteresis vs. front channel density of interface states generated during HC stress of different nMOSFETs (extracted according to [16]). (ΔI_D hysteresis is given in percentage ($I_{Dhysteresis}$-$I_{Dhysteresis0}$)/$I_{Dhysteresis0}$, where $I_{Dhysteresis0}$ is before stress value).

In order to evaluate a possible correlation between the HC-induced damage and the observed I_D hysteresis behavior, figure 4 shows the dependence of the 2nd peak of I_D hysteresis on the increase of the front channel density of interface states (ΔN_{itf}) generated during the HC stress of different nMOSFETs. Although a slight scattering of the I_D hysteresis peak values can be sometimes observed (what can be attributed to experimental conditions and the use of such a short L devices, for which the 2nd peak of I_D hysteresis can be affected by geometrical factors (Figure 2)), an overall correlation between the HC-induced damage and the reduction of the I_D hysteresis can be appreciated.

4.2. Hot-carrier degradation of switch-off I_D transients

In order to investigate the impact of HCD on generation and recombination I_D transients, front gate switch-off I_D transients were measured for the nMOSFETs before and after HCD, using V_{FGon} voltages above and below the V_{FG} threshold voltage for body to gate EVB tunneling [11]. The results after HCD showed faster generation and recombination processes in the film (Figure 5), with a correlation between the HCD of the front channel and the reduction of this FBE. This suggests an increased contribution of surface states on the generation and recombination processes [17].

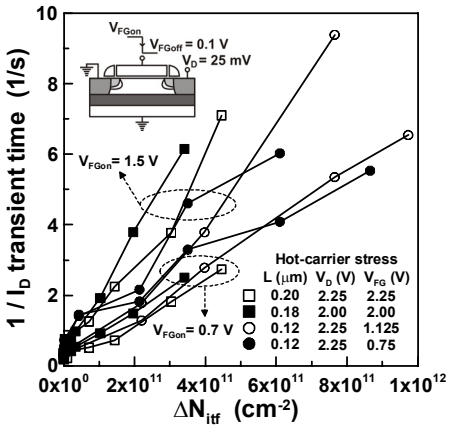

Figure 5. Dependence of the inverse of switch-off I_D transient times (defined as the time to reach either, 90% (undershoot: V_{FGon} = 0.7 V) or 110% (overshoot: V_{FGon} = 1.5 V) of $I_D(t=\infty)$) on the front channel density of interface states generated during the HCD of different nMOSFETs (extracted according to [16]).

5. Thermal annealing effects

In order to gain better insight into the HC-induced damage affecting the FBEs and evaluate its thermal stability, some annealing experiments were carried out by applying different constant temperature annealing phases in the range of 150-250 ºC to previously HC-stressed nMOSFETs. During the thermal anneals, the device terminals were left floating and care was taken in order to get enough cooling of the samples down to room T before the measurements were performed.

Figure 6 shows a typical example of the evolution of the 1st and 2nd peaks of I_D hysteresis for two nMOSFETs subjected to different hot-carrier stress times and subsequent consecutive thermal annealing phases. In figure 7 there are given the corresponding V_{FG} values at which the I_D hysteresis peaks were registered.

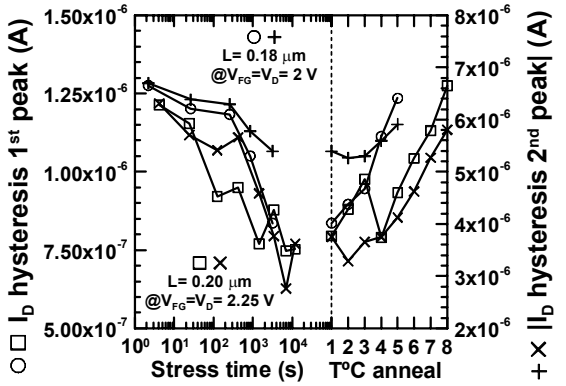

Figure 6. Evolution of I_D hysteresis peaks for two nMOSFETs subjected to HCD and subsequent consecutive thermal annealing phases (TºC anneal for L=0.18 μm device: 1: Just after the HC stress, 2: +1000s @145ºC, 3: +1000s @175ºC, 4: +1000s @195ºC, 5: +1000s @225ºC, 6: +2000s @250ºC). (TºC anneal for L=0.20 μm device: 1: re-measured after HCD and 25 days at room T, 2: +600s @145ºC, 3: +600s @165ºC, 4: +600s @170ºC, 5: +900s @190ºC, 6: +900s @195ºC, 7: +900s @245ºC, 8: +900s @245ºC).

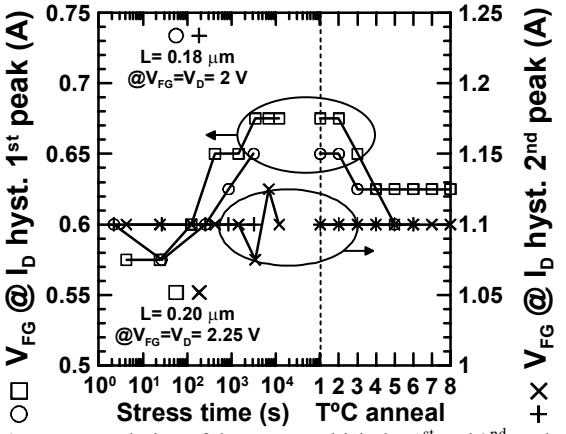

Figure 7. Evolution of the V_{FG} at which the 1st and 2nd peaks of I_D hysteresis are registered for figure 6 nMOSFETs.

From figures 6 and 7, it is clearly observed that unbiased thermal annealing experiments lead to a partial recovery of both, the I_D hysteresis peaks, as well as the V_{FG} values at which the 1st peak is registered. This is further supported by the results from switch-off I_D transients (not shown here), in which both, the steady-state I_D levels, as well as the transients times, were also partially recovered after unbiased thermal annealing experiments. Finally, figure 8 shows the evolution of the extracted front channel oxide trapped charges and interface states densities for figures 6 and 7 nMOSFETs. The thermal annealing experiments were found to give rise to a clear partial recovery of the hot-carrier-induced

damage, thus supporting the existence of a link between the physical hot-carrier-induced damage of the front channel and the reduction of the FBEs.

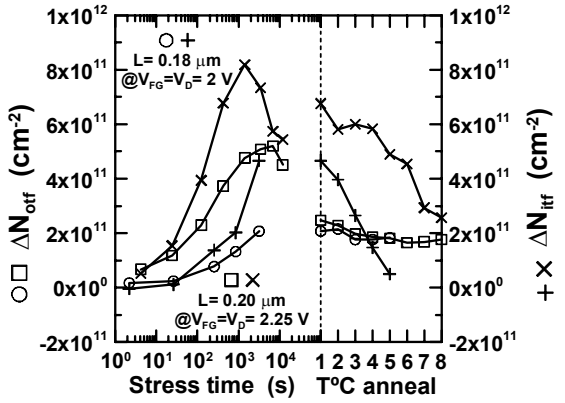

Figure 8. Evolution of front channel oxide trapped charges and interface states densities (N_{otf} and N_{itf}, extracted according to [16]) for figure 6 nMOSFETs.

6. Conclusions

The impact of hot-carrier degradation on ID hysteresis and switch-off ID transients of thin gate oxide floating body PD SOI nMOSFETs is analyzed. An extended characterization of these floating body effects (FBEs) is carried out for a wide range of transistor geometries and bias conditions. The results show a link between the hot-carrier-induced damage of the front channel and the reduction of the FBEs. This is further supported by unbiased thermal annealing experiments in the range of 150ºC-250ºC, which are found to give rise to a partial recovery of the hot-carrier-induced damage and FBEs.

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