**Gate Induced Floating Body Effects in
TiN/SiON and TiN/HfO₂ Gate Stack
Triple Gate SOI nFinFETs**

J. M. Rafi^{1*}, E. Simoen², A. Mercha², N. Collaert², K. Hayama³,
F. Campabadal¹ and C. Claeys^{2,4}

¹Centro Nacional de Microelectrónica (IMB-CNM-CSIC), Campus UAB,
08193 Bellaterra, Spain

²IMEC, Kapeldreef 75, B-3001 Leuven, Belgium

³Kumamoto National College of Technology, 2569-2 Nishigoshi,
Kumamoto 861-1102, Japan

⁴also at KU Leuven, Electr. Eng. Dept., Kasteelpark Arenberg 10,
B-3001 Leuven, Belgium

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^{*}Corresponding author. Tel.: +34 93 5947700, Ext.: 2201; fax: +34 93 5801496.
E-mail address: jmrafi@cnm.es (J. M. Rafi).

Abstract

In this paper, the appearance of gate induced floating body effects in triple gate SOI nFinFETs with TiN/SiON and TiN/HfO₂ gate stacks is investigated. Different floating body effects (FBEs) are found to appear under moderate accumulation back gate bias (V_{BG}) conditions in devices with wide and long enough geometries. In particular, a 2nd peak in the linear transconductance (g_{mf}), associated with electron valence band (EVB) direct tunneling, is observed in TiN/SiON devices for front gate voltages (V_{FG}) around 0.8 V. Interestingly, in spite of showing about two orders of magnitude lower total gate current, a 2nd peak in g_{mf} is also found in TiN/HfO₂ devices for V_{FG} around 1.1 V.

Under the accumulation V_{BG} conditions in which FBEs are observed, front gate switch drain current (I_D) transients are also appreciated. Interestingly, a change in the shape of I_D transients is observed for V_{FG} conditions in which EVB majority carriers are injected into the floating fin. The I_D transients, as well as the 2nd peak of g_{mf} and other FBEs, are found to gradually diminish for strong accumulation V_{BG} conditions or reduced geometry dimensions.

1. Introduction

In recent years, silicon on insulator (SOI) technologies have emerged as serious competitors to bulk silicon technology [1,2]. Owing to device integration requirements and intrinsic resistance constraints of the thin film layers, no film contacts are generally supplied in advanced SOI technologies. If the body is not grounded, so-called floating body effects (FBEs) arise, having a detrimental impact on device performance [1]. FBEs are especially observed in partially depleted (PD) SOI MOSFETs, but they can be also observed on fully depleted (FD) ones when these are operated at accumulation back gate bias (V_{BG}) conditions [2].

In particular, after switching “on” or “off” the front gate, there is no substrate current to quickly adjust the majority carrier density and equilibrium has to be reached through generation-recombination processes. Under these conditions, drain current (I_D) transients are observed [1,3]. Originating from generation and recombination processes, the I_D transients can be a useful tool for assessing the quality of the starting material, process-induced defects or contamination. They have also been used to monitor the degradation of devices subjected to irradiation [4-6] or electrical stress [7].

With the marked decrease in front-gate-oxide thickness, a new type of FBEs associated with gate-body direct tunneling has been identified in linear operation (low drain voltage (V_D)) of SOI n- and p-channel MOSFETs [8,9]. They have a similar influence on device and circuit operation as the classical impact ionization related “kink” effect. The main difference is that for thin SiO_2 -based gate oxides (as thin as 2-2.5 nm),

electron valence band (EVB) tunneling, occurring for a sufficiently large front-gate voltage (V_{FG}) [10], supplies majority carriers that charge the film and increase the body potential, inducing a “kink” in the linear I_D - V_{FG} characteristics and a second peak in the derived front gate transconductance (g_{mf}) [8,9]. Associated with this effect, a change in the gate switch I_D transients shape [8,9,11] and I_D hysteresis [12], as well as an increase of the low-frequency noise [13,14] have been observed.

The presence of these gate-induced FBEs (GIFBEs) [8], leading to history and memory effects could be a limitation for PD SOI CMOS circuits operation [15], however, it has been also reported that the EVB gate-to-body tunneling currents can provide some benefits at circuit level [15-17]. In spite of the above, the significance of these effects was expected to diminish in scaled PD SOI CMOS circuits because of the reduced power supply below the front gate voltages at which the GIFBEs are observed, as well as the possible introduction of alternative gate dielectrics [18], with larger physical thickness, what could prevent or alleviate the EVB tunnelling phenomenon.

Owing to their short channel immunity, superior subthreshold characteristics and low leakage currents, FinFETs are emerging as strong candidates to replace planar MOSFETs for the 32 nm technology node and beyond [19]. In the case of SOI FinFETs, full and partial depletion effects that were found in the past exclusively in FD and PD SOI MOSFETs have been recently found to appear simultaneously in FinFETs with conventional polysilicon/ SiO_2 -based gate stacks [20,21]. In particular, a second peak in the linear transconductance has been observed for long and wide enough fins (above around 0.1 μm) [21], where the devices showed PD behavior. Similarly, the second

peak of the transconductance has been also observed in the case of double gate FinFETs with similar minimum geometries when operated at accumulation V_{BG} conditions, what has been shown, with electrical simulation results, to originate a certain floating body partially depleted region at the bottom of the fin [20].

In this contribution, we investigate the appearance of gate induced floating body effects and front gate switch drain current transients, in triple gate SOI nFinFETs with metal gate (TiN) and SiON or HfO₂ gate dielectrics. Special attention is paid to the impact of the GIFBE on the I_D transients as well as to the accumulation back gate bias and device geometry conditions that enable to measure all these FBEs.

2. Devices and experimental details

The triple gate nFinFETs studied in this work were fabricated using 193nm optical lithography and aggressive trimming of the oxide hard mask in order to reach fin widths down to 25 nm. Devices with metal gate (TiN) and two different gate dielectrics, SiON or HfO₂, giving a total capacitance equivalent thickness (CET) of 1.9 nm were fabricated [22]. Processing was performed on 200 mm UNIBOND wafers, with a final fin height of 60 nm. The devices did not receive a fin implant. The buried oxide thickness was 150 nm. NFinFETs composed of various fins (N_{fin}) with width and length (W_{fin} and L , respectively) ranging from 25 nm to 10 μ m were used for this work. Figure 1 gives a sketch of the studied triple gate nFinFETs, showing their main characteristic features, as well as the nomenclature used for the applied biases.

All current-voltage measurements and gate switch I_D transients were measured using an HP-4156A Parameter Analyzer. During a conventional weak inversion single-gate switch-off experiment, the front gate is switched at $t=0$ s from an ‘on’ gate bias (V_{FGon}) above threshold voltage (V_{Tr}) to an ‘off’ gate bias (V_{FGoff}) in the subthreshold regime [23]. Care was taken with the duration of the ‘on’ bias level, as well as for the conditions between two transient measurements, so that there were no device history (memory) effects. In order to reach equilibrium during the initial “on” step, the duration of the “on” bias level was set to a minimum of 2 minutes. A 640 μ s short integration time, with 0.1 s time step and zero hold and delay times were used for the case of such time measurements. Unless the contrary is indicated, the back gate was grounded ($V_{BG}=0$ V) and the drain bias was kept in the linear operation regime ($V_D=50$ mV) for all measurements. All experiments were carried out in a controlled temperature room with a lightproof and electrically shielded probe station.

3. Gate Induced Floating Body Effects in front channel linear characteristics

3.1 NFinFETs with TiN/SiON gate stack

Figure 2 (a) shows drain current versus front gate voltage (I_D-V_{FG}) and the derived transconductance characteristics ($g_{mf}-V_{FG}$) corresponding to a TiN/SiON gate stack long and wide “FinFET” (nearly planar, when taking into account the fin height of 60 nm), measured at $V_{BG}=0$ V and with a V_{FG} sweep from both, accumulation to inversion

(V_{FG} sweep > 0) and inversion to accumulation (V_{FG} sweep < 0). The corresponding I_D hysteresis, defined as the I_D difference between the two V_{FG} sweep directions is also shown in Fig. 2(a). As it can be easily observed, no appreciable difference is noticed at $V_{BG} = 0$ V bias between the characteristics measured in the two V_{FG} sweep directions, indicating that no FBEs are observed under $V_{BG} = 0$ V condition. On the contrary, when a negative enough V_{BG} is applied to the back gate, a clear difference is observed between the two V_{FG} sweep directions (Fig. 2(b)). In particular, a second peak in the linear transconductance appears for V_{FG} voltages around 0.8 V.

Such a second peak in g_{mf} has been already observed in previous floating body (FB) PD SOI technologies, as well as in FD ones when operated at accumulation V_{BG} conditions [8,9]. The phenomenon is explained as the result of the injection of majority carriers into the floating body by EVB direct tunnelling, occurring at high enough V_{FG} voltages in devices with thin (below around 2.5 nm) SiO_2 -based gate dielectrics [8,9]. The charges introduced into the FB increase the body potential, reducing V_{Tf} and inducing a “kink” in the linear I_D - V_{FG} characteristics and the 2nd peak in the derived g_{mf} . This “linear kink effect” is quite analogous to the classical impact-ionization-related kink effect; however, the main difference is that the excess majority carriers are introduced into the film by gate-body direct tunnelling when V_{FG} surpasses a certain threshold voltage for EVB tunnelling. Consequently, it is observed for small drain biases (V_D) and is, therefore, present in the linear operation regime.

In past planar PD and FD FB SOI technologies, this 2nd peak of g_{mf} has been generally reported to occur for V_{FG} values around 1.1 V or 1.2 V [8,9,24,25]. More recently, in

the case of a FinFET technology with polysilicon gate electrode and 2 nm-thick nitrided SiO₂, the 2nd peak of g_{mf} was found to already appear in wide enough fins for V_{FG} values slightly below 1 V [21]. As a difference to those previous planar and non-planar technologies, in our devices with metal gate (TiN) and SiON gate dielectric, the 2nd peak of g_{mf} already appears here for V_{FG} voltages around 0.8 V.

At this point, it has to be commented that owing to the transient nature of FBEs, the measurement conditions (sweep step and speed) can have a significant impact on the position and magnitude of the 2nd g_{mf} peak. In previous studies, the influence of different sweeping conditions on the GIFBEs has been shown [8,9], as well as the temperature dependence of I_D hysteresis peaks [12]. In particular, by increasing the measurement time, it has been observed that the 2nd peak of g_{mf} can be slightly shifted to lower V_{FG} values, but in all cases these were above $V_{FG} = 1$ V. Since time step issue is a critical point for FB devices, a fixed 20 ms conventional medium integration time was kept for all the I_D double sweeps, which were performed at fixed room T conditions.

Associated with this GIFBE phenomenon, a change in the I_D hysteresis shape is also observed [12]. It is known that I_D hysteresis appears in floating body devices, which originates from generation and recombination processes associated with their FB nature. In this way, the first peak in the I_D hysteresis curve (positive I_D hysteresis peak for V_{FG} around $V_{Tf} \sim 0.4$ V in Figure 2(b)) is associated with the body potential difference between the switch-on and switch-off conditions present during the accumulation to inversion and inversion to accumulation V_{FG} sweeps, respectively [12,7,23]. In the case of an n-channel device, when V_{FG} is swept from accumulation to inversion, holes have

to be recombined to increase the space-charge depletion region for the new V_{FG} condition. While this recombination process occurs, the V_{Tf} of the device is slightly lower than the one that would correspond to such a V_{FG} in steady state condition. On the other hand, when V_{FG} is swept from inversion to accumulation, holes have to be generated to replenish the space-charge region, during this generation process, V_{Tf} is slightly higher than the one corresponding to steady state condition [12,7,23].

Apart from the above conventional 1st peak of I_D hysteresis (positive peak), an EVB-induced 2nd peak of I_D hysteresis (negative peak) is also observed in Figure 2(b) for V_{FG} values around 0.8 V. This is originated by the majority carriers (holes) introduced into the film, which increase the body potential, reducing V_{Tf} and inducing the “kink” in the linear I_D - V_{FG} characteristics. Under this situation, the I_D measured from inversion to accumulation is higher than the I_D measured in the opposite direction, thus originating the negative I_D hysteresis peak in the vicinity of the 2nd peak of g_{mf} .

3.2 NFinFETs with TiN/HfO₂ gate stack

With the aggressive scaling of front gate oxide thickness, the introduction of alternative gate dielectrics with higher permittivity than SiO₂ (high-k) should allow to meet the performance requirements imposed for 45 nm and 32 nm CMOS scaling nodes [19]. The larger physical dielectric thickness should result in a significant reduction of the gate leakage current, while achieving also improved gate capacitance [18]. It was an objective of this study to check the behaviour of the FinFETs with high-k toward the

appearance of GIFBEs. It was expected that the devices with HfO₂ front gate dielectric, with a higher physical thickness and reduced gate currents, would not suffer from GIFBEs.

In this way, an identical characterization was carried out on the nFinFETs with metal gate (TiN) and high-k front gate dielectric (HfO₂). Figure 3 (a) shows I_D - V_{FG} and the corresponding g_{mf} - V_{FG} characteristics for a TiN/HfO₂ gate stack long and wide FinFET (nearly planar), measured at zero back gate bias ($V_{BG}=0$ V) and with V_{FG} sweep from both, accumulation to inversion and inversion to accumulation. The corresponding I_D hysteresis, defined as the I_D difference between the two V_{FG} sweep directions is also shown. As it can be easily appreciated in Fig. 3(a), similar to the case of the TiN/SiON gate stack devices (Fig. 2(a)), no appreciable difference is noticed at $V_{BG}=0$ V bias between the characteristics measured in the two V_{FG} sweep directions, indicating that no FBEs are observed under $V_{BG}=0$ V condition. However, when a negative enough V_{BG} is applied to the back gate, a clear difference is observed between the two V_{FG} sweep directions (Fig. 3(b)). In particular, and surprisingly, a second peak of g_{mf} is also found to appear in these TiN/HfO₂ gate stack nFinFETs for V_{FG} voltages around 1.1 V.

As it could be already appreciated from Figures 2 and 3, it has to be commented here that some fixed difference has been observed between the front gate threshold voltage (V_{Tf}) of these long and wide nFinFETs having SiON or HfO₂ gate dielectrics. In this way, for a wide range of V_{BG} conditions covering from accumulation V_{BG} to positive V_{BG} biases, in which the back channel starts conducting for V_{BG} values around 7 V, originating a subthreshold hump in the front channel characteristics, the V_{Tf} of the HfO₂

devices has been found to be about 0.2 V higher than the one corresponding to their SiON counterparts.

In spite of the obtained results, showing the appearance of the 2nd peak of g_{mf} also in the devices with HfO₂ gate dielectric, it has to be remarked that the total gate current measured at the front gate electrode (I_G) has been found to be significantly lower in the case of the nFinFETs with such alternative gate dielectric. In this way, Figure 4 shows the I_G - V_{FG} characteristics for nFinFETs with TiN/SiON and TiN/HfO₂ gate stack measured under different V_{BG} bias conditions. From the figure, a reduction of about 2 orders of magnitude in I_G is observed for the HfO₂ devices under fixed V_{FG} - V_{Tf} conditions for positive V_{FG} “on” biases. Furthermore, lower I_G levels in HfO₂ devices are also observed in the negative part of the V_{FG} axis, where the gate-induced drain leakage (GIDL) [26] is also significantly reduced. In fact, for the FinFETs with high-k dielectric, there is a significant range of low $|V_{FG}|$ voltages in which the measured I_G current is thought to be below the accuracy of our set-up, what could be estimated to be around 0.1 pA.

Taking into account the significant I_G reduction observed in the devices with HfO₂ gate dielectric, it is interesting to see that the 2nd peak of g_{mf} (GIFBE) is still observed in these FinFETs with a higher physical thickness and different energy band structure. However, it has to be pointed out that the EVB direct tunnelling current giving rise to the GIFBEs is, in the case of thin SiO₂-based gate dielectrics, only a small part of the measured I_G , which in device operation conditions is dominated by the contribution associated to the direct tunnelling of electrons from the channel semiconductor

conduction band to the gate [10,27,28]. To our best knowledge, no results have been published till date about the appearance of a 2nd peak in g_{mf} related to GIFBEs in MOSFETs with alternative high-k gate dielectrics.

In the published literature there are some recent works about modelling or measuring tunneling current through high-k gate dielectric stacks [29,30]. Due to the larger tunneling barrier compared with the conduction band electron barrier for HfO_2/Si , very often the EVB and hole tunneling contributions to the total gate current are neglected [31]. However, some recent works have used the EVB current (also called valence band electron tunneling (VBET)) measured by charge separation through 1.5 nm EOT (equivalent oxide thickness) $HfSiON$ high-k dielectric and submonolayer traces of HfO_2 , to measure the band alignment between the silicon substrate and the polysilicon gate electrode [32,33]. In some other recent work about tunnel current modelling in high-k stacks, it has been pointed that the use of midgap metal electrodes instead of conduction band (E_c) metals in HfO_2/SiO_2 gate dielectric stacks for double gate SOI structures can significantly increase the EVB component to the total gate current [34]. From our results, it seems that such EVB component it is high enough in the studied HfO_2 devices to cause the GIFBE.

3.3 Gate Induced Floating Body Effects: impact of back gate bias

As discussed in Figs. 2 and 3, the GIFBEs (2nd peak of g_{mf}) have been found to appear only under certain accumulation V_{BG} bias conditions. So, our interest here was to

investigate the appearance of such GIFBEs as a function of V_{BG} . In this way, Figure 5 shows the dependence of the magnitude of the 1st and 2nd peaks of g_{mf} and I_D hysteresis on the applied V_{BG} for a TiN/SiON gate stack nFinFET. In general, it has to be stated that for devices with the two types of gate stacks, all FBEs, including also the conventional impact ionization kink in I_D - V_D characteristics (not shown here), have been found to appear only for sufficient accumulation V_{BG} biases ($< \sim -10$ V), what can be thought to be necessary for the creation of a certain partially depleted region, as it has been shown by 2D electrical simulation in a similar case with double gate FD FinFETs [20]. However, for strong accumulation V_{BG} conditions ($< \sim -30$ V) all FBEs are found to gradually diminish. This may be attributed to an electric-field-enhanced generation/recombination at the back channel, similar to that of the conventional front gate GIDL mechanism. In fact, a similar decrease of FBEs with strong accumulation V_{BG} has been also observed for the case of I_D transients in past PD single gate SOI technologies [6].

3.4 Gate Induced Floating Body Effects: dependence on device width and length

So far, all the results presented regarding the appearance of GIFBEs in TiN/SiON and TiN/HfO₂ gate stack devices have been limited to long and wide “FinFETs” (nearly planar, when taking into account the fin height of 60 nm). The reason was to avoid the impact of possible small geometry effects related to isolation and short channel, which are well-known to diminish the FBEs [35,36]. However, at this point we are also interested in evaluating the behavior of real FinFETs of scaled dimensions against the

observed GIFBEs. In this way, Figures 6(a) and 6(b) show the dependence of the 1st and 2nd peaks of g_{mf} and I_D hysteresis on nFinFETs width and length, respectively, for devices with SiON and HfO₂ gate dielectric. The results show a gradual disappearance of the GIFBEs for reduced geometries.

In this way, as shown in Fig. 6(a), the 2nd peak of g_{mf} is only appreciated for devices with wide enough fins ($W_{fin_mask} \geq 0.5 \mu m$) and it is not observed for the narrowest ones. A similar result is found in Fig. 6(b), where the 2nd peak of g_{mf} can be only appreciated for devices with L longer than about $0.1 \mu m$. Regarding to the conventional positive 1st peak of I_D hysteresis, as observed in previous single gate PD-SOI technologies [7], it is appreciated an overall linear dependence of their magnitude with W , thus corroborating their expected scaling with channel current. However, more scattered results are observed for the case of the L dependence, what could be probably attributed to a competition between increased hysteresis values for short L devices with higher I_D and the reduction of FBEs associated with the L reduction. The EVB-induced negative 2nd peak of I_D hysteresis is more sensitive to fin narrowing and it is only appreciated for wide enough fins showing the 2nd peak of g_{mf} .

As a conclusion, it can be said that the observed geometry dependence of the GIFBEs, represented here basically by the 2nd peak of g_{mf} , has shown that they only appear for devices having large enough fin widths and lengths. These results are in agreement with two first previous studies on FinFET technologies with conventional polysilicon gate electrode and SiO₂-based gate oxides, where the 2nd peak of g_{mf} was found to appear only in long and wide fins of similar dimensions [20,21]. In the case of the narrowest

fins, the back gate action enabling the observation of FBEs is minimized due to the lateral coupling between the two vertical sides of the front gate [37,38,39], thus preventing the GIFBEs from appearing. This is also observed as a threshold voltage lowering for the narrowest FinFETs in comparison with the wider ones for a given accumulation V_{BG} [39].

4. Front gate switch-off I_D transients

The analysis of the I_D transients observed on past PD SOI technologies when switching off one of the two MOSFET gates is nowadays a well-established technique for the estimation of silicon film generation and recombination lifetimes [3,40-42]. In order to avoid short and narrow device geometry effects on I_D transients [35,36], long and wide channel transistors (with L and W in the range of 10 μm) are normally used for such lifetime extraction. After switching-off the device, an increase of I_D is generally observed for several tens of seconds until the I_D steady state value ($I_D(t=\infty)$) is reached [23]. It has been shown that for a fixed temperature the measured I_D transient time (defined, for example, as the time to reach 90% of $I_D(t=\infty)$) can be used to extract the effective film generation lifetime (τ_{geff}) of PD SOI MOSFETs, by means of an approximated linear relationship [40,43]. In the case of FinFETs technologies, this may be of special interest, as no film contact is normally available in such structures, thus preventing the use of Zerbst methods based on capacitance versus time measurements.

In view of the results obtained in the previous chapter, where the appearance of GIFBEs has been observed under accumulation V_{BG} conditions in devices with wide and long enough geometries having both, TiN/SiON and TiN/HfO₂ gate stacks, our objective here was to investigate if under such conditions it would be also possible to observe another FBE, I_D transients, when switching the front gate. In particular, it was also of interest to investigate whether these could be or not affected by the GIFBEs, as it was observed in past single gate PD and FD SOI technologies with conventional polysilicon gate and SiO₂-based gate dielectrics [8,9].

As observed for the case of the current-voltage characteristics (ex.: Figs. 2(a) and 3(a)), no I_D transients were measured under $V_{BG}=0$ V condition, however, and interestingly, when accumulation V_{BG} conditions giving rise to the GIFBEs observed in Figs. 2(b) and 3(b) were applied, I_D transients were clearly registered. In this way, Figs. 7(a) and 7(b) show the normalized front gate “switch-off” I_D transients from different V_{FGon} values to a fixed V_{FGoff} in subthreshold regime, measured for $L=10$ μ m nFinFETs with TiN/SiON and TiN/HfO₂ gate dielectrics. First of all, it has to be commented that owing to the existing difference of about 0.2 V in V_{Tf} between the two types of devices (with SiON and HfO₂ gate dielectrics), slightly different conditions were consequently used for the V_{FGoff} values (0.1 V and 0.3 V for devices with SiON and HfO₂ gate dielectrics, respectively), so as to achieve appropriate positions in the subthreshold regime in both cases.

As observed in past PD-SOI technologies [23], from Figs. 7(a) and 7(b), it is clear that for V_{FGon} values up to the corresponding V_{Tf} an I_D undershoot arises. In this way, I_D is

significantly suppressed immediately after the negative V_{FG} step and it gradually increases towards the steady-state value with time. The amplitude of the I_D transients increases with higher negative V_{FG} steps due to the difference in depletion charge between the two bias conditions and the floating-body nature of the device. For V_{FGon} values approaching the region at which the 2nd peak of g_{mf} starts to appear, a gradual decrease in the magnitude of the I_D transients is observed. Finally, for V_{FGon} conditions above the V_{FG} at which the 2nd peak of g_{mf} is observed in Figs. 2(a) and 3(a), a change in the shape of the I_D transients is clearly appreciated. Under this situation, released majority carriers (holes) associated with EVB tunneling from the film to the gate are introduced into the film, causing the inversion of the shape of the I_D transients [8,9,23]. The shape of such I_D overshoot has been found to be in good agreement with switch-on-type I_D transients, in which the gate is pulsed from a V_{FGoff} to a V_{FGon} condition and holes have to be recombined in the floating fin.

From the results in Figs. 7(a) and 7(b), a similar shape for the I_D transients on both types of devices is observed. However, these seem to be a bit smaller or faster for the case of the TiN/HfO₂ gate stack nFinFETs, what could be related to a possible higher surface generation/recombination at the silicon/high-k interface. Moreover, the recombination overshoots are found to be higher in the case of the SiON gate dielectric nFinFETs, what could be associated with a higher EVB injection in comparison with the HfO₂ gate dielectric devices for the applied bias conditions.

4.1 I_D transients: Impact of back gate voltage

As carried out for the case of the 2nd peak of g_{mf} and I_D hysteresis, our interest here was also to investigate the appearance of such I_D transients as a function of V_{BG} . In this way, Figure 8(a) shows the normalized front gate “switch-off” I_D transients from $V_{FGon}= 0.9$ V to $V_{FGoff}= 0.3$ V measured for an nFinFET with HfO_2 gate dielectric at different V_{BG} conditions. Moreover, Fig. 8(b) shows the I_D transient times, defined as the time to reach either, 90% (undershoot) or 110% (overshoot) of steady-state I_D level at V_{FGoff} ($I_D(t=\infty)$) versus V_{BG} for devices with SiON and HfO_2 gate dielectric. From the figures it is clear that similarly to what happens with the other FBEs, the I_D transients are found to appear only for sufficient accumulation V_{BG} biases ($< \sim -10$ V). At the same time, they are found to gradually diminish for strong accumulation V_{BG} conditions.

4.2 I_D transients: Dependence on device width and length

Finally, we were also interested in evaluating the behavior of real FinFETs of scaled dimensions against the observed I_D transients. In this way, Figures 9(a) and 9(b) show the dependences of I_D transient times on fin width (W_{fin}) and length, respectively, for devices with SiON and HfO_2 gate dielectrics. The results show also here a gradual reduction of the I_D transient times for reduced geometries. In this way, from Fig. 9(a) it can be clearly observed that the I_D transients are much faster as fin width is reduced and they can be only observed for devices having a fin width larger than about 0.25 μm . It is also interesting to appreciate that for switch-off conditions with V_{FGon} below the V_{FG} threshold for EVB (90% transient times data in Fig. 9(a)), the generation-shape I_D

transients are often quite similar for the devices having SiON or HfO₂ gate dielectrics. However, in the case of V_{FGon} conditions giving rise to EVB injection of majority carriers into the fin (110% transient times data in Fig. 9(a)), as already seen in Figs. 7(a) and 7(b), the transient times are larger in the case of SiON devices. This seems the result of less EVB injection in the case of the HfO₂ gate dielectric devices under the range of bias conditions applied. Finally, from Fig. 9(b), showing the dependence of the transient times with device length, it is seen that they rapidly vanish and disappear for devices with channel lengths in the range around 0.1 or 0.2 μm . As in previous SOI technologies, it is inferred that the use of large area devices, to avoid small area effects, may continue to be useful for modelling and extraction of effective lifetimes, what can be of interest for quality assessment or degradation purposes.

5. Conclusions

The appearance of gate induced floating body effects (GIFBEs) in triple gate SOI nFinFETs with TiN/SiON and TiN/HfO₂ gate stacks has been investigated. Different floating body effects (FBEs) have been found to appear under moderate accumulation back gate bias (V_{BG}) conditions in devices with wide and long enough geometries. In particular, a 2nd peak in the linear transconductance (g_{mf}), associated with electron valence band (EVB) direct tunneling, has been observed in TiN/SiON devices for front gate voltages (V_{FG}) around 0.8 V. Interestingly, in spite of showing about two orders of magnitude lower total gate current, a 2nd peak in g_{mf} has been also observed in the TiN/HfO₂ devices for V_{FG} voltages around 1.1 V.

Under the accumulation V_{BG} conditions in which FBEs are observed, front gate switch I_D transients have been also appreciated. Interestingly, a change in the shape of front gate switch-off I_D transients has been appreciated for V_{FG} conditions in which EVB majority carriers are injected into the floating fin. The I_D transients, as well as the 2nd peak of the linear transconductance and other FBEs, have been found to gradually diminish for strong accumulation V_{BG} conditions or reduced geometry dimensions.

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FIGURE CAPTIONS

- Fig. 1:** Sketch of the studied triple gate nFinFETs, showing their main characteristic features, as well as the nomenclature used for the applied biases.
- Fig. 2:** I_D and corresponding g_{mf} versus V_{FG} , measured at (a) $V_{BG} = 0$ V and (b) $V_{BG} = -15$ V, from accumulation to inversion (V_{FG} sweep > 0) and inversion to accumulation (V_{FG} sweep < 0) for an $L = 10$ μm nFinFET with five 3 μm -wide fins and TiN/SiON gate stack. The corresponding I_D hysteresis, defined as the I_D difference between the two V_{FG} sweep directions, is also shown.
- Fig. 3:** I_D and corresponding g_{mf} versus V_{FG} , measured at (a) $V_{BG} = 0$ V and (b) $V_{BG} = -20$ V, from accumulation to inversion (V_{FG} sweep > 0) and inversion to accumulation (V_{FG} sweep < 0) for an $L = 10$ μm nFinFET with five 3 μm -wide fins and TiN/HfO₂ gate stack. The corresponding I_D hysteresis, defined as the I_D difference between the two V_{FG} sweep directions, is also shown.
- Fig. 4:** Gate current measured at the front gate terminal (I_G) versus V_{FG} for TiN/SiON and TiN/HfO₂ gate stack $L = 10$ μm nFinFETs with five 3 μm -wide fins, subjected to different V_{BG} conditions.
- Fig. 5:** Dependence of the 1st and 2nd peaks of g_{mf} and I_D hysteresis on V_{BG} for an $L = 10$ μm nFinFET with five 3 μm -wide fins and TiN/SiON gate stack.
- Fig. 6:** (a) Dependence of the 1st and 2nd peaks of g_{mf} and I_D hysteresis on fin mask width ($W_{fin} \approx W_{fin_mask} - 0.12$ μm), for devices with SiON and HfO₂ gate dielectric. (b) Dependence on device length (L).

Fig. 7: Normalized front gate “switch-off” I_D transients from different V_{FGon} values to a fixed V_{FGoff} in subthreshold regime, measured for an $L = 10 \text{ } \mu\text{m}$ nFinFET with five $3 \text{ } \mu\text{m}$ -wide fins and (a) SiON and (b) HfO_2 gate dielectric. ($I_D(t=\infty)$ = steady state I_D level at $V_{FG} = V_{FGoff}$ condition).

Fig. 8: (a) Normalized front gate “switch-off” I_D transients from $V_{FGon} = 0.9 \text{ V}$ to $V_{FGoff} = 0.3 \text{ V}$ measured for an $L = 10 \text{ } \mu\text{m}$ nFinFET with five $3 \text{ } \mu\text{m}$ -wide fins at different V_{BG} conditions. ($I_D(t=\infty)$ = steady state I_D level at $V_{FG} = V_{FGoff}$ condition). (b) I_D transient times (defined as the time to reach either, 90% (undershoot) or 110% (overshoot) of $I_D(t=\infty)$) versus V_{BG} for devices with SiON and HfO_2 gate dielectric.

Fig. 9: (a) I_D transient times (defined as the time to reach either, 90% (undershoot) or 110% (overshoot) of $I_D(t=\infty)$) versus fin width (W_{fin}) for devices with SiON and HfO_2 gate dielectric. (b) Dependence on device length (L).

Fig. 1

Fig. 2(a)

Fig. 2(b)

Fig. 3(a)

Fig. 3(b)

Fig. 4

Fig. 5

Fig. 6(a)

Fig. 6(b)

Fig. 7(a)

Fig. 7(b)

Fig. 8(a)

Fig. 8(b)

Fig. 9(a)

Fig. 9(b)