Progressive Degradation of TiN/SiON and TiN/HfO_2 Gate Stack Triple Gate SOI nFinFETs Subjected to Electrical Stress

J. M. Rafí[1*], E. Simoen[2], A. Mercha[2], N. Collaert[2]

F. Campabadal[1] and C. Claeys[2,3]

[1]Centro Nacional de Microelectrónica (IMB-CNM-CSIC), Campus UAB,

08193 Bellaterra, Spain

[2]IMEC, Kapeldreef 75, B-3001 Leuven, Belgium

[3]also at KU Leuven, Electrical Engineering Department, Kasteelpark Arenberg 10,

B-3001 Leuven, Belgium

[*]Corresponding author. Tel.: +34 93 5947700, Ext.: 2201; fax: +34 93 5801496

Electronic mail: jmrafi@cnm.es

ABSTRACT

In this contribution, we analyze first results about the impact of electrical stress on triple gate SOI nFinFETs with metal gate (TiN) and SiON or HfO_2 gate dielectrics, with particular emphasis on the roles of fin width and back gate polarization. A similar progressive degradation of the characteristics is observed for both types of gate dielectric devices. An increasing degradation with reducing fin width is observed for a certain range of wide fin devices (between about 3 μm and 130 nm), what could be attributed to a higher contribution of corner effects or lower quality side surfaces. However, the narrowest triple gate FinFETs with geometries around the nominal values of this technology (70 nm long and 30 nm wide fins) show reduced degradation with electrical stress.

Under the studied experimental conditions, no clear impact on device degradation is observed for different back gate bias conditions applied during electrical stress. A typical dielectric breakdown mode characterized by a sudden decrease in drain current, accompanied by a significant increase in front gate current, is observed quite often in devices subjected to strong or long stress conditions. From the analysis of the encountered post-breakdown source/drain asymmetries, it is inferred that most of such catastrophic failures under $V_{FG} = V_D$ stress regime may correspond to gate-to-source dielectric breakdown.

I. INTRODUCTION

Multi-gate MOSFETS (MuGFETs), such as FinFETs [1,2], have been identified as one of the most promising device architectures to replace planar MOSFETs for the 32 nm technology node and beyond [3,4]. Processing on silicon on insulator (SOI) substrates provides further advantages in terms of device performance and scalability, thus emerging as a serious competitor to classical bulk silicon technology [2,5].

In recent times, much attention is paid to different characterization and reliability aspects of MuGFETs device architectures [2,6]. In particular, hot-carrier reliability [7] and bias temperature instabilities (N/PBTI) [8] are potential issues. The damage generated under electrical stress is commonly believed to result in charge trapping in the gate dielectrics and interface-state generation at the Si/dielectric interfaces.

In the case of SOI technologies, the presence of floating body effects and concurrent mechanisms like self-heating can make device degradation a more complex subject [7,9]. For conventional partially-depleted (PD) and fully-depleted (FD) planar SOI technologies, the existence of the thick buried oxide and its additional interface can also introduce certain constraints and coupling effects may appear between the damage generated at the different gates [10]. In this way, opposite channel injection phenomena and hot-carrier-induced degradation of the thick buried oxide have been reported [11,12].

For SOI MuGFETs, a good lateral gate control and suppression of substrate bias effects has been observed for narrow fin devices [13]. However, it has recently been demonstrated that

the front-channel characteristics of short-channel triple gate FinFETs may still be susceptible to V_{BG}, with a significant degradation of their linear transconductance [14]. This has been explained in terms of a V_{BG}-induced series resistance increase leading to performance degradation in such short channel FinFETs.

As a difference to some previous studies with conventional polysilicon/SiO_2-based gate stack MuGFETs, we study here first results about degradation effects caused by electrical stress on the characteristics of metal gate (TiN) triple gate SOI nFinFETs with either SiON or HfO_2 gate dielectrics. Moreover, to evaluate the possible generation of damage in the buried oxide, the impact of different back gate bias conditions during electrical stress is also investigated.

II. DEVICES AND EXPERIMENTAL DETAILS

The triple gate nFinFETs studied in this work were fabricated using 193nm optical lithography and aggressive trimming of the oxide hard mask in order to reach fin widths down to 25 nm. The devices got TiN/SiON or TiN/HfO_2 gate stacks with 1.9 nm capacitance equivalent thickness (CET) [15].Processing was performed on 200 mm UNIBOND wafers, with buried oxide thickness and final fin height of 150 nm and 60 nm, respectively. The devices did not receive a fin implant. NFinFETs composed of various fins (N_{fin}) with width (W_{fin}) ranging from 25 nm to 10 μm and lengths (L) from 50 nm to 10 μm were used for this work. Figure 1 gives a sketch of the studied triple gate nFinFETs, showing their main characteristic features, as well as the nomenclature used for the applied biases.

All current-voltage and electrical stress experiments were carried out by means of an HP-4155B Parameter Analyzer. For the electrical stress, the transistors were subjected to constant-voltage conditions, with drain biases (V_D) above the power supply voltage associated to this technology (V_{DD}= 1 V). The degradation was mainly evaluated through the analysis of front and back channel input characteristics (I_D vs. V_{FG} and I_D vs. V_{BG}, respectively), which were regularly measured between the different stress phases. Owing to the floating body nature of the devices under study, special attention was paid to ensure that steady-state conditions were reached before performing the measurements after the different electrical stress phases. A set of different front and back channel parameters, among them the front gate threshold voltage (defined as $V_{Tf}\equiv V_{FG}$ @I_D= 0.01 W/L μA), were used as primary degradation monitors. Unless the contrary is indicated, the back gate (chuck contact to wafer substrate) was grounded (V_{BG}= 0 V) and the drain bias was kept in the linear operation regime (V_D= 50 mV) for all measurements. All experiments were carried out in a lightproof and electrically shielded setup.

III. DEGRADATION OF CURRENT-VOLTAGE CHARACTERISTICS

A set of transistors were subjected to electrical stress under different drain voltages (V_D) and at V_{FG} = V_D condition, which has been reported to arise as the worst V_{FG} regime for hot-carrier degradation in recent floating-body planar and FinFET SOI technologies [7,16]. Moreover, in order to evaluate any possible impact of the buried oxide and back gate bias

on the nature and localization of the electrically-induced damage, different back gate voltage (V_{BG}) conditions were also considered for the electrical stresses.

Fig. 2(a) shows typical I_D-V_{FG} and derived transconductance characteristics (g_{mf}-V_{FG}) corresponding to an HfO_2 gate dielectric nFinFET subjected to electrical stress. A progressive degradation of the characteristics has been observed for both, SiON and HfO_2 gate dielectric devices, with clear I_D and transconductance reductions (Fig. 2(a)). Associated with this degradation mode, a positive shift of V_{Tf} is also registered, which is generally accompanied by an increase in the subthreshold slope of the I_D-V_{FG} characteristics. As expected, device degradation is found to be accelerated for reduced L and increased stress bias conditions. During the different stress and measurement phases, special attention has been paid to ensure that the gate current (I_G) doesn't show any significant increase that could be associated to front gate dielectric breakdown of the devices (Fig. 2(b)).

In order to investigate the localization of the generated damage, front and back channel input characteristics (I_D vs. V_{FG} and I_D vs. V_{BG}), as well as output (I_D vs. V_D) characteristics, were measured before and after some electrical stress experiments, both, interchanging and without interchanging the source for the drain relative to the configuration in which the stress was performed. It was expected that if the hot-carrier-induced damage occurred in a localised region close to the drain junction, its electrical effect would be partially masked by the drain depletion region, making the device asymmetric to source-drain interchange after the electrical stress [10]. As expected, no asymmetry was observed after stress in the low-V_D (linear) front (Fig. 2(a) and (b)) and back channel input characteristics. Moreover, even for

the case of the output characteristics reaching higher V_D biases, such a post-stress asymmetry was not clearly observed under the studied experimental conditions.

In order to minimize the impact of any possible perimeter effect on the electrical stress degradation behavior, a first stage of our studies was concentrated on relatively wide and planar-like devices (W_{fin} large taking into account the 60 nm fin height, Fig. 1). In a second phase, our studies focused on real triple gate FinFETs with the nominal geometries of this technology (L and W_{fin} around 70 nm and 30 nm, respectively).

The degradation of the different front channel characteristics parameters has been found to be similar for SiON and HfO_2 gate dielectric devices. As a difference to some early studies with conventional polysilicon/SiO_2-based gate stack MuGFETs [7], an increasing degradation with reducing fin width has been observed here for the wide-fin range between 3 μm and 130 nm. This can be observed in Figures 3(a) and 3(b), showing the degradation of parameter I_{Dlin} (defined as $I_D@V_{FG}$= 1 V, V_D= 50 mV) and maximum linear transconductance (g_{mfmax}) for SiON and HfO_2 gate dielectric devices of various wide-fin geometries subjected to different electrical stress conditions. A similar behavior has been explained in terms of a higher contribution of corner effects and lower quality side surfaces in the case of narrow bulk FinFETs [17].

In our case, however, the analysis on narrower triple gate FinFETs with geometries around the nominal values of this technology (L and W_{fin} of 70 nm and 30 nm, respectively) shows reduced degradation with electrical stress. This can be observed in Figures 4(a) and 4(b), showing the degradation of parameter I_{Dlin} and front gate threshold voltage shift (ΔV_{Tf}) for

various SiON and HfO_2 gate dielectric nFinFETs subjected to different electrical stress conditions. A similar improved hot-carrier resistance has been explained in terms of either, a lower electric field distribution in narrow fin geometries [7], or the effect of an increased parasitic series resistance with W_{fin} reduction, what would lead to a lower effective potential drop near the stressed drain junction [18].

In contrast to some previous partially-depleted (PD) and fully-depleted (FD) planar SOI technologies, in which opposite channel injection phenomena and hot-carrier-induced degradation of the thick buried oxide have been reported [11,12], under the studied experimental conditions, no clear impact on device degradation has been observed for different back gate bias conditions applied during electrical stress. Only under the highest $V_{FG}=V_D$ and V_{BG} bias conditions some slight back channel degradation has been appreciated in wide fin devices. In this way, it has to be remembered also that the effectiveness of substrate to front gate coupling rapidly diminishes with fin narrowing [13], and the back channel threshold voltage becomes very high for narrow fin devices [13].

IV. DIELECTRIC BREAKDOWN AND CURRENT-VOLTAGE CHARACTERISTICS

An important issue to mention from our present electrical stress study has been related to front gate dielectric breakdown of the devices. In this way, a quite common pattern observed under strong or long stress conditions has been found to be associated with a sudden decrease in drain current, what is also accompanied by a significant increase in front gate current. A typical example of such behavior can be observed in Figure 5(a), where the

degradation of I_D measured during stress time ($I_{Dstress}$) is plotted for various nFinFETs subjected to different electrical stress conditions. As it can be easily appreciated, a sudden decrease in drain current, indicated as "breakdown" in Fig. 5(a), is registered for one of the plotted devices. As indicated, this is generally accompanied by a significant increase in the corresponding measured gate current (Fig. 5(b)). After such a sudden event, if the electrical stress is continued, the $I_{Dstress}$ and $I_{Gstress}$ values may still experience some further changes towards either, a progressively higher breakdown level or, on the other hand, they may show some degree of recovery (as it can be appreciated in Figs. 5(a) and 5(b) case). In some devices, only a subtle increase of I_G is detected, but a significant loss of the channel conductance properties (I_D and g_{mf}) is registered. To some extent, it is believed that the limited fin volume and floating body nature of these devices could play some role in this behavior. For example, in past PD and FD planar SOI technologies, it has been observed that a relatively small electron valence band tunnel conduction through an ultrathin gate dielectric may be responsible for a certain injection of majority carriers into the floating film, which results in significant macroscopic phenomena observed in the I-V characteristics [19].

Some additional properties about a dielectric breakdown event can be drawn from the characteristics measured after electrical stress. In this way, for example, Figure 6(a) shows I_D-V_D characteristics measured for Fig. 5 HfO_2 gate dielectric nFinFET before electrical stress and after its dielectric breakdown (DB) registered during the electrical stress (Figs. 5(a) and 5(b)). As it can be observed, the device showed normal I_D-V_D characteristics before electrical stress. Only a slight asymmetry between normal and reverse source/drain configuration was detected at the higher levels of current, what is attributed to some slight series resistance asymmetry that may occur sometimes in some of these narrowest fin devices (W_{fin}= 30 nm).

As easily appreciated in Fig. 6(a), after dielectric breakdown the gate loses the control of the channel conduction and this is mostly governed by the applied V_D. This is better appreciated in Fig. 6(b), where the corresponding front gate current I_G-V_D characteristics are plotted. The increased I_G levels after breakdown show different trends depending on the measurement condition. In this way, the value and direction of I_G remains independent of the applied V_D for the case of a measurement performed in normal S/D configuration. On the other hand, the measured I_G is strongly dependent on V_D (in both, value and direction) when the measurement is performed interchanging the drain for the source relative to the configuration in which the electrical stress was performed. From Fig. 6(b) results it can be inferred that the breakdown event occurred between the gate and source terminals. In this way, in normal S/D configuration, the breakdown position is located near the source and I_G is only dependent on V_{FG} applied to the gate, but not on V_D. On the other hand, for reverse S/D configuration, the breakdown position becomes located near the measuring drain and, both, the direction and value of I_G are basically depending on V_{FG}-V_D bias difference. For low V_D conditions, the measured I_G values are similar for normal and reverse S/D measuring configurations. It has to be commented at this point that most of the breakdown events observed during the electrical stress of the devices correspond to a similar pattern to Figures 5 and 6 results. This seems in agreement with the expected dielectric breakdown behavior for electrical stress under the studied $V_{FG} = V_D$ regime, where the higher gate-to-channel vertical electric field corresponds to the portion of the channel near to the stressing source junction.

IV. CONCLUSION

The impact of electrical stress on triple gate SOI nFinFETs with metal gate (TiN) and SiON or HfO_2 gate dielectrics has been investigated, with particular emphasis on the roles of fin width and back gate polarization. A similar progressive degradation of the characteristics has been observed for both gate stack devices. An increasing degradation with reducing fin width has been observed for a certain range of wide fin devices (between about 3 μm and 130 nm), what could be explained in terms of a higher contribution of corner effects or lower quality side surfaces. However, the narrower triple gate FinFETs with geometries around the nominal values of this technology (L and W_{fin} of 70 nm and 30 nm, respectively) show reduced degradation with electrical stress. This could be attributed to a lower electric field distribution in narrow fin geometries or to the effect of an increased parasitic series resistance with W_{fin} reduction.

Under the studied experimental conditions, no clear impact on device degradation has been observed for different back gate bias conditions applied during electrical stress. A typical dielectric breakdown mode characterized by a sudden decrease in drain current, accompanied by a significant increase in front gate current, has been observed quite often in devices subjected to strong or long stress conditions. From the analysis of the encountered post-breakdown source/drain asymmetries, it has been inferred that most of such catastrophic failures under $V_{FG} = V_D$ stress regime may correspond to gate-to-source dielectric breakdown.

ACKNOWLEDGEMENTS

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FIGURE CAPTIONS

Fig. 1: Sketch of the studied triple gate nFinFETs, showing their main characteristic features, as well as the nomenclature used for the applied biases.

Fig. 2: (a) Drain current (I_D) and corresponding front gate transconductance (g_{mf}) characteristics measured for an HfO_2 gate dielectric nFinFET before hot-carrier degradation and after different stress times at $V_D = V_{FG} = 1.25$ V and $V_{BG} = -10$ V stress bias condition. (b) Corresponding front gate current (I_G) vs. V_{FG} characteristics. The results corresponding to a measurement performed after stress interchanging the source for the drain relative to the configuration in which the stress was performed are also shown (reverse S/D).

Fig. 3: (a) Degradation of parameter I_{Dlin} (defined as $I_D@V_{FG}= 1$ V, $V_D= 50$ mV) for SiON gate dielectric nFinFETs of various wide fin geometries subjected to different electrical stress conditions. (b) Degradation of maximum linear transconductance value (g_{mfmax}) for HfO_2 gate dielectric nFinFETs of various wide fin geometries subjected to different electrical stress conditions.

Fig. 4: Degradation of parameter I_{Dlin} (defined as $I_D@V_{FG}= 1$ V, $V_D= 50$ mV) and front gate threshold voltage shift (ΔV_{Tf}) for various (a) SiON and (b) HfO_2 gate dielectric nFinFETs with narrow fin geometry ($W_{fin} = 30$ nm) subjected to different electrical stress conditions.

Fig. 5: (a) Degradation of I_D measured during stress time ($\Delta I_{Dstress}/I_{Dstress0}$) for various nFinFETs subjected to different electrical stress conditions (where $\Delta I_{Dstress}$ = $I_{Dstress}$ - $I_{Dstress0}$ and $I_{Dstress0}$ correspond to the $I_{Dstress}$ value just at the beginning of the electrical stress). (b) Corresponding evolution of I_G measured during stress ($I_{Gstress}$).

Fig. 6: (a) I_D-V_D characteristics measured for an HfO_2 gate dielectric nFinFET before electrical stress and after its dielectric breakdown (DB) when subjected to an electrical stress at V_D = V_{FG} = 1.2 V and V_{BG} = +10 V stress bias condition. (b) Corresponding front gate current I_G-V_D characteristics. The measurements are shown for normal and reverse source/drain configuration, in which the source is interchanged for the drain relative to the configuration in which the stress is performed.

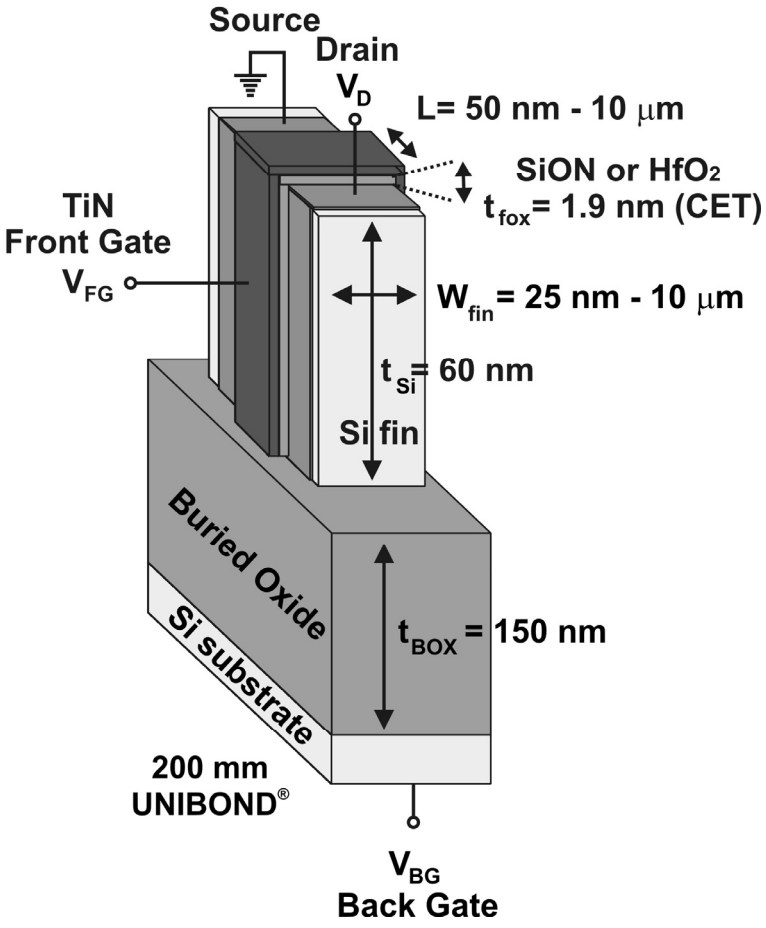
Source
Drain
V_D
L= 50 nm - 10 μm
SiON or HfO_2
t_{fox}= 1.9 nm (CET)
TiN
Front Gate
V_{FG}
W_{fin}= 25 nm - 10 μm
t_{Si}= 60 nm
Si fin
Buried Oxide
Si substrate
t_{BOX} = 150 nm
200 mm
UNIBOND®
V_{BG}
Back Gate

Fig. 1

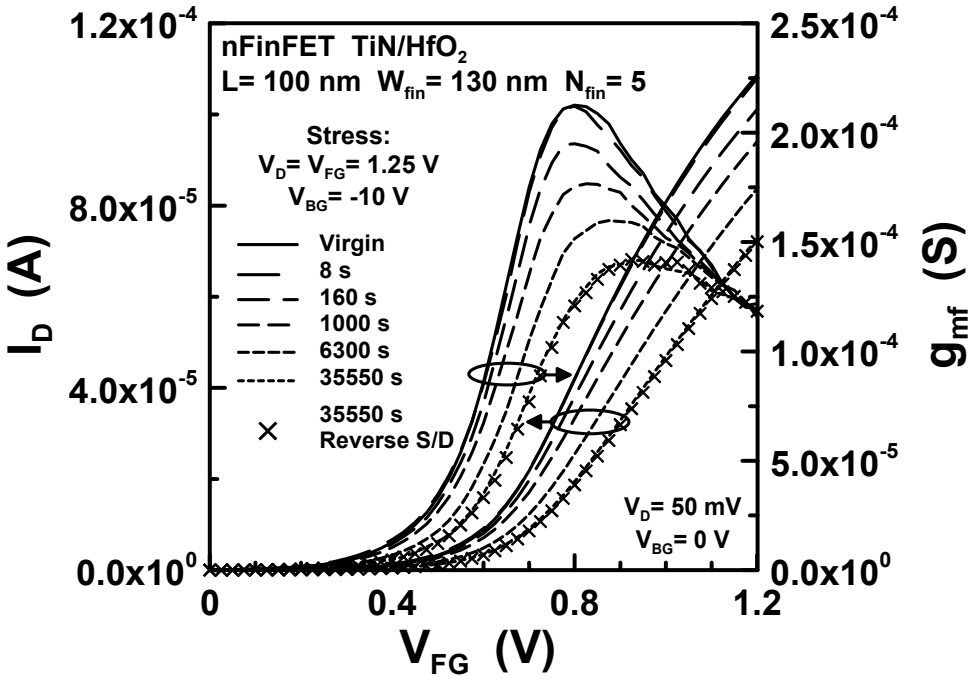
nFinFET TiN/HfO2
L= 100 nm Wfin= 130 nm Nfin= 5
Stress:
VD= VFG= 1.25 V
VBG= -10 V
Virgin
8 s
160 s
1000 s
6300 s
35550 s
35550 s
Reverse S/D
VD= 50 mV
VBG= 0 V
ID (A)
gmf (S)
VFG (V)
1.2x10-4
8.0x10-5
4.0x10-5
0.0x100
2.5x10-4
2.0x10-4
1.5x10-4
1.0x10-4
5.0x10-5
0.0x100
0
0.4
0.8
1.2

Fig. 2(a)

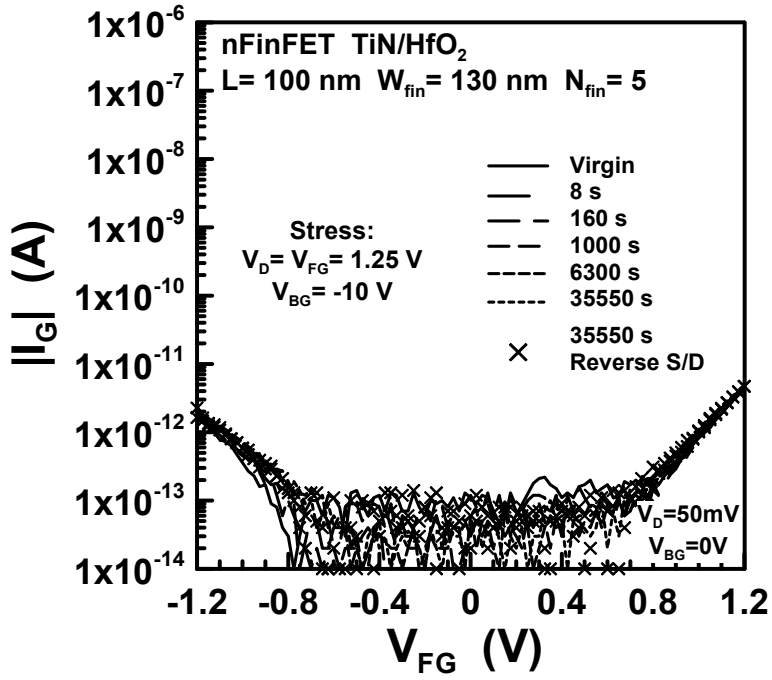
nFinFET TiN/HfO2
L= 100 nm Wfin= 130 nm Nfin= 5
Stress:
VD= VFG= 1.25 V
VBG= -10 V
Virgin
8 s
160 s
1000 s
6300 s
35550 s
35550 s
Reverse S/D
VD=50mV
VBG=0V
|IG| (A)
VFG (V)
1x10-6
1x10-7
1x10-8
1x10-9
1x10-10
1x10-11
1x10-12
1x10-13
1x10-14
-1.2
-0.8
-0.4
0
0.4
0.8
1.2

Fig. 2(b)

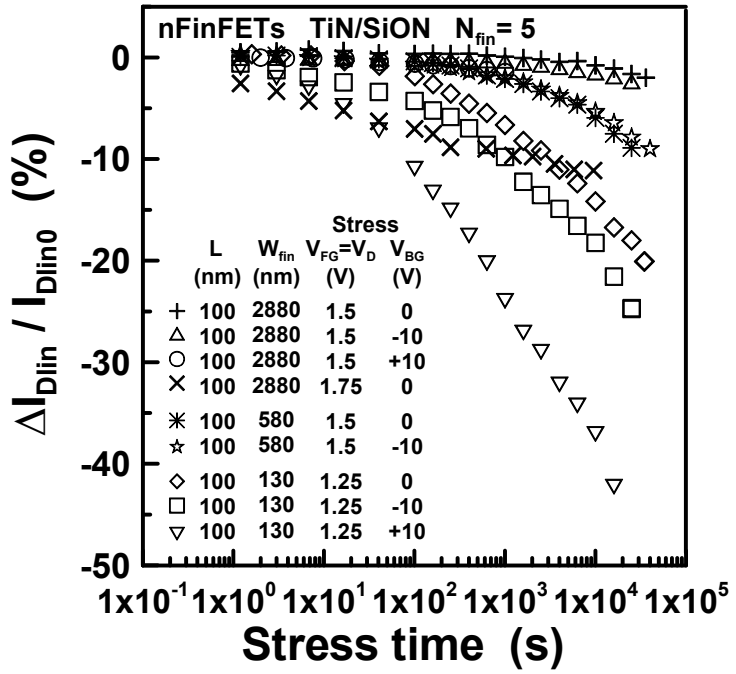
nFinFETs TiN/SiON N_fin= 5
ΔI_Dlin / I_Dlin0 (%)
Stress time (s)
Stress
L (nm) W_fin (nm) V_FG=V_D (V) V_BG (V)
100 2880 1.5 0
100 2880 1.5 -10
100 2880 1.5 +10
100 2880 1.75 0
100 580 1.5 0
100 580 1.5 -10
100 130 1.25 0
100 130 1.25 -10
100 130 1.25 +10

Fig. 3(a)

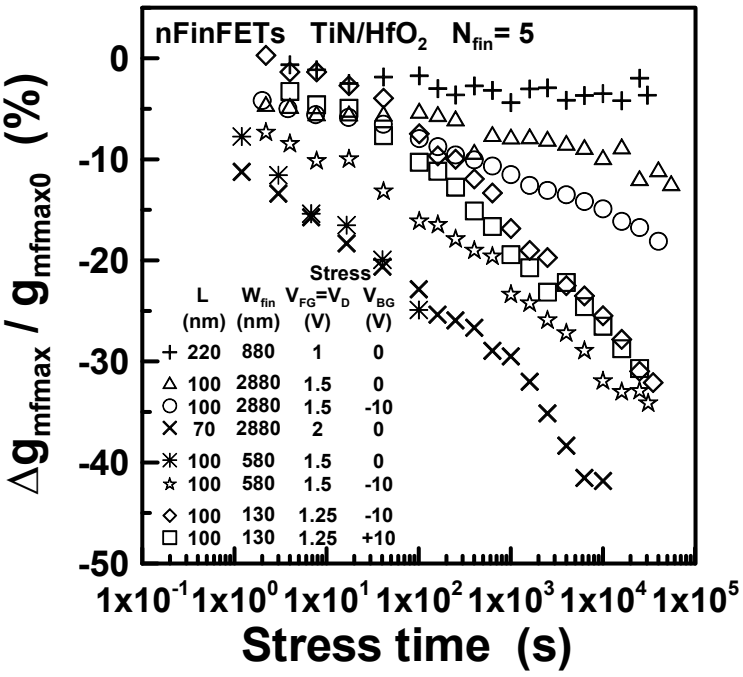
nFinFETs TiN/HfO2 N_fin= 5
Δg_mfmax / g_mfmax0 (%)
Stress time (s)
Stress
L (nm) W_fin (nm) V_FG=V_D (V) V_BG (V)
220 880 1 0
100 2880 1.5 0
100 2880 1.5 -10
70 2880 2 0
100 580 1.5 0
100 580 1.5 -10
100 130 1.25 -10
100 130 1.25 +10

Fig. 3(b)

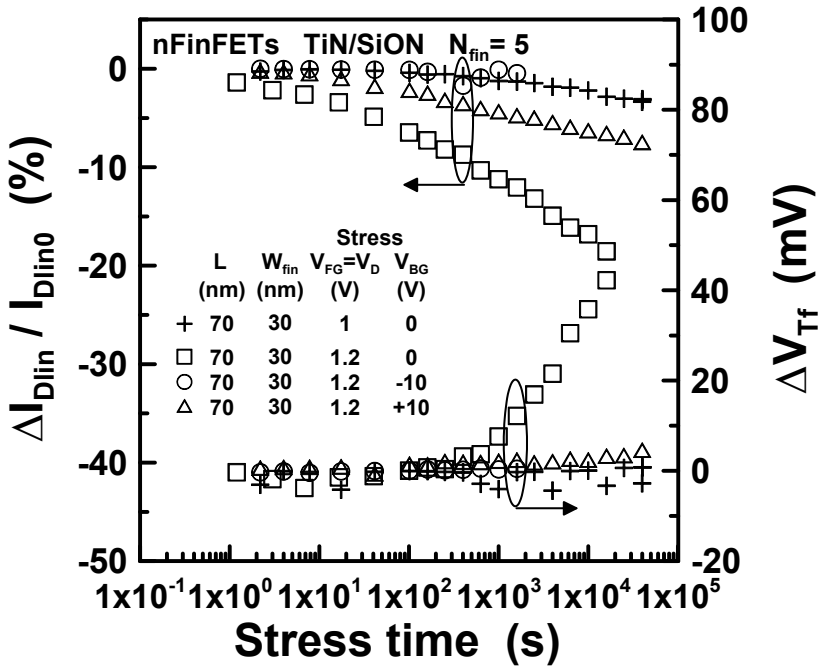
nFinFETs TiN/SiON N_{fin} = 5
Stress
L (nm) W_{fin} (nm) V_{FG}=V_D (V) V_{BG} (V)
70 30 1 0
70 30 1.2 0
70 30 1.2 -10
70 30 1.2 +10
$\Delta I_{Dlin} / I_{Dlin0}$ (%)
ΔV_{Tf} (mV)
Stress time (s)

Fig. 4(a)

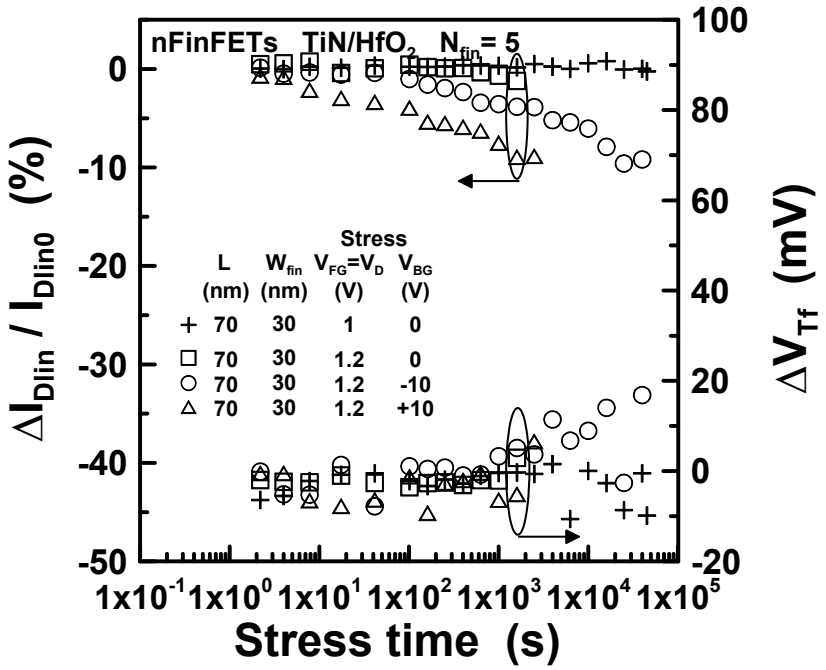
nFinFETs TiN/HfO_2 N_{fin} = 5
Stress
L (nm) W_{fin} (nm) V_{FG}=V_D (V) V_{BG} (V)
70 30 1 0
70 30 1.2 0
70 30 1.2 -10
70 30 1.2 +10
$\Delta I_{Dlin} / I_{Dlin0}$ (%)
ΔV_{Tf} (mV)
Stress time (s)

Fig. 4(b)

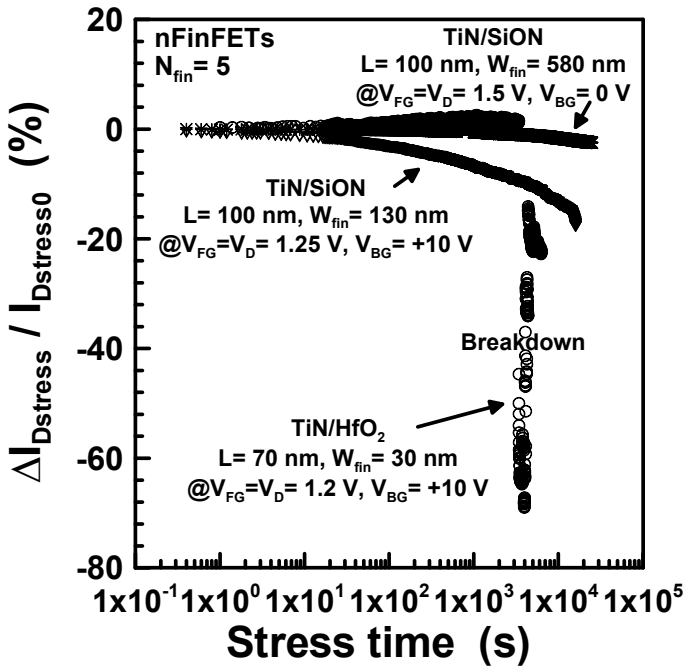
nFinFETs
N_fin= 5
TiN/SiON
L= 100 nm, W_fin= 580 nm
@V_FG=V_D= 1.5 V, V_BG= 0 V
TiN/SiON
L= 100 nm, W_fin= 130 nm
@V_FG=V_D= 1.25 V, V_BG= +10 V
Breakdown
TiN/HfO2
L= 70 nm, W_fin= 30 nm
@V_FG=V_D= 1.2 V, V_BG= +10 V
ΔI_Dstress / I_Dstress0 (%)
Stress time (s)

Fig. 5(a)

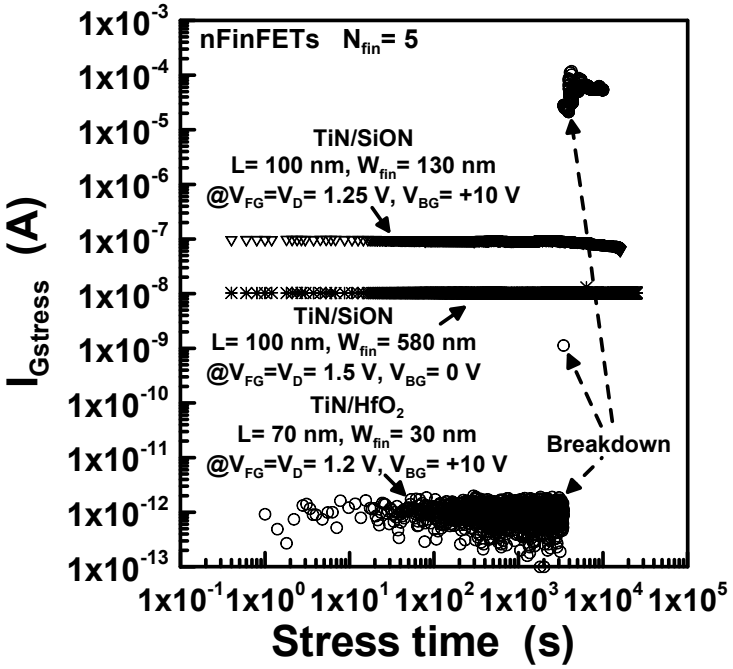
nFinFETs N_fin= 5
TiN/SiON
L= 100 nm, W_fin= 130 nm
@V_FG=V_D= 1.25 V, V_BG= +10 V
TiN/SiON
L= 100 nm, W_fin= 580 nm
@V_FG=V_D= 1.5 V, V_BG= 0 V
TiN/HfO2
L= 70 nm, W_fin= 30 nm
@V_FG=V_D= 1.2 V, V_BG= +10 V
Breakdown
I_Gstress (A)
Stress time (s)

Fig. 5(b)

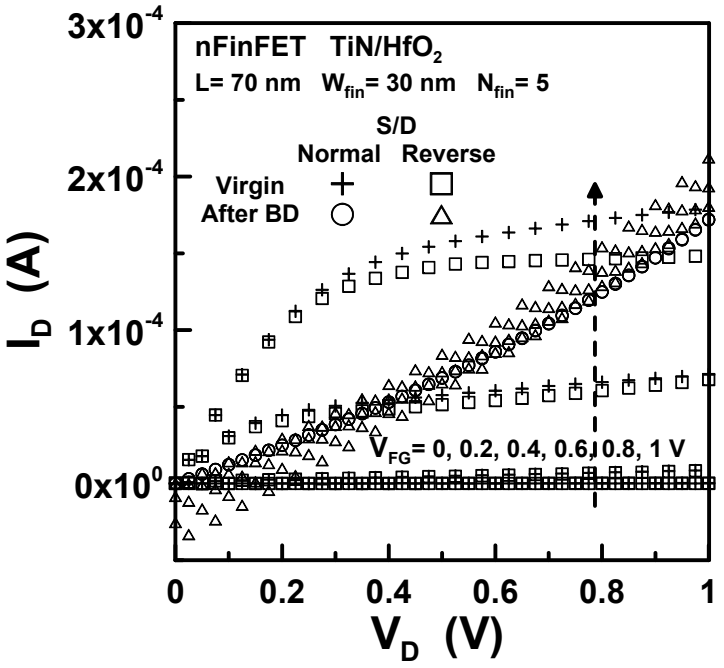
nFinFET TiN/HfO2
L= 70 nm Wfin= 30 nm Nfin= 5
S/D
Normal Reverse
Virgin
After BD
VFG= 0, 0.2, 0.4, 0.6, 0.8, 1 V
ID (A)
VD (V)
3x10-4
2x10-4
1x10-4
0x100
0
0.2
0.4
0.6
0.8
1

Fig. 6(a)

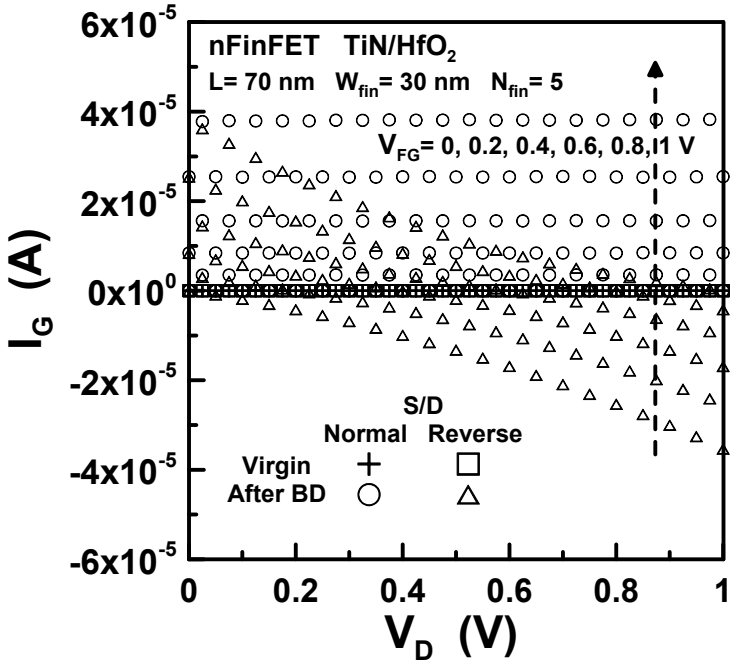
nFinFET TiN/HfO2
L= 70 nm Wfin= 30 nm Nfin= 5
VFG= 0, 0.2, 0.4, 0.6, 0.8, 1 V
S/D
Normal Reverse
Virgin
After BD
IG (A)
VD (V)
6x10-5
4x10-5
2x10-5
0x100
-2x10-5
-4x10-5
-6x10-5
0
0.2
0.4
0.6
0.8
1

Fig. 6(b)