Deposition Temperature and Thermal Annealing Effects on the Electrical Characteristics of Atomic Layer Deposited Al_2O_3 Films on Silicon

J. M. Rafí*, M. Zabala, O. Beldarrain and F. Campabadal

Institut de Microelectrònica de Barcelona (CNM-CSIC)

Campus UAB, 08193 Bellaterra, Spain

*Corresponding author. Tel.: +34 93 5947700, Ext.: 2201; fax: +34 93 5801496

Electronic mail: joanmarc.rafi@imb-cnm.csic.es

Abstract

Atomic layer deposition (ALD) of Al_2O_3 is of interest for a wide range of micro-nanoelectronic applications, where the electrical properties of the deposited layers can be strongly affected by deposition conditions and post-deposition treatments. In this work, a mercury-probe capacitance-voltage characterization is carried out on Al_2O_3 films deposited on silicon by ALD at different temperatures and subjected to various thermal treatments in N_2 ambient. Effective positive charges located at the semiconductor/dielectric interface are encountered for the films deposited at the lowest temperature (100ºC). Positive V_{fb} shifts are always registered after the different thermal annealing conditions studied; however, the impact of the thermal treatments is found to be different depending on the deposition temperature. A significant negative charges build-up is observed after a 30 minutes anneal at 450ºC, where improved surface passivation properties are achieved. Interestingly, the hysteresis, as well as the V_{fb} shifts, clearly diminish for higher deposition temperatures or after a thermal anneal. However, the highest temperature treatments (≥800ºC) result in significant interface states generation. Finally, exploratory experiments about the stability of the Al_2O_3 layers under UV-light irradiation (in the 200 nm-300 nm wavelengths range) show that this can be responsible for a significant degradation of their electrical characteristics.

Introduction

Al_2O_3 is a material of interest for a wide range of applications because of its unique material properties. Owing to its high dielectric constant (k ~ 9) and high band gap energy (~ 9 eV), it has been commonly investigated as a gate dielectric layer for complementary metal oxide semiconductor (CMOS) technologies or dynamic random access memories (DRAM) [1-3]. In addition, Al_2O_3 attracts interest in a variety of emerging technologies such as nanodevices [4,5], organic light emitting devices [6], as a surface passivation layer on high-efficiency crystalline silicon solar cells [7], and for a variety of microelectromechanical systems due to its excellent mechanical properties [8].

For all these applications, it becomes necessary to have a deposition technique capable of producing high-quality films with good dielectric properties, large area uniformity and conformality and accurate control of thickness. To this respect, atomic layer deposition (ALD) of Al_2O_3 has been shown to meet most of these demands.

The electrical properties of ALD-deposited layers can be strongly affected by deposition conditions and post-deposition treatments [1,2]. Whereas some of these treatments can have a deleterious effect, others may be useful to improve the characteristics of the as-deposited layers. For instance, it has recently been reported that a post-deposition thermal treatment of ALD Al_2O_3 layers allows reaching low surface recombination velocities, and the inclusion of such layers in solar cells can lead to higher conversion efficiencies [7,9]. In particular, recent studies indicate that the best surface passivation is obtained for ALD deposition temperatures around 200ºC and after a low temperature annealing treatment (in

the range of 400ºC) [10]. Contrary to silicon oxide grown or nitride deposited layers, which tend to be positively charged, the passivation properties of ALD Al_2O_3 layers have been attributed to a field-enhanced passivation originated from a high density of negative charges appearing after the thermal treatments [11-13].

The integration of new materials and processes requires some preliminary studies and fast characterization techniques to optimize process parameters related to the deposition conditions and post-deposition annealing treatments. To perform such electrical measurements, the use of a mercury-probe is an alternative to the more costly fabrication of patterned MOS test structures [14-16].

In this work, a mercury-probe capacitance-voltage (C-V) characterization is carried out on Al_2O_3 films deposited on silicon by ALD. The studied dielectric layers, with number of ALD cycles between 20 and 200, and ellipsometry measured thickness in the range around 2 nm to 20 nm, were deposited at different temperatures and they were subjected to various post-deposition thermal treatments in N_2 atmosphere. The layers are analyzed in terms of flat-band voltage, presence of hysteresis and characteristics of the measured C-V curves. Surface passivation properties are evaluated by means of microwave photoconductance decay recombination lifetime measurements and exploratory experiments about degradation of the Al_2O_3 layers subjected to UV-light irradiation (in the 200 nm-300 nm wavelengths range) are also presented.

Experimental

The starting material used in this work was one-side polished p-type Czochralski (CZ) (100) silicon, with a resistivity (ρ) between 0.1 Ω·cm and 1.4 Ω·cm and a wafer thickness of 500 μm. The wafers were cut into 1.8 cm x 1.6 cm pieces and these were cleaned in a 2:1 H_2SO_4:H_2O_2 solution, followed by an HF dip, deionized water rinse and nitrogen blow dry. Al_2O_3 layers were immediately deposited on the polished wafer side by using an atomic layer deposition Savannah 200 system from Cambridge NanoTech. The precursors used were H_2O and trimethylaluminum (TMA). One ALD cycle was the sequence of an H_2O pulse of 15 ms, a purge in N_2 for 5 s, a TMA pulse of 50 ms and a purge in N_2 for 5 s. In order to evaluate the impact of processing conditions on the properties of the Al_2O_3 ALD films, different layer thicknesses were deposited, with number of ALD cycles ranging from 20 to 200, at 100ºC, 200ºC and 300ºC deposition temperatures. After Al_2O_3 deposition, the samples were subjected to different thermal annealing treatments in N_2 ambient, as indicated in Table 1.

The film thickness of each sample was obtained by a Rudolph Research Auto EL ellipsometer, using indexes of refraction of 1.60, 1.63 and 1.64 for Al_2O_3 layers deposited at 100ºC, 200ºC and 300ºC, respectively, as determined by means of refractive index measurements performed on slightly thicker (30 nm) layers. In order to evaluate the electrical characteristics of the deposited layers, capacitance versus voltage (C-V) and accumulation capacitance versus frequency (C-w) measurements were carried out by using an HP-4192 A LF Impedance Analyzer. The corresponding conductance versus voltage (G-V) and conductance versus frequency (G-w) characteristics were also recordered. Electrode

contact to the dielectric layers was achieved by means of a Materials Development Corp. MDC 802B mercury-probe set-up, with an Hg drop contact diameter of 760 μm (contact area = $4.54 \cdot 10^{-3}$ cm^2).

The C-V measurements were performed for both, inversion to accumulation and accumulation to inversion voltage sweeps. The hysteresis was defined as the difference between the extracted flat-band voltages (V_{fb}) corresponding to the two voltage sweeps (hysteresis = $V_{fb_inv_to_acc}$-$V_{fb_acc_to_inv}$). V_{fb} has been extracted from the maximum capacitance in accumulation (C_{max}) and the minimum capacitance in depletion (C_{min}), considering C_{max} as a direct measurement of the dielectric capacitance (C_{ox}). C_{min} coupled with C_{ox} is used to determine the substrate capacitance in depletion, allowing an evaluation of the substrate doping level. The total capacitance in flat band condition is then calculated from the substrate capacitance in flat band condition and C_{ox}. An estimation of the effective trapped charge density (N_{eff}), defined as a fixed charge located at the insulator/silicon interface, has been obtained from the comparison of the extracted V_{fb} values with the ones expected for an ideal MOS structure with 4.5 eV metal work function, corresponding to the mercury drop contact [17]. An estimation of the interface states density (N_{it}) has been obtained from the peak of the parallel conductance derived from the measured conductance versus voltage curves [17].

In order to investigate the passivation effectiveness of the layers, an Al_2O_3 film was deposited on both sides of some silicon substrates and microwave photoconductance decay (μW-PCD) minority carrier recombination lifetime (τ_r) measurements at low injection level were carried out by using a Semilab WT-1000 setup [18].

Results and Discussion

As-deposited Al_2O_3 layers

Layer thickness: Ellipsometry results. Figure 1 shows ellipsometry-measured thickness versus number of ALD cycles plots for Table 1 as-deposited samples. Note that for each temperature and number of ALD cycles, three or four samples were simultaneously processed, so that the results also indicate the uniformity of the deposition process. From the figures, good linear deposition kinetics were obtained for the different studied conditions (as-deposited data in Fig. 1), being the slope of the linear fit, the growth rate. The results obtained indicate growth rates of 0.09, 0.11 and 0.10 nm/cycle for depositions at 100ºC, 200ºC and 300ºC, respectively, i.e., a maximum growth rate seems to exist at deposition temperatures around 200ºC, a result that is in accordance with previously reported Al_2O_3 deposition with ALD [19].

Capacitance-Voltage characterization with Hg-probe system. In order to evaluate the electrical characteristics of the atomic layer deposited Al_2O_3 films, C-V characteristics were measured with a Hg-probe on the as-deposited dielectric layers of Table 1. In a Hg-MOS structure the metal gate contact is formed by a mercury drop in contact with the dielectric layer [14,15]. Despite of the fact that this structure allows fast screening evaluation of dielectric layers, some limitations may affect the measured characteristics. In particular, a strong attenuation of the accumulation capacitance as a function of the measurement

frequency is observed. Recently, an analytical electrical model for capacitance-voltage measurements with Hg-probe has been presented [14,15]. This approach considers the series association of the substrate impedance, the high-k dielectric impedance, and an additional impedance modelling the interfacial layer between the dielectric and the mercury-drop contact [14,15]. Based on the results from capacitance measurements at a wide range of frequencies, in the present work all the C-V characterizations are carried out at a measurement frequency of 1 kHz, so as to limit the impact of Hg-probe-related parasitic effects.

Figure 2 shows an example of C-V (and corresponding G-V) characteristics measured for as-deposited and thermal annealed Al_2O_3 layers. As it can be appreciated, some hysteresis is generally observed for the as-deposited Al_2O_3 layers.

Figures 3 and 4 show the extracted flat-band voltages and hysteresis values for different Al_2O_3 thickness layers deposited at 100ºC, 200ºC and 300ºC. From Figure 3, a general trend to more positive V_{fb} values for higher deposition temperatures has been obtained for the as-deposited layers. Regarding the V_{fb} dependence on the layer thickness, a different behaviour is observed depending on the deposition temperature. For the case of the Al_2O_3 layers deposited at 100ºC (Figure 5), a linear dependence is obtained suggesting the presence of dominant positive charges located at the semiconductor/dielectric interface, with an estimated effective trapped charge density (N_{eff}) of $2 \cdot 10^{12}$ cm^{-2} [20]. On the other hand, no clear V_{fb} versus layers thickness dependences have been appreciated for the Al_2O_3 films deposited at 200ºC and 300ºC, indicating that the charges are more distributed within the layers for these dielectrics deposited at higher temperatures [20].

Furthermore, from Fig. 4, C-V curve hysteresis is found to clearly diminish with increasing deposition temperature and the highest hysteresis values (above 500 mV) have been observed for the as-deposited Al_2O_3 layers at 100ºC. On the other hand, no clear trends between the magnitude of the hysteresis and the layer thickness have been observed.

With regard to the origin of the instabilities in the Al_2O_3 layers, in previous studies on similar TMA-H_2O-based Al_2O_3 layers, it has been found that the concentration of H impurity increases for low ALD deposition temperatures [10,21-23], suggesting that the hysteresis in the Al_2O_3 layers could be attributed to an excess of hydrogen and/or hydroxyl groups in the layers [2]. Unfortunately, information about the composition and impurity profiling of the films studied here are not available and studies about this would be needed.

Impact of thermal annealing

Layer thickness: Ellipsometry results. After subjecting some of the samples to the different thermal annealing conditions described in Table 1, the thickness of the dielectric layers was re-measured by ellipsometry under the same conditions as previously described. The results showed that the effect of a high temperature anneal depends on the initial thickness of the film. This can be easily appreciated in Figure 1 plots, where it is observed that for the thickest films (thickness > 12 nm) the annealing process at temperatures greater than 650ºC leads to a decrease in thickness. Although the reduction in thickness increases as the annealing temperature increases, this reduction process somehow saturates, since no

significant difference in thickness is obtained between the results of annealing at 950 and 1000ºC (Fig. 1(b)). The phenomenon of thickness reduction can be attributed to a densification of the films, as already suggested to occur for such TMA and H_2O-based Al_2O_3 ALD films subjected to similar high-temperature conditions [24]. Contrary to what is observed for thick layers, in the case of thin films, an increase of thickness, in the range of 1-2 nm, was registered for the thinnest Al_2O_3 layers (especially for 20 cycles and 40 cycles samples) subjected to high temperature treatments (Fig. 1). This effect, that is especially significant for the longest and highest temperature annealing conditions, can be associated with an oxidation of the silicon interface occurring for those thin layers. The growth of such an interface layer during thermal anneal of ALD Al_2O_3 films has been studied by means of different spectroscopic techniques [25]. The results for high-k layers deposited on silicon and subjected to high temperature treatments under inert ambient have also revealed the contribution of oxygen present in the deposited high-k films in this process [26,27].

In summary, from the analysis of the results obtained from ellipsometry measurements, it is concluded that a thermal annealing at 450ºC does not lead to significant thickness changes in the ALD Al_2O_3 layers, but higher temperature treatments do change either the thickness of the ALD film, the interfacial layer or both.

Capacitance-Voltage characterization with Hg-probe system. In order to investigate the impact of post-deposition thermal treatments on the electrical properties of the ALD-deposited layers, C-V characteristics were also measured on the Al_2O_3 films subjected to the different thermal annealing conditions described in Table 1. Some typical C-V characteristics measured for 80 ALD cycles Al_2O_3 layers deposited at 300ºC and thermally annealed for 30

min at 450ºC, 30 min at 650ºC and 30 min at 800ºC have been also plotted in Figure 2(a), where shifts of the C-V curves are appreciated after the different thermal treatments. The corresponding extracted N_{eff} values are $-3.8\cdot10^{12}$ cm^{-2}, $-5\cdot10^{12}$ cm^{-2}, $-6.7\cdot10^{12}$ cm^{-2} and $-6.8\cdot10^{12}$ cm^{-2} for the as-deposited condition and the increasing temperature anneals studied, respectively. Interestingly, a hump in the C-V curve and an associated peak in the corresponding conductance curve (Fig. 2(b)) have been observed for all the samples subjected to the highest thermal annealing treatments (1 h at 1000ºC, 1h at 950ºC and 30 min at 800ºC). These humps and peaks can be attributed to the loss mechanism due to interface trap capture and emission of carriers and is related to the interface states density [17]. From this analysis, the extracted N_{it} values for Figure 2 samples are $6\cdot10^{10}$ cm^{-2}, $6.5\cdot10^{10}$ cm^{-2}, $2\cdot10^{11}$ cm^{-2} and $1.2\cdot10^{12}$ cm^{-2} for the as-deposited condition and the increasing temperature anneals studied, respectively. A small discretization in the measurements took place in the accumulation region for the case of Fig. 2 measurements what was caused by a change of scale in the capacitance meter, when capacitances were higher than 2.2 nF. However, this has no impact in all the discussed results (V_{fb}, hysteresis, conductance peaks, etc...), which belong to a lower capacitance region below accumulation.

Figure 3 also shows V_{fb} results versus annealing conditions for the whole set of Al_2O_3 layers deposited at 100ºC, 200ºC and 300ºC. Positive V_{fb} shifts have been always registered after the different thermal annealing conditions studied; the impact of such thermal treatments, however, has been found to be significantly different depending on the deposition temperature. Interestingly, the layers deposited at lower temperature are found to experience higher V_{fb} changes after the thermal anneal. For example, while a 30 min anneal at 450ºC is responsible for the highest positive V_{fb} shifts of the layers deposited at 100ºC, it

has only minor effects on the layers deposited at 300ºC. Furthermore, while a 30 min anneal at 650ºC performed on 100ºC-ALD layers generally gives rise to lower V_{fb} values than a 30 min anneal at 450ºC, this is just the opposite in the case of ALD layers deposited at 300ºC. Similarly, for layers deposited at 100ºC, a 30 min anneal at 800ºC always leads to lower V_{fb} values than a 30 min anneal at 650ºC, however, for layers deposited at 300ºC, a 30 min anneal at 800ºC leads to similar or lower V_{fb} values than a 30 min anneal at 650ºC.

Interestingly, a higher variation of V_{fb} after thermal anneal has been observed for the case of the thicker Al_2O_3 layers. In particular, this is especially significant for the case of layers deposited at 100ºC and after their 30 min anneal at 450ºC, where the V_{fb} dependence on the layer thickness shows a good linear dependence (Fig. 5). This suggests the presence of negative charges placed at the semiconductor/dielectric interface, with an estimated effective trapped charge density (N_{eff}) around $-5.7 \cdot 10^{12}$ cm^{-2} [20]. Some linear correlations have been also observed for the cases of the Al_2O_3 layers deposited at 100ºC and after their 30 min anneals at 650ºC or 800ºC (Fig. 5), with estimated N_{eff} values around $-2.4 \cdot 10^{12}$ cm^{-2} and $-0.9 \cdot 10^{12}$ cm^{-2}, respectively. On the contrary, no V_{fb} dependence on layer thickness has been appreciated for the Al_2O_3 films deposited at 300ºC that underwent a 30 min anneal at 450ºC, suggesting that the charges are more distributed within the layers for these conditions. With respect to the Al_2O_3 films deposited at 300ºC and subjected to thermal treatments of 30 min at 650ºC and 30 min at 800ºC, N_{eff} values around $-2.5 \cdot 10^{12}$ cm^{-2} are deduced from their V_{fb} versus layer thickness dependences. Finally, for the case of the Al_2O_3 films deposited at 200ºC, some linear correlation between V_{fb} and layer thickness has been only appreciated after 1 h anneal at 1000ºC, giving an estimated effective trapped charge density around $-6 \cdot 10^{12}$ cm^{-2}.

As it is shown in Figure 2, the hysteresis generally diminishes after the studied thermal annealing treatments (Figure 4). A significant hysteresis (in the range of 200 mV) only remains after 30 min annealing at 800ºC for the thickest layers (200 and 150 cycles) deposited at 100ºC. No clear trends exist between the magnitude of the hysteresis and the layer thickness. The reduction of the hysteresis with the thermal treatments could be explained by a reduction of the excess of hydrogen and/or hydroxyl groups in the layers after the thermal treatments [2,28]. The growth of a certain silicon oxide interface layer between the silicon and the dielectric may also play a role on the observed hysteresis. In particular, lower hysteresis values have been reported for Al_2O_3 and HfO_2 ALD high-k dielectrics with thicker interface layers, being this attributed to a reduced charge tunnelling mechanism between the substrate and existing traps in the high-k dielectric [29-31]. However, from Figure 4 and Figure 1 results, no direct relation between the reduction of the hysteresis and the possible increase of interface layer thickness after the different thermal treatments has been appreciated.

Finally, it is known that contamination caused by mobile charges is responsible for hysteresis phenomena affecting the C-V characteristics of MOS structures. In the case of SiO_2-based dielectrics, this is generally studied by means of bias-temperature stress experiments, where the ion drift of the most common ion species in SiO_2 (Na^+, Li^+ and K^+) becomes significant during the applied high-temperature steps (typically in the range of 200ºC to 300ºC) [17,32]. In the present study, the samples were always measured at room temperature and processed under CMOS-line cleanroom conditions, where no detectable contamination by mobile charges is observed in SiO_2 dielectrics. Moreover, it has to be

pointed out that under the hypothetical presence of dominant mobile charge effects (caused either by positive or negative ions), clockwise hysteresis, instead of the normally encountered counter clockwise hysteresis would be expected [17,33].

Surface passivation properties

In order to investigate the passivation effectiveness of the Al_2O_3 layers deposited by ALD, 500 μm-thick CZ (100) silicon wafer pieces of two-side polished p-type (with ρ between 10 $\Omega\cdot$cm and 20 $\Omega\cdot$cm), one-side polished p-type (with ρ between 0.1 $\Omega\cdot$cm and 1.4 $\Omega\cdot$cm) and one-side polished n-type CZ Si (with ρ between 1 $\Omega\cdot$cm and 12 $\Omega\cdot$cm), were cleaned using exactly the same sequence described above and passivated for one or both wafer sides with a 11 nm (100 cycles) Al_2O_3 layer deposited at 200ºC. C-V measurements were carried out with the Hg-probe set-up on the samples with passivation on one side, and μW-PCD minority carrier recombination lifetime (τ_r) measurements were carried out on the samples with both sides passivated; the main results are given in Figure 6.

As expected, from Figure 6(a), low τ_r values (in the range of 10 μs or 20 μs) are measured on the non-passivated, as-received materials, having high recombination velocities on the front and back bare surfaces [34]. The τ_r values significantly increase after the passivation with 11 nm Al_2O_3 on both sides. However, as observed in Figure 6(a), the recombination lifetime is found to further increase after a thermal anneal of 30 min at 450ºC. These results can be explained from a field-enhanced passivation originated by a high density of negative charges appearing after the thermal treatments [7,11-13]. This is supported by the shift of the C-V

characteristics and their extracted N_{eff} values (Figure 6(b)). Interestingly, in spite of its higher C-V positive shift, a thermal treatment of 30 min at 800ºC is not so effective for surface passivation. This could be explained by the hump appearing on the C-V characteristics, and its associated peak in the conductance (Fig. 6(c)), which is found to be associated with a significant interface state generation (N_{it}) under such thermal annealing condition.

Impact of UV-light irradiation

Apart from the thermal treatments, a negative charge build-up was earlier reported for the case of Al_2O_3 layers grown on silicon by pyrolysis of aluminium-tri-isopropoxide and subjected to non-ionizing ultraviolet irradiation [35]. The effect was attributed to photoinjection of electrons from the silicon valence band over the silicon/insulator barrier into the aluminium oxide film. A threshold energy of 4.1 eV (λ = 302 nm) was required for this internal photoinjection process. As a result of the UV-induced negative fixed charges, and whereas the interface states density remained low, the passivation properties of the Al_2O_3 layers on either p-type or n-type silicon could be improved via enhancement of accumulation or inversion conditions, respectively [35].

In order to evaluate the possible effects of UV light irradiation on our studied Al_2O_3 layers deposited by ALD, samples of p-type CZ Si with an 11 nm (100 cycles) Al_2O_3 layer deposited at 200ºC were exposed to UV light. C-V measurements were carried out with the Hg-probe set-up before and after the irradiations. UV exposure was performed for different times with a UVAPRINT 40CE equipment (Dr Hönle GmbH, Germany [36]) provided with a UVC

lamp (with maximum emission spectra in the 200 nm-300 nm wavelengths range) and a parabolic reflector. The samples were placed on a holder inside the chamber with the 11 nm Al_2O_3 layer facing the UV light and at a distance of about 15 cm of the lamp. Special care was taken to wait enough time for UV-light stabilization before opening the shutter for irradiation, as well as in allowing thermal stabilization of the samples before C-V measurements were performed after UV-irradiation.

Figure 7(a) shows the C-V curves measured for a typical sample before and after different ultraviolet light exposure times. As previously commented for Figure 4 results, the non-irradiated (0 min UV) C-V curve in Fig. 7(a) shows a slight hysteresis, typical of such 200ºC-deposited Al_2O_3 layers. Interestingly, a significant positive shift and stretch-out of the C-V curve, as well as an increase of the hysteresis, is already observed after 2 min UV-light irradiation. A hump in the depletion region of the C-V characteristics and a peak in the corresponding conductance curves (not shown here) are also observed. Under the experimental conditions studied, the UV-irradiation-induced degradation increases with UV-light exposure times, with a subsequent positive effective charge trapping and a progressive interface states generation (Fig. 7(b)). Finally, saturation of the generation of damage is observed for long UV-light irradiation times.

Conclusions

The effects of different deposition temperatures and thermal anneal in N_2 ambient on the electrical characteristics of atomic layer deposited (ALD) Al_2O_3 films on silicon have been

analyzed by means of mercury-probe capacitance-voltage characterization. Effective positive charges located at the semiconductor/dielectric interface have been encountered for the films deposited at the lowest temperature (100ºC). More positive flat-band voltages (V_{fb}) and more distributed charges within the films have been obtained for higher deposition temperatures (200ºC and 300ºC). Positive V_{fb} shifts have been always registered after the different thermal annealing conditions studied; however, the impact of such thermal treatments has been found to be significantly different depending on the deposition temperature. A significant negative charges build-up has been observed after the 450ºC thermal treatments, where improved surface passivation properties have been achieved. Interestingly, the hysteresis, as well as the V_{fb} shifts, clearly diminish for higher deposition temperatures or after a thermal anneal. However, the highest temperature treatments (≥800ºC) have been found to lead to significant interface states generation. Finally, exploratory experiments have shown that UV-light irradiation (in the 200nm-300nm wavelengths range) can be responsible for a significant degradation of the electrical characteristics of the studied Al_2O_3 ALD layers.

Acknowledgements

This work has been partially funded by the Spanish Ministry of Science and Innovation through project TEC2008-06698-C02-01.

References

[1] G.D. Wilk, R.M. Wallace, and J.M. Anthony, Journal of Applied Physics **89**, 5243 (2001).

[2] J. Robertson, Rep. Prog. Phys. **69**, 327 (2006).

[3] E. Gerritsen, N. Emonet, C. Caillat, N. Jourdan, M. Piazza, D. Fraboulet, B. Boeck, A. Berthelot, S. Smith, and P. Mazoyer, Solid-State Electronics **49**, 1767 (2005).

[4] S.K. Kim, Y. Xuan, P.D. Ye, S. Mohammadi, J.H. Back, and M. Shim, Applied Physics Letters **90**, 163108 (2007).

[5] T. Helbling, C. Hierold, C. Roman, L. Durrer, M. Mattmann, and V.M. Bright, Nanotechnology **20**, 434010 (2009).

[6] S.J. Yun, Y.-W. Ko, and J.W. Lim, Applied Physics Letters **85**, 4896 (2004).

[7] B. Hoex, S.B.S. Heil, E. Langereis, M.C.M. van de Sanden, and W.M.M. Kessels, Applied Physics Letters **89**, 042112 (2006).

[8] T.M. Mayer, J.W. Elam, S.M. George, P.G. Kotula, and R.S. Goeke, Applied Physics Letters **82**, 2883 (2003).

[9] J. Schmidt, A. Merkle, R. Brendel, B. Hoex, M.C.M. van de Sanden, and W.M.M. Kessels, Progress in Photovoltaics: Research and Applications **16**, 461 (2008).

[10] G. Dingemans, M.C.M. van de Sanden, and W.M.M. Kessels, Electrochemical and Solid-State Letters **13**, H76 (2010).

[11] G. Agostinelli, A. Delabie, P. Vitanov, Z. Alexieva, H.F.W. Dekkers, S. De Wolf, and G. Beaucarne, Solar Energy Materials & Solar Cells **90**, 3438 (2006).

[12] B. Hoex, J. Schmidt, P. Pohl, M.C.M. van de Sanden, and W.M.M. Kessels, Journal of Applied Physics **104**, 044903 (2008).

[13] B. Hoex, J.J.H. Gielis, M.C.M. van de Sanden, and W.M.M. Kessels, Journal of Applied

Physics **104**, 113703 (2008).

[14] X. Garros, C. Leroux, and J.-L. Autran, Electrochemical and Solid-State Letters **5**, F4 (2002).

[15] X. Garros, C. Leroux, D. Blin, J.F. Damlencourt, A.M. Papon, and G. Reimbold, in Proceedings of 32nd European Solid-State Device Research Conference (ESSDERC), Firenze (Italy), 2002, p. 411.

[16] R.J. Hillard, and B. Roberds, in Proceedings of Analytical Techniques for Semiconductor Materials and Process Characterization III (ALTECH), Leuven (Belgium), 1999, p. 385.

[17] D.K. Schroder, Semiconductor Material and Device Characterization, p. 261, John Wiley & Sons, New York (1990).

[18] http://www.semilab.hu

[19] A.W. Ott, J.W. Klaus, J.M. Johnson, and S.M. George, Thin Solid Films **292**, 135 (1997).

[20] D.K. Schroder, in Defects in Microelectronic Materials and Devices, D.M. Fleetwood, S.T. Pantelides, and R.D. Schrimpf, p. 131, CRC Press, Boca Raton (2009).

[21] M.D. Groner, J.W. Elam, F.H. Fabreguette, and S.M. George, Thin Solid Films **413**, 186 (2002).

[22] M.D. Groner, F.H. Fabreguette, J.W. Elam, and S.M. George, Chemistry of Materials **16**, 639 (2004).

[23] J.L. van Hemmen, S.B.S. Heil, J.H. Klootwijk, F. Roozeboom, C.J. Hodson, M.C.M. van de Sanden, and W.M.M. Kessels, Journal of The Electrochemical Society **154**, G165 (2007).

[24] P. Ericsson, S. Bengtsson, and J. Skarp, Microelectronic Engineering **36**, 91 (1997).

[25] R. Katamreddy, R. Inman, G. Jursich, A. Soulet, A. Nicholls, and C. Takoudis, Thin Solid Films **515**, 6931 (2007).

[26] S. Ferrari, and G. Scarel, Journal of Applied Physics **96**, 144 (2004).

[27] R.M.C. de Almeida, and I.J.R. Baumvol, Surface Science Reports **49**, 1 (2003).

[28] K. Kukli, T. Pilvi, M. Ritala, T. Sajavaara, J. Lu, and M. Leskelä, Thin Solid Films **491**, 328 (2005).

[29] M. Xu, C.-H. Xu, S.-J. Ding, H.-L. Lu, D. W. Zhang, and L.-K. Wang, Journal of Applied Physics **99**, 074109 (2006).

[30] C. Leroux, J. Mitard, G. Ghibaudo, X. Garros, G. Reimbold, B. Guillaumot, and F. Martin, in IEDM Technical Digest, 2004, p. 737.

[31] L. Pantisano, E. Cartier, A. Kerber, R. Degraeve, M. Lorenzini, M. Rosmeulen, G. Groeseneken, and H.E. Maes, in Symposium on VLSI Technology Digest of Technical Papers, 2003, p. 163.

[32] E.H. Snow, A.S. Grove, B.E. Deal, and C.T. Sah, Journal of Applied Physics **36**, 1664 (1965).

[33] G.A. Brown, in High Dielectric Constant Materials, VLSI MOSFET Applications, H.R. Huff, and D.C. Gilmer, p. 539, Springer, Berlin Heidelberg (2005).

[34] J.M. Rafí, L. Cardona-Safont, M. Zabala, C. Boulord, F. Campabadal, G. Pellegrini, M. Lozano, E. Simoen, and C. Claeys, Solid State Phenomena **131-133**, 431 (2008).

[35] R. Hezel, and K. Jaeger, Journal of The Electrochemical Society **136**, 518 (1989).

[36] http://www.hoenle.de

Figure and Table Captions

Table 1: Matrix of the different Al_2O_3 processing conditions studied in this work. The study includes for each ALD and annealing processes, different number of ALD cycles: 20, 40, 80, 100, 150 and 200 cycles.

Fig. 1: Ellipsometry-measured thickness versus number of ALD cycles for Al_2O_3 films as-deposited at (a) 100ºC, (b) 200ºC, (c) 300ºC and after being subjected to different thermal annealing conditions. The solid line corresponds to the linear fit for the as-deposited samples whereas the dashed line corresponds to the linear fit for the samples subjected to the highest temperature treatments (30 min at 800ºC in (a) and (c) and 1 h at 1000ºC in (b)).

Fig. 2: (a) C-V characteristics measured from inversion to accumulation and accumulation to inversion for an 80 ALD cycles Al_2O_3 layer deposited at 300ºC. The different curves correspond to as-deposited or after thermal annealing treatments (30 min at 450ºC or 30 min at 650ºC or 30 min at 800ºC). (b) Corresponding conductance versus voltage curves.

Fig. 3: Flat-band voltage versus thermal annealing conditions for Al_2O_3 layers deposited at (a) 100ºC, (b) 200ºC and (c) 300ºC.

Fig. 4: C-V curves hysteresis versus thermal annealing conditions for Al_2O_3 layers deposited at (a) 100ºC, (b) 200ºC and (c) 300ºC.

Fig. 5: Flat-band voltage versus ellipsometry-measured thickness for Al_2O_3 layers deposited at 100ºC and after being subjected to different thermal annealing conditions.

Fig. 6: (a) Microwave photoconductance decay recombination lifetime values measured on different silicon substrates before and after surface passivation with a 11 nm layer of ALD Al_2O_3 deposited at 200ºC on both wafer sides. The lifetime results after 30 min at 450ºC or 30 min at 800ºC thermal treatments in N_2 ambient are also given. (b) C-V curves measured on single-side passivated 2-side polished p-type samples under the same conditions of (a) ($N_{eff_as\text{-}dep}$ = -3.2·10^{12} cm^{-2}, $N_{eff_30m450ºC}$ = -5.6·10^{12} cm^{-2}, $N_{eff_30m800ºC}$ = -7.7·10^{12} cm^{-2}). (c) Corresponding conductance versus voltage curves ($N_{it_as\text{-}dep}$ = 1.5·10^{11} cm^{-2}, $N_{it_30m450ºC}$ = 2.2·10^{11} cm^{-2}, $N_{it_30m800ºC}$ = 9.7·10^{12} cm^{-2}).

Fig. 7: (a) C-V curves measured on a typical sample with an 11 nm-thick ALD Al_2O_3 layer before and after different ultraviolet light exposure times (accumulated UV irradiation times). (b) Extracted effective trapped charges and interface states densities (N_{eff} and N_{it}, respectively) corresponding to Fig. 7(a) C-V curves.

	Al_2O_3 ALD Temperature		
Annealing in N_2	100 ºC	200 ºC	300 ºC
30 min @ 450ºC	x	-	x
30 min @ 650ºC	x	-	x
30 min @ 800ºC	x	-	x
60 min @ 950 ºC	-	x	-
60 min @ 1000 ºC	-	x	-

Table 1

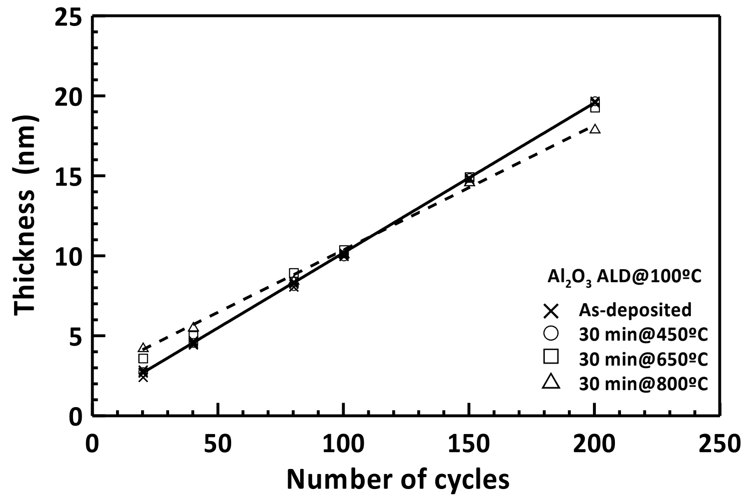

Fig. 1(a)

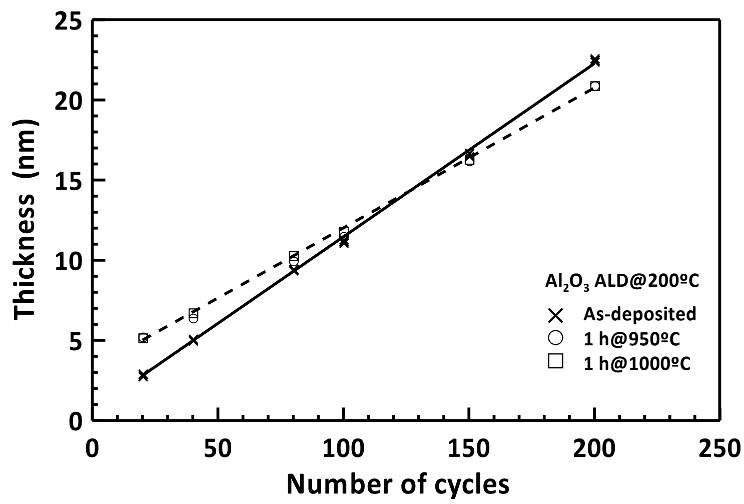

Fig. 1(b)

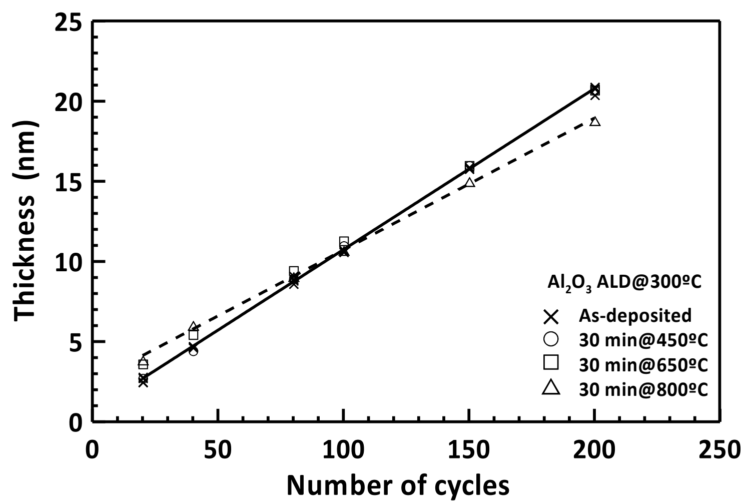

Fig. 1(c)

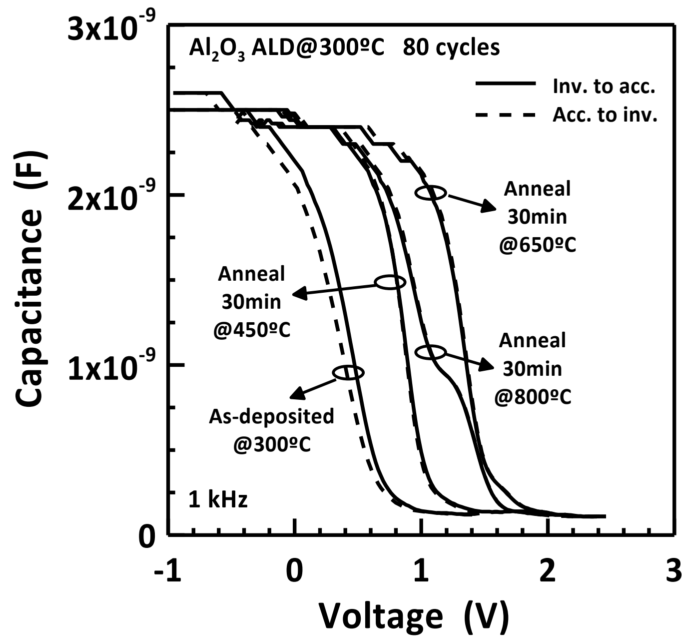

Fig. 2(a)

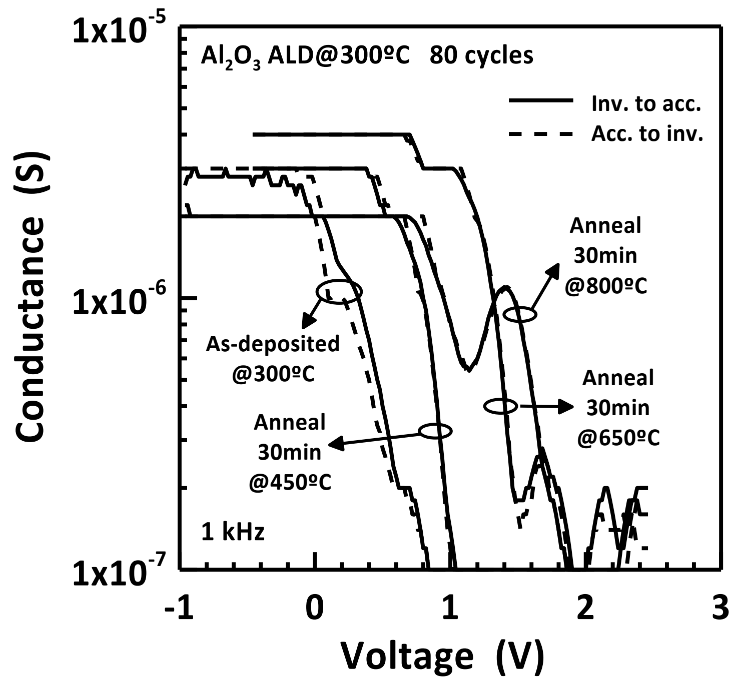

Fig. 2(b)

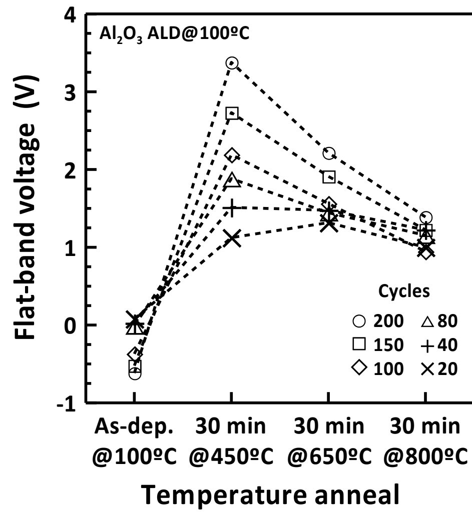

Fig. 3(a)

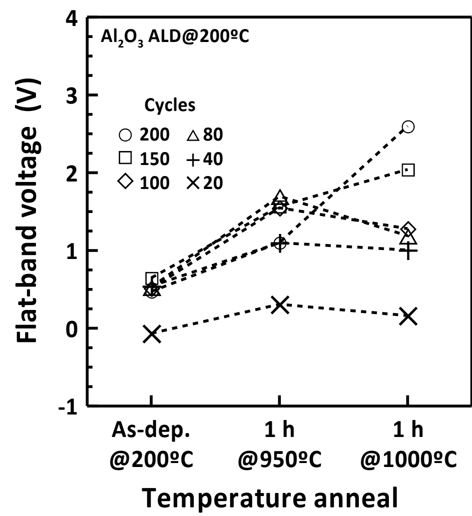

Fig. 3(b)

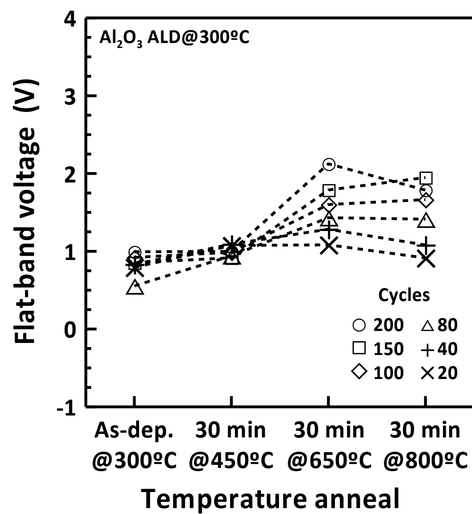

Fig. 3(c)

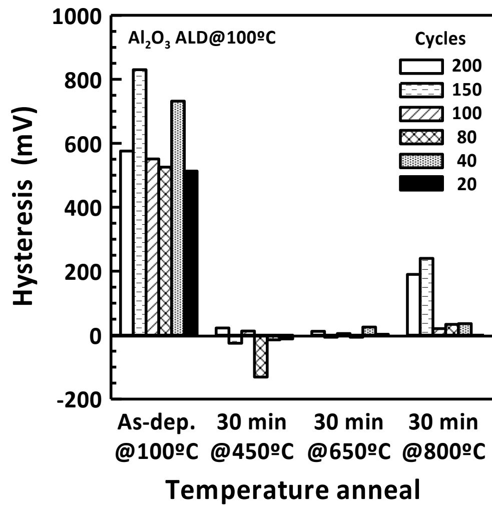

Fig. 4(a)

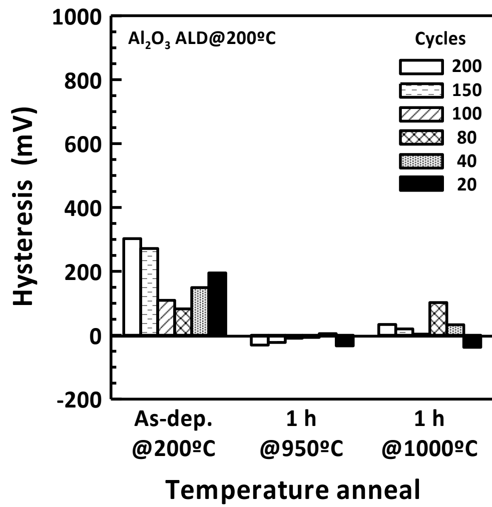

Fig. 4(b)

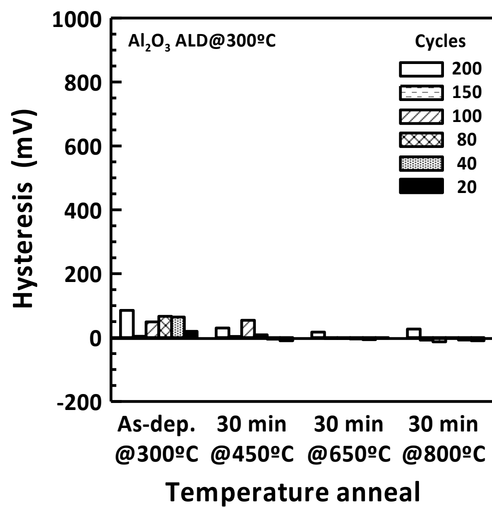

Fig. 4(c)

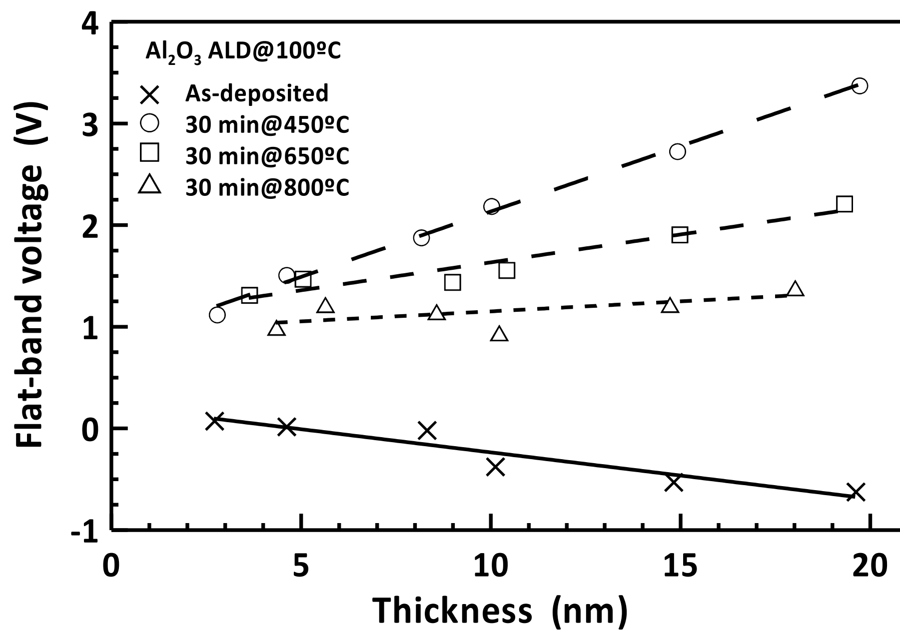

Fig. 5

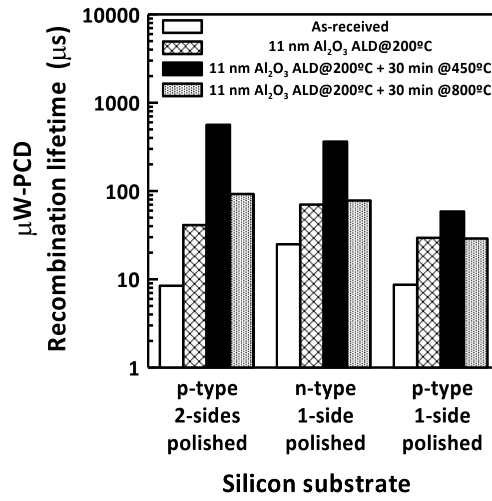

Fig. 6(a)

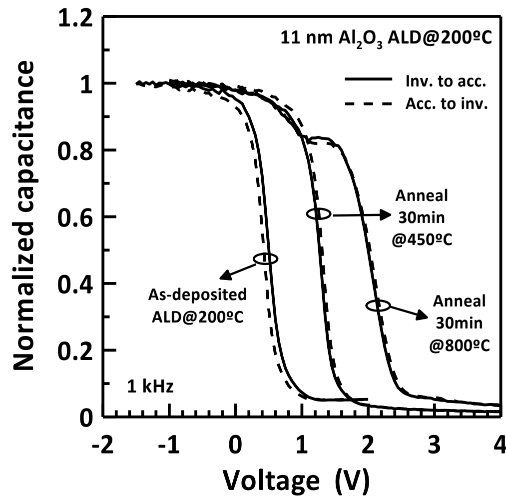

Fig. 6(b)

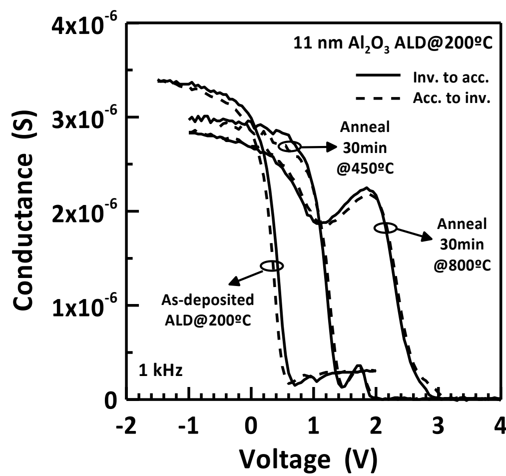

Fig. 6(c)

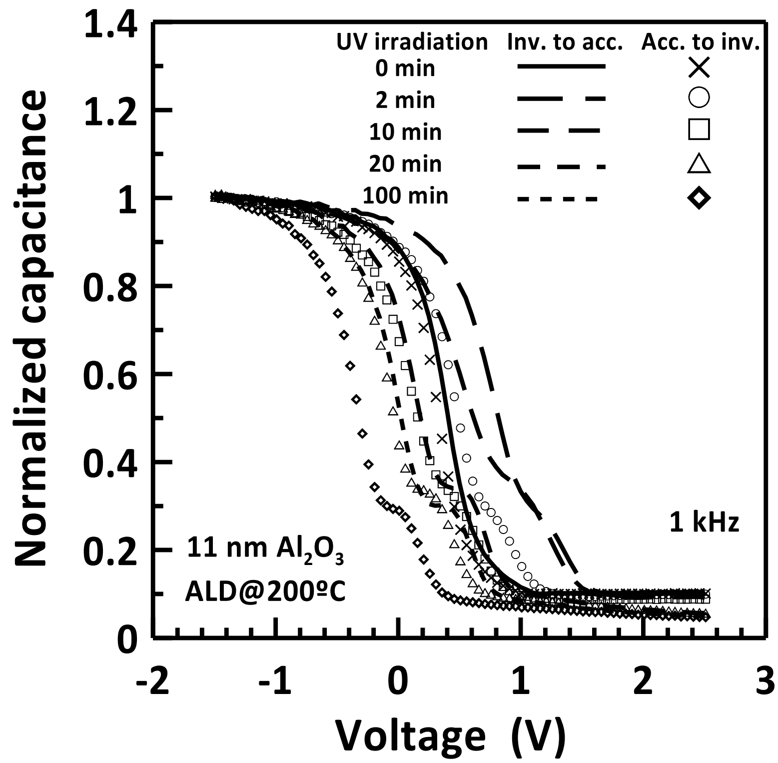

Fig. 7(a)

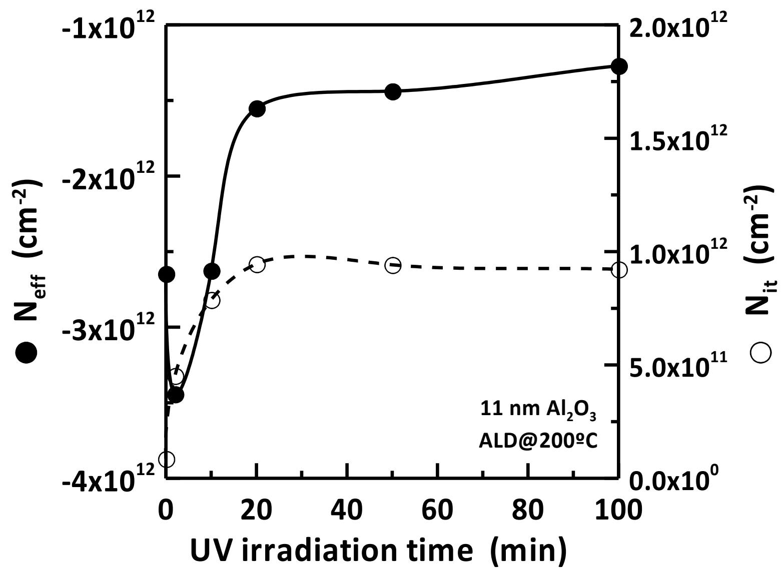

Fig. 7(b)