**Impact of electrical stress on the electrical characteristics of
2 MeV electron irradiated metal-oxide-silicon capacitors with
atomic layer deposited Al₂O₃, HfO₂ and nanolaminated dielectrics**

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ABSTRACT

In this work, the impact of electrical stress on the electrical characteristics of 2 MeV electron irradiated metal-oxide-silicon capacitors with atomic layer deposited (ALD) high permittivity (high-k) dielectric layers of Al_2O_3 , HfO_2 and a nanolaminate of them is evaluated. The aim is to investigate the susceptibility to electrical stress of the radiation effects created in irradiated MOS structures, paying especial attention to any possible interaction between the radiation-induced damage and the subsequent electrical stress degradation. For this study, MOS capacitors with a nominal dielectric physical thickness of 10 nm (equivalent oxide thickness (EOT) between 3 nm and 7 nm) on different p-type and n-type silicon substrates were investigated. An exponentially increasing stress current was forced to flow in accumulation through the different dielectric layers, registering the evolution of gate voltage versus stress time until dielectric breakdown occurred. Capacitance-voltage characteristics of the different irradiated and non-irradiated structures are analyzed as a function of electrical stress. Different charge trapping behaviours and significant polarity dependence in interface state generation are observed for the dielectric layers subjected to substrate and gate injections. No clear interaction between radiation and electrical stress damages is noticed under substrate injection (n-type samples). However, higher negative charge trapping near the metal/dielectric interface is registered for the irradiated Al_2O_3 and nanolaminate layers subjected to gate injection and, in the case of the most irradiated samples, the radiation-induced interface states damage is found to dominate against the damage generated in early stages of the electrical stress.

Keywords: electrical stress; electron irradiation; Al_2O_3 ; HfO_2 ; nanolaminate; high-k; ALD

I. INTRODUCTION

During the last decade a number of high permittivity (high-k) dielectrics have been investigated as candidates to replace the SiO₂ as gate dielectric in complementary metal-oxide-semiconductor (CMOS) technologies, being Al₂O₃ and HfO₂ among the most studied ones [1,2]. Apart from CMOS technologies, high-k dielectrics are also of strong interest for a wide range of micro/nanoelectronics applications, including, resistive random access memories (ReRAM) [3,4], emerging nanodevices [5,6], organic light emitting diodes [7], high-efficiency silicon solar cells [8], and for a variety of microelectromechanical systems [9]. In all these applications, high-k dielectric layers with typical thickness from a few nanometers to some tens of nanometers are of interest. The requirements of large area uniformity, conformality and accurate thickness control of the dielectric layers can be achieved by means of atomic layer deposition (ALD), a technique with a great potential for all the above applications. Moreover, a good advantage of ALD is that it allows the possibility to deposit thin alternate layers of different high-k materials (nanolaminates). This can be useful to tailor the dielectric properties of the stack, reduce leakage currents in the presence of possible crystallization processes or improve the interface in contact with the semiconductor [10,11].

In recent years, a lot of work has been devoted to physical and electrical characterization, as well as to reliability issues, of high-k dielectrics [12,13]. However, much less is known about their behaviour in radiation environments. The study of ionizing radiation effects on high-k dielectrics is of special interest for space applications, but also for high energy physics

experiments and to gain insight into possible effects of advanced micro/nanofabrication processes like e-beam or X-rays lithography.

Since the early days of microelectronics, radiation-induced effects on conventional SiO_2 dielectrics for CMOS technologies have been investigated [14-16]. Fortunately, the continuous miniaturization process has led to radiation-harder SiO_2 layers, with reduced charge trapping and thickness below the trapped-hole tunnelling limit (around 3 nm) [15]. However, the introduction of new high-k dielectric materials brings some uncertainty in terms of their radiation hardness [16]. Different works have been published on radiation effects on a limited number of high-k dielectrics, being these mostly limited to irradiations with heavy ions or X-rays [17-20]. As a difference to irradiation with other particles like neutrons, protons or heavy ions, in the case of electron irradiation, the ionization damage is dominant against the displacement damage and this make them appropriate to evaluate ionizing radiation effects in dielectric materials. On the other hand, electrons are present in hostile radiation environments like advanced micro/nanofabrication processes, high energy physics experiments or the earth's natural radiation environment. For the case of the electrons trapped by the earth's magnetic field, typical energies of a few MeV are encountered, affecting the operation of electronic devices in artificial satellites [21].

In a previous work [22], we studied the effects of 2 MeV electron irradiation on the capacitance-voltage (C-V) and current-voltage (I-V) electrical characteristics of MOS capacitors with ALD-deposited layers of Al_2O_3 , HfO_2 and nanolaminate dielectrics. The results showed similar radiation-induced charge trapping and interface states generation for

the three high-k dielectrics, with an increase of the leakage current with electron irradiation fluence and no apparent impact of electron irradiation on dielectric breakdown voltage.

Few works in the literature have addressed the electrical stress effects on irradiated CMOS gate dielectrics, most of them dealing with conventional SiO₂-based dielectrics, where no much effects of the radiation-induced damage on the subsequent generation rate of traps during high-field stress was encountered [23-25]. More recently, some first attempts to evaluate possible combined effects between irradiation and electrical stress have been also carried out for HfO₂-based dielectrics [26,27].

The aim of the present work is to evaluate any possible interaction between the radiation-induced damage and the subsequent electrical stress degradation, focusing on the study of effective trapped charges, generation of interface states and presence of hysteresis.

II. EXPERIMENTAL

A. Sample description

Three high-k dielectric layers, Al₂O₃, HfO₂ and a 5-layer stack nanolaminate of them (Al₂O₃/HfO₂/Al₂O₃/HfO₂/Al₂O₃), with physical thickness 11.6 nm, 10.5 nm and 10 nm, respectively, are studied. The layers were deposited by ALD in a Cambridge NanoTech Savannah 200 system. Al-gate MOS capacitors were fabricated on n-type and p-type silicon wafers. Three types of silicon substrates were used: n-type (phosphorus-doped with a

resistivity 1-12 $\Omega\cdot\text{cm}$), and two p-type substrates with different doping concentrations of boron, giving resistivity ranges of 4-40 $\Omega\cdot\text{cm}$ and 0.1-1.4 $\Omega\cdot\text{cm}$, which are referred here as p-type 10 $\Omega\cdot\text{cm}$ and p-type 1 $\Omega\cdot\text{cm}$, respectively. Although only results for a single p-type substrate may be given in the following discussions, the results were qualitatively and quantitatively similar for both p-type substrates. The used MOS capacitors are square-shaped with $6.4\times 10^{-5} \text{ cm}^2$ area (A). The obtained equivalent oxide thickness (EOT) values on the different silicon substrates ranged between 5.9 nm and 6.9 nm, 3.2 nm and 3.5 nm, and 4.3 nm and 5.1 nm for the Al_2O_3 , HfO_2 and nanolaminate layers, respectively. Following this, the corresponding effective permittivity values ranged between 6.5 and 7.7, 11.8 and 13.1, and 8.2 and 9.7, respectively. A detailed description of the fabrication process can be found in [28].

B. Irradiation, electrical stress and electrical characterization

MOS capacitors were subjected to unbiased 2 MeV electron irradiations (the gates of capacitors were left floating) at room temperature for three different fluences ($\phi = 1\cdot 10^{14} \text{ e/cm}^2$, $1\cdot 10^{15} \text{ e/cm}^2$ and $1\cdot 10^{16} \text{ e/cm}^2$, with total ionizing doses about 2.5 Mrad(Si), 25 Mrad(Si) and 250 Mrad(Si), respectively), using the electron accelerator at Takasaki-JAEA in Japan.

In order to subject non-irradiated and 2 MeV electron-irradiated high-k dielectric MOS capacitors to electrical stress, an exponentially increasing stress current was forced to flow through the different dielectric layers, recording the evolution of gate voltage versus stress

time until dielectric breakdown occurred, which was detected as a sudden drop of the measured gate voltage. Such a time dependent dielectric breakdown experiment will provide a reliability assessment of the different irradiated and non-irradiated layers for a potentially wide range of injected charge densities [29]. Figure 1 shows a sketch of the experimental method used for the electrical stress. The specific values corresponding to the current densities and injection times used for each step are given in Table 1. The stresses were always performed in accumulation regime, i.e., corresponding to negative gate voltages with respect to the p-type substrates and positive gate voltages in the case of the n-type silicon ones. The injected charge density (Q_{inj}) is the sum of the injected charge densities corresponding to the different injection steps (Q_i).

C-V characteristics and electrical stresses were measured using an HP-4192 A LF impedance analyzer and an HP 4155B semiconductor parameter analyzer, respectively. C-V measurements were performed before and after each electrical stress step at a signal frequency (f) of 30 kHz for both, inversion to accumulation and accumulation to inversion voltage sweeps. The hysteresis was defined as the difference between the extracted flat-band voltages (V_{fb}) corresponding to the two voltage sweeps ($\text{hysteresis} = V_{fb_inv_to_acc} - V_{fb_acc_to_inv}$) [30]. An estimation of the effective trapped charge density (N_{eff_CV}), defined as a charge located at the insulator/silicon interface, was obtained from the comparison of the extracted V_{fb} values with the ones expected for an ideal MOS structure with 4.25 eV metal work function, corresponding to the aluminium gate electrode.

The conductance versus voltage (G-V) characteristics were also recorded. An estimation of the interface states density (D_{it}) was obtained from the peak of the parallel conductance (G_p) derived from the G-V measurements [31-33]:

$$D_{it} \approx \frac{2.5}{q \cdot A} \cdot \frac{G_p}{2\pi f} \quad (1)$$

where q is the electron charge.

III. RESULTS AND DISCUSSION

A. Voltage versus injection time characteristics

Figure 2 shows an example of the measured gate voltage as a function of cumulative stress time for non-irradiated and 2 MeV electron-irradiated Al_2O_3 layers under substrate injection (n-type silicon) subjected to the exponential stress current experiment described in Figure 1 and Table 1. As it can be noticed, a voltage staircase is obtained when injecting the increasing current densities. It can be noted that lower voltage levels are required for injecting a fixed current density in the irradiated capacitors at a given step. This result is explained by the the radiation-induced damage, which leads to an increase of the electrical conduction through the dielectric layers [22].

Interestingly, the voltage level in each current injection step is not constant and some variation is detected with injection time. For the particular case of the Al_2O_3 layers on n-type

Si of Figure 2, a progressive increase of the applied voltage is observed in each step. This is indicative of negative charge trapping in the high-k dielectric layer, which increases the gate dielectric potential barrier, decreasing the electron transmission probability [34,35]. Finally, a sudden drop of the measured gate voltage, indicative of dielectric breakdown, is observed at the beginning of the sixth injection step in Figure 2 samples. Although no statistical evaluation of dielectric breakdown was carried out, no clear impact of electron irradiation fluence on the registered dielectric breakdown events was observed for the three different studied dielectrics, as it can be already seen in Figure 2 for Al₂O₃ on n-type Si. These results are in agreement with our previous work [22], where no significant differences in breakdown voltages between non-irradiated and 2 MeV electron irradiated samples were noticed by means of voltage ramp tests.

From gate voltage versus stress time measurements analogous to Figure 2, the cumulative variation of the gate voltage (ΔV) along stress time can be extracted. Assuming that under gate and substrate injections the gate voltage is sensitive to the generated charges near the gate/dielectric and dielectric/semiconductor interfaces, respectively [36,37], an estimation of the involved effective trapped charges densities ($N_{\text{eff_vt}}$) can be obtained from $(\Delta V \cdot C_{\text{ox}})/q$, where C_{ox} is the accumulation capacitance. This has been plotted in Figs. 3 and 4 for the different dielectrics on n-type and p-type silicon, respectively. Interestingly, the results have shown different trends for the dielectrics on n-type or p-type Si. In the case of the studied dielectrics under substrate injection (n-type silicon), monotonous negative charge trapping near the high-k dielectric/semiconductor interface has been found (Figure 3). The highest electron trapping under substrate injection has been registered for the case of Al₂O₃, while densities about three times smaller have been registered for HfO₂ and

intermediate values have been obtained for the combined nanolaminate material. With regard to the impact of irradiation on the cumulative charge trapping, no clear differences have been observed for the different dielectric layers under substrate injection (n-type silicon samples).

Some authors have extracted trap parameters, such as the capture cross section from the variation of the gate voltage during constant current stress experiments [38,39]. Assuming no significant generation of new traps and a single type of trap, the gate voltage versus injected charge during a constant electrical stress phase should be of the form [40]:

$$V(N_{inj}) = V_0 + \left(\frac{q\bar{x}N_t}{dC} \right) (1 - e^{-\sigma N_{inj}}) \quad (2)$$

where N_{inj} is the injected charge density ($N_{inj}=Q_{inj}/q$), V_0 is the voltage required for the injected current without trapping, q is the electron charge, N_t is the areal density of traps, $\bar{x}$ is the trapped charge centroid measured from the collecting electrode, d and C are the insulator thickness and capacitance, respectively and σ is the capture cross section.

From Eq. (2), a plot of $\ln(\partial V / \partial N_{inj})$ versus N_{inj} would yield a straight line with a slope which is the capture cross section. Following this approach, the inset in Fig. 3(a) shows a plot of the derivative of the measured gate voltage with respect to N_{inj} corresponding to a particular stress step. As it could be expected from the large electron fluences and charge injection levels involved in this study, no single straight line is observed in Fig. 3(a) inset; however, the decreasing slope may be explained by different traps with lower cross sections

and the asymptotic tendency towards increasing values at high injection would indicate the influence of trap generation for the more irradiated layers [38].

Additionally, as reported in [41], the kinetics of the charge build-up has been also fitted by the following empirical power law:

$$\frac{\partial V(N_{inj})}{\partial N_{inj}} = k \cdot N_{inj}^{-\nu} \quad (3)$$

where k is a constant dependent on the oxide technology and ν a positive exponent.

The extracted values for ν (in the range of 1.1 to 1.3) are similar to previous results published in the literature for conventional SiO₂-based gate dielectrics [23,41,42].

Concerning the high- k dielectrics under gate injection (p-type silicon) (Figure 4), different trends are observed for the cumulative charge trapping near the metal/dielectric interface. Negative charge trapping near the injecting gate electrode [34] is observed for HfO₂, as well as for early stages of the electrical stress in Al₂O₃ and nanolaminate layers. This phenomenon is also attributed to electron trapping in pre-existing defects, which tends to hinder the injection from the gate. Similarly to the case of the dielectric layers under substrate injection (n-type Si), the highest electron trapping is registered for the case of Al₂O₃, whereas a few times smaller values are registered for HfO₂ and nanolaminate. Moreover, higher negative charge trapping near the metal/dielectric interface is registered for the most irradiated Al₂O₃ and nanolaminate layers (Figs. 4(a) and 4(c)). However, a

turnaround behaviour is observed after long electrical stress for the Al_2O_3 and nanolaminate layers non-irradiated or exposed to the lowest irradiation fluences. For these cases, a progressive increase of the electron injection is observed, which can be originated by either, a decrease of the gate dielectric potential barrier due to positive charge near the metal/dielectric interface [43,44] or stress induced leakage current (SILC) due to additional defect generation in the bulk of the dielectric after such long electrical stresses [45]. Similar results showing an increase in the stress current after long constant voltage stresses have been reported for the case of SiO_2 - Al_2O_3 stacks under gate injection [46]. As will be shown later, the significant generation of dielectric/semiconductor interface states found for gate injection conditions is also a clear indication for trap creation under this polarity. Finally, a plot of the efficiency with which an injected electron produces charge that results in a change of the gate voltage during the injection experiment is shown in Fig. 4(a) inset. Although this figure corresponds to the particular case of Al_2O_3 MOS capacitors on p-type silicon, the shape and magnitude of the trapping efficiencies were qualitatively similar for the different dielectrics and substrates studied, being this also in agreement with trapping probabilities observed on similar high-k dielectric layers subjected to electrical stress [47].

B. Capacitance-voltage and conductance-voltage characteristics

Effective trapped charge density ($N_{\text{eff_CV}}$)

In order to better investigate the electrically-induced degradation, C-V characteristics were measured before and after each electrical stress step. As a difference to I-V or the measured

voltage versus injection time curves, which sense the trapped charge from the injection electrode side, C-V curves provide an assessment of the charge close to the dielectric/semiconductor interface [34,37]. Figure 5(a) shows an example of typical C-V characteristics measured for an Al₂O₃ MOS capacitor on n-type silicon substrate. The different curves correspond to different injected charge densities, by increasing the electrical stress (process described in Figure 1 and Table 1). Although Figure 5(a) C-V plots correspond to a MOS capacitor irradiated at 10¹⁴ e/cm², the results are qualitatively similar for irradiated or non-irradiated devices subjected to substrate injection (n-type samples), where a progressive positive shift of the characteristics is observed with increasing electrical stress, indicating a negative charge build-up process near the dielectric/n-type Si interface. This is in agreement with Fig. 3(a) results.

Figures 6(a), 6(b) and 6(c) show the effective trapped charge density ($N_{\text{eff_CV}}$) versus injected charge density (Q_{inj}) corresponding to non-irradiated and irradiated Al₂O₃, HfO₂ and nanolaminate layers on n-type and p-type silicon. As expected, radiation-induced positive trapped charges are normally noticed for the irradiated samples before electrical stress ($Q_{\text{inj}}=0$) [22]. When subjecting the samples to the electrical stress, regardless of the irradiation fluence, a quite similar electrical-induced degradation trend is generally observed for each different dielectric layer and silicon substrate. Similar charge trapping behaviours have been reported in the literature for electrical stress of Al₂O₃ [37] and HfO₂-based [48,49] gate dielectrics. No apparent interaction between the radiation-induced and electrical stress damages is noticed. At high stressing conditions, for the particular case of the Al₂O₃ layers on n-type substrates in Fig 6(a), significantly higher negative charge trapping rate is observed for the more irradiated devices, leading to some convergence of the N_{eff}

versus Q_{inj} curves of the different fluences towards trapped charge densities around $-1 \cdot 10^{13} \text{ cm}^{-2}$, where dielectric breakdown of the layers finally occurs. The ultimate reason of this behaviour is not known and, as shown in Figs. 6(b) and 6(c), this is not observed for the HfO_2 and nanolaminated dielectrics.

Consistently with the measured gate voltage under substrate injection curves, the higher electron trapping is registered for the case of Al_2O_3 , followed by nanolaminate and HfO_2 . Furthermore, a reasonable agreement has been found between the evolution of the effective trapped charge densities measured by C-V near the dielectric/n-type silicon interface (N_{eff_cv}) (n-type in Figure 6) and the ones associated to the variation of the gate voltage during the electrical stress experiments (N_{eff_vt}) (Figure 3).

On the other hand, for the case of the samples subjected to gate injection (p-type substrates), the effective trapped charges results are different for Al_2O_3 compared to HfO_2 and nanolaminate. In this way, negative charge trapping is registered during the major portion of the gate injection stress for the Al_2O_3 layers (Fig. 6(a)), being this in agreement with the electron trapping near the metal/dielectric electrode derived from Fig. 4(a) results. Moreover, and also in agreement with Figure 4(a) results, a certain positive charge trapping tail is also detected for the Al_2O_3 MOS capacitors on p-type Si after the highest injection conditions. As in Figure 4(a) results, the positive charge build-up tail in p-type Al_2O_3 capacitors of Fig. 6(a) is more detected in the samples non-irradiated or exposed to the lowest irradiation fluences.

Opposite to Al_2O_3 on p-type Si results, positive charge trapping near the dielectric/semiconductor interface is detected under the gate injection experiments for HfO_2 , leading to positive $N_{\text{eff_CV}}$ values for all electrically stressed conditions (Fig. 6(b)). A somewhat smaller positive charge trapping is noticed for the combined nanolaminate stack, with negative $N_{\text{eff_CV}}$ values for most of the studied electrical stress conditions (Fig. 6(c)). From Figs. 4(b), 4(c), 6(b) and 6(c) it is derived that effective charges of different signs (negative near the metal/dielectric interface and positive near the dielectric/semiconductor interface) are generated through the high-k dielectric during gate injection in the HfO_2 and nanolaminate films. These results are in agreement with previous studies reported in the literature for either $\text{SiO}_2\text{-Al}_2\text{O}_3$ stacks [46] or HfO_2 [50], where positive charge build-up near the Si substrate has been also observed after long gate injection. This has been attributed to the damage generated by hot carriers releasing their energy at the dielectric/silicon collecting interface. For the case of our Al_2O_3 results, the high negative charge trapping registered by the layers under gate injection (Fig. 4(a)) could dominate during the major part of the gate injection stress and only a certain positive charge trapping tail is detected after the highest injection conditions (Fig. 6(a)).

Interface states density (D_{it})

Figure 5(b) shows the conductance versus voltage (G-V) characteristics measured from inversion to accumulation corresponding to Fig. 5(a) results. As shown, a peak in the conductance curves is generally observed. These peaks are especially noticed in the samples irradiated at the highest irradiation fluences and are due to the loss mechanism associated

to interface trap capture and emission of carriers [22]. As it can be observed in the example of Fig. 5(b), the conductance peaks have been found to increase with the injected charge density and an estimation of the interface states density (D_{it}) has been obtained from the peak of the corresponding parallel conductance (Eq. (1)).

The extracted D_{it} results are plotted in Figures 7(a) and 7(b). From the figures, significant polarity dependence in interface state generation is observed between gate injection (p-type Si, Fig. 7(a)) and substrate injection (n-type Si, Fig. 7(b)). At high stressing levels, the higher generation rate of interface-states under gate injection is explained by the primary damage generated by the injected electrons when releasing their energy at the dielectric/silicon collecting interface. This phenomenon has been reported for conventional SiO_2 gate dielectrics [51] and similar results have been observed for $\text{SiO}_2/\text{Al}_2\text{O}_3$ high-k dielectric stacks [37] and HfO_2 [50,52].

From Fig. 7(a), a common trend can be noticed for interface state generation on the less irradiated Al_2O_3 and nanolaminate samples, from which a potential law can be inferred $D_{it} \propto Q_{inj}^n$, with n values around 0.36 for Al_2O_3 and 0.24 for nanolaminate. Similar n values have been reported in the literature for electrical-stress of non-irradiated SiO_2 [53,54] or HfO_2 -based [49,52] gate dielectrics, as well as gamma-irradiated conventional and nitrured SiO_2 [25]. It has to be commented that for the case of the most irradiated samples a lower dependence of D_{it} on Q_{inj} is observed for early stages of the electrical stress, which is attributed to a dominant role of the radiation-induced interface states. For the case of the HfO_2 devices, the conductance peaks on the small area capacitors studied could be only

detected for the more irradiated samples and, within the studied Q_{inj} range, no additional contribution of the electrical stress to the radiation-induced D_{it} was noticed (Fig. 7(a)).

With regard to the substrate injection condition (dielectric layers on n-type silicon, Fig. 7(b)), as commented, a significantly lower generation rate of interface-states with electrical stress is found, with typical “n” values for the D_{it} versus Q_{inj} potential dependence in the range of 5 times lower than their p-type substrate counterparts. This is explained by the higher difficulties of secondary processes in the generation of damage at the dielectric/semiconductor interface when this is not the collecting electrode. In particular, carrier heating and generation of interface states could be also prevented by a high density of defects present in the case of the irradiated devices [46].

Hysteresis

As it could be already observed in Figure 5(a), the magnitude of the C-V curves hysteresis has been found to evolve with the applied electrical stress. Interestingly, no clear differences have been noticed between non-irradiated and irradiated layers subjected to electrical stress, and a similar increase of the hysteresis can be observed in Figure 8(a) for the non-irradiated and irradiated Al_2O_3 layers on p-type Si. This hysteresis increase is in agreement with previously published results corresponding to H_2O and O_3 -based Al_2O_3 ALD layers with and without post-deposition annealings and subjected to constant voltage stresses [44]. However, the opposite trend is observed for the HfO_2 dielectrics on p-type

silicon substrate and an intermediate behaviour is obtained for the nanolaminate stack, combining Al_2O_3 and HfO_2 layers.

The hysteresis of the C-V characteristics is believed to be associated to interface (fast) and near interface (slow) border traps, which may get charged and exchange electrons with the silicon substrate depending on the sweep direction [55,56]. As observed in Figs. 8(a) and 8(b), positive (counter-clockwise) and negative (clockwise) hysteresis values are registered for the case of the high-k dielectrics on p-type and n-type silicon, respectively. This is in agreement with the charge and discharge of defects situated near the semiconductor/dielectric interface [31]. In case of defects located near the metal/dielectric interface, reduced effects on C-V curves and with opposite hysteresis directions would be expected [57].

Similarly to the 2 MeV electron irradiation effects [22], in the present work it is believed that damage generated by the injected electrons when releasing their energy at the dielectric/silicon collecting interface may be responsible for the increasing hysteresis observed for the Al_2O_3 dielectric layers on p-type Si (Fig. 8(a)). On the other hand, the opposite trend shown by the HfO_2 layers on p-type Si can be originated by their high pre-existing non-irradiated hysteresis values. In the present study, the applied electrical stress could result in hydrogen release from the HfO_2 layers, introduced by the precursors chemistry, leading to a certain passivation of the instabilities responsible for the C-V hysteresis. From Figure 8(a), the decrease of the hysteresis in the HfO_2 layers is more significant at the beginning of the electrical stress and diminishes with the progress of the stress, where more electrically-induced defects are expected to contribute to the overall C-V

curves hysteresis. A similar mechanism was proposed for the case of ALD Al_2O_3 layers of comparable thickness subjected to 10-keV X-rays irradiation [18,58], where a decrease of interface states with radiation exposure was attributed to a possible radiation-induced hydrogen passivation of traps in those layers with quite high pre-irradiation interface states densities (in the range of $1 \times 10^{12} \text{ cm}^{-2}$). Finally, the behaviour of the nanolaminate stacks can be explained by the combined effects of the Al_2O_3 and HfO_2 layers on p-type Si.

With regard to the high-k dielectrics on n-type silicon (Fig. 8(b)), a reduction of the C-V hysteresis has been observed for the three insulators subjected to the substrate injection electrical stress. This can be explained by the lower generation of damage at the dielectric/semiconductor interface under substrate injection (Fig. 7(b)) and possible hydrogen release from the layers near the collecting gate electrode under this polarity, which may diffuse through the high-k layer leading to a certain beneficial passivation of the instabilities responsible for the C-V hysteresis at the dielectric/semiconductor interface.

IV. CONCLUSIONS

The impact of electrical stress on the electrical characteristics of 2 MeV electron irradiated MOS capacitors with Al_2O_3 , HfO_2 and nanolaminate ALD high-k dielectric layers has been evaluated. An exponentially increasing stress current has been forced to flow in accumulation through the different test structures, until dielectric breakdown has occurred. The evolution of gate voltage versus stress time and C-V characteristics have shown that electron trapping near the dielectric/semiconductor interface occurs for the dielectrics

subjected to substrate injection (n-type silicon samples). On the other hand, combined effects of negative and positive charge trapping are encountered under gate injection conditions (p-type silicon samples), as well as high generation rates of interface-states. A clear reduction of the C-V curves hysteresis with injected charge is observed for the studied dielectric layers under substrate injection (n-type samples), while different trends are observed for the different dielectrics under gate injection (p-type samples). No clear interaction between the radiation-induced and electrical stress damages is noticed under substrate injection (n-type samples). However, higher negative charge trapping near the metal/dielectric interface has been observed for the irradiated Al_2O_3 and nanolaminate layers subjected to gate injection and, in the case of the most irradiated samples, the radiation-induced interface states damage is found to dominate against the generated in early stages of the electrical stress.

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TABLE CAPTIONS

Table 1: Current densities (J_{inj}) and injection times (t_{inj}) used for each step of the exponential stress current experiment described in Fig. 1.

FIGURE CAPTIONS

Figure 1: Sketch of the exponential stress current experiment used for the electrical stress of the non-irradiated and 2 MeV electron-irradiated high-k dielectric MOS capacitors under study.

Figure 2: Measured gate voltage as a function of cumulative stress time for non-irradiated and 2 MeV electron-irradiated Al_2O_3 layers on n-type Si subjected to the exponential stress current experiment described in Fig. 1 and Table 1.

Figure 3: Effective trapped charges densities associated to the cumulative variation of the gate voltage (N_{eff_vt}) for non-irradiated and 2 MeV electron-irradiated (a) Al_2O_3 , (b) HfO_2 , and (c) Nanolaminate dielectric layers on n-type Si subjected to the exponential stress current experiment described in Fig. 1 and Table 1. The inset in Fig. 3(a) shows the derivative of the measured gate voltage with respect to the injected charge density ($N_{inj}=Q_{inj}/q$) versus N_{inj} (Eq. 2) corresponding to a particular stress step.

Figure 4: Effective trapped charges densities associated to the cumulative variation of the gate voltage ($N_{\text{eff_vt}}$) for non-irradiated and 2 MeV electron-irradiated (a) Al_2O_3 , (b) HfO_2 , and (c) Nanolaminate dielectric layers on p-type Si subjected to the exponential stress current experiment described in Fig. 1 and Table 1. The inset in Fig. 4(a) shows the ratio between $N_{\text{eff_vt}}$ and the injected charge density ($N_{\text{inj}}=Q_{\text{inj}}/q$) versus N_{inj} .

Figure 5: (a) C-V characteristics measured from inversion to accumulation (lines) and accumulation to inversion (symbols) for an Al_2O_3 MOS capacitor on n-type Si irradiated with 2 MeV electrons at a fluence of 10^{14} e/cm². The different curves correspond to increasing injected charge densities. (b) Corresponding conductance characteristics measured from inversion to accumulation.

Figure 6: Effective trapped charges densities extracted from C-V curves ($N_{\text{eff_cv}}$) versus injected charge density for non-irradiated and 2 MeV electron-irradiated (a) Al_2O_3 , (b) HfO_2 and (c) nanolaminate MOS capacitors on n-type and p-type Si.

Figure 7: Interface states densities (D_{it}) versus injected charge density for non-irradiated and 2 MeV electron-irradiated Al_2O_3 , HfO_2 and nanolaminate MOS capacitors on (a) p-type and (b) n-type Si.

Figure 8: C-V hysteresis versus injected charge density for non-irradiated and 2 MeV electron-irradiated Al_2O_3 , HfO_2 and nanolaminate MOS capacitors on (a) p-type and (b) n-type Si.

$J_{inj} [A/cm^2]$	$t_{inj} [s]$	$J_{inj} [A/cm^2]$	
		Al_2O_3 or Nanolaminate	HfO_2
J_1	500	$2 \cdot 10^{-6}$	$2 \cdot 10^{-6}$
J_2	500	$2 \cdot 10^{-5}$	$6.3 \cdot 10^{-6}$
J_3	500	$2 \cdot 10^{-4}$	$2 \cdot 10^{-5}$
J_4	500	$2 \cdot 10^{-3}$	$6.3 \cdot 10^{-5}$
J_5	500	$2 \cdot 10^{-2}$	$2 \cdot 10^{-4}$
J_6	500	$2 \cdot 10^{-1}$	$6.3 \cdot 10^{-4}$
J_7	500	$2 \cdot 10^0$	$2 \cdot 10^{-3}$
J_8	500	$2 \cdot 10^1$	$6.3 \cdot 10^{-3}$

Table 1

Figure 1

Figure 2

Figure 3(a)

Figure 3(b)

Figure 3(c)

Figure 4(a)

Figure 4(b)

Figure 4(c)

Figure 5(a)

Figure 5(b)

Figure 6(a)

Figure 6(b)

Figure 6(c)

Figure 7(a)

Figure 7(b)

Figure 8(a)

Figure 8(b)