GOBIERNO DE ESPAÑA
MINISTERIO DE ECONOMÍA Y COMPETITIVIDAD
CSIC
Consejo Superior de Investigaciones Científicas

Instituto de Microelectrónica de Sevilla
Centro Nacional de Microelectrónica

IMSE-CNM
Biennial Report 2011/2012

CENTRO NACIONAL DE MICROELECTRONICA
IMSE

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Biennial Report 2011/2012

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Instituto de Microelectrónica de Sevilla
Centro Nacional de Microelectrónica

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FOREWORD

This report summarizes the research activities and the main achieved objectives by the Instituto de Microelectrónica de Sevilla during the 2011-2012 biennium. This period was marked by an economic situation that has led to the progressive reduction of the research funding sources, of the opportunities to recruit young researchers and highly qualified personnel. These drawbacks, however, have not prevented this Institute from reaching, during both years, 100% of the targets set in the Strategic Plan of the CSIC, particularized with the indicators collected in the PCO (Productivity for Achievement of Objectives).

In the two years herein considered, 24 research projects, supported by various regional, national and international programs, as well as 5 contracts with private companies, have started. The research results have led to 36 publications in high-impact international journals and 118 contributions to renowned international conferences. The process of obtaining 11 new patents, which will facilitate the transfer of these results to the microelectronics industry, has also been initiated. Last, it is worth mentioning the active participation of researchers from this center in the Master program in Microelectronics at the Universidad de Sevilla, as well as the implementation of numerous outreach activities.

With respect to organizational aspects, this biennium has been characterized by the consolidation of the laboratories and related infrastructures, created on the occasion of the change of the Institute's headquarters, at the Parque Científico y Tecnológico Cartuja, the development of a process of internal restructuring to adapt its administrative organization to other centers of CSIC, and the ongoing process of transforming the Institute into a joint center between the CSIC and the Universidad de Sevilla.

Regarding the personnel, in these two years 4 members of the Technical Units have consolidated their position, 6 new doctoral students have joined the Institute and 17 doctoral theses have been defended. Finally, 7 new doctors have left the center to continue their careers in major Spanish and European organizations and industries.

Last, but not least important, in October 2011 there was a change in the direction position of the Institute, prompted by the retirement of José Luis Huertas, its creator and promoter, teacher and role model for many members of the Institute. I would like to take this opportunity to thank, once again, his continual efforts to launch a research center that has become a national and international reference.

Santiago Sánchez Solano
Acting Director

ABOUT IMSE

The Instituto de Microelectrónica de Sevilla (IMSE-CNM – Seville Institute of Microelectronics) is an R&D&I center belonging to the Agencia Estatal Consejo Superior de Investigaciones Científicas (CSIC - Spanish National Research Council). Together with its counterpart institutes in Barcelona and Madrid, it forms part of the Centro Nacional de Microelectrónica (CNM - National Microelectronics Center).

The Institute is dedicated to the field of Physical Science and Technologies, one of the eight areas into which research activity is divided by the CSIC. Its main area of specialization is the design and test of CMOS analog and mixed-signal integrated circuits and their use in different application contexts such as radiofrequency, microsystems or data conversion.

The IMSE-CNM began its operations in October 1989 under the auspices of an agreement signed by the Junta de Andalucía (the Andalusian Regional Government), the CSIC and the Universidad de Sevilla. Its founding research group was initially based on the premises of the Centro de Informática Científica de Andalucía (CICA – Scientific Computing Center of Andalucía), as a subsidiary department of the Instituto de Microelectrónica de Barcelona (Barcelona Microelectronics Institute). Later, in 1996, it was established by the Governing Board of the CSIC as a Training Institute, occupying a building next to the CICA ceded by the Junta de Andalucía. In late 2008, the Institute was enlarged and relocated in new premises purpose-built by the CSIC in the Parque Científico y Tecnológico Cartuja (Cartuja Scientific and Technological Park).

The IMSE-CNM staff consists of approximately one hundred people, including scientists and support personnel. Most of them work for the CSIC and the Universidad de Sevilla. IMSE-CNM employees are involved in advancing scientific knowledge, designing high level scientific-technical solutions and in technology transfer. Their duties include research and teaching activities, the latter mainly taking place at the University.

Projects undertaken at IMSE-CNM mostly correspond to EU research initiatives, national R+D plans and research plans funded by the Junta de Andalucía. They focus primarily on implementing innovative concepts in silicon, using either the Instituto de Microelectrónica de Barcelona (IMB-CNM)'s own clean room or external foundries mainly from Europractice or CMP IC services.

The Institute also participates in several technology and knowledge transfer activities with microelectronics companies, at both national and international level. These activities take the form of collaboration in numerous research contracts, the organization of training courses and the provision of scientific and technical consultation services for companies and government departments.

DIRECTIONS

The Instituto de Microelectrónica de Sevilla (IMSE) is located in the Parque Científico y Tecnológico Cartuja (Isla de La Cartuja) (Cartuja Scientific and Technological Park), at the corner of Calle Americo Vespucio and Calle Leonardo da Vinci.

Seville is easily accessible by any of the forms of transport detailed below:

- **Plane**: San Pablo Airport, A-4, Km 532
- **Train**: Santa Justa Station, Kansas City Av, s/n.
- **Bus**: Plaza de Armas Station (Cristo de la Expiración Av, s/n) and Prado de San Sebastián Station (Prado de San Sebastián).
- **Road**: A-4, Madrid (538 km) / A-92, Málaga-Granada (219-256 km) / A-4, Cádiz (125 km) / A-49, Huelva (94 km) / A-66, Mérida (197 km)

To reach the Institute you can use:

- **Taxi service**: Radiotaxi: 954580000 / Teletaxi: 954622222 / Radiotaxi Giralda: 954675555.
- **Bus service**: Lines C1 or C2, with a stop at the nearby Faculty of Communication; these lines also have a stop at the Santa Justa train station.
- **Local trains**: Train C-2, connecting Santa Justa station with nearby Cartuja station.
- **Bicycle**: The infrastructure of bike lanes and bike hiring services are managed by Sevici. Bicycle parking is available in front of the IMSE building.
- **Walking**: You can come walking from the city center, across the river by the Barqueta Bridge.

Instituto de Microelectrónica de Sevilla
Centro Nacional de Microelectrónica

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VISITING IMSE

A visit to the Instituto de Microelectrónica de Sevilla will help students, teachers, and citizens in general getting first-hand knowledge about the world of research and development in modern microelectronics.

To visit IMSE, please contact us by email to *visitas@imse-cnm.csic.es*, or call us on +34 954 466666.

ORGANIZATION

The Instituto de Microelectrónica de Sevilla (IMSE-CNM) is a research center belonging to the Consejo Superior de Investigaciones Científicas (CSIC - Spanish National Research Council). Its current administrative status is that of a full-fledged CSIC facility, with significant participation by scientists from the Universidad de Sevilla.

The IMSE-CNM management structure is as follows:

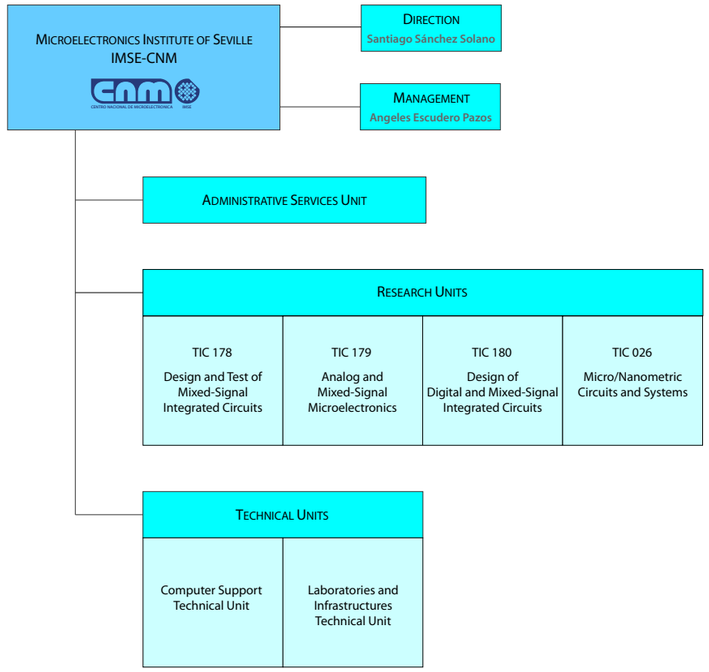
- Direction: Santiago Sánchez Solano (*direccion.ims-cnm@csic.es*)
- Management: Ángeles Escudero Pazos (*gerencia.ims-cnm@csic.es*)
- Administrative Services Unit

The Institute's research activities are carried out by Research Units responsible for project development. There are currently four of these units, corresponding to different Junta de Andalucía TIC Groups:

- TIC-178: Design and Test of Mixed-Signal Integrated Circuits
- TIC-179: Analog and Mixed-Signal Microelectronics
- TIC-180: Design of Digital and Mixed-Signal Integrated Circuits
- TIC-026: Micro/Nanometric Circuits and Systems

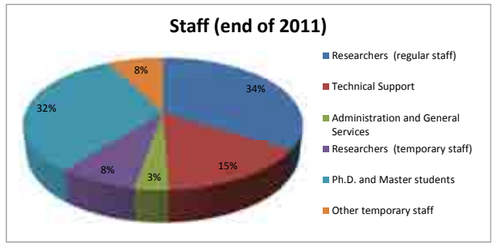
The Institute's infrastructure is also supported by two Technical Units:

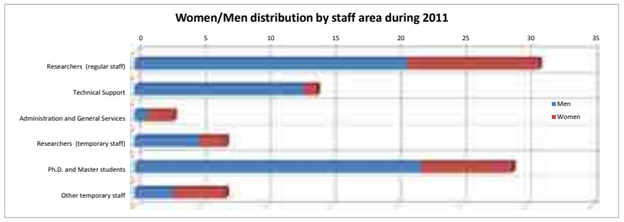
- Computer Support Technical Unit
- Laboratories and Infrastructures Technical Unit

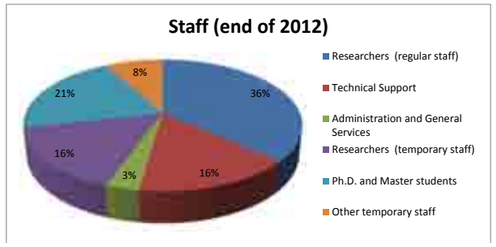


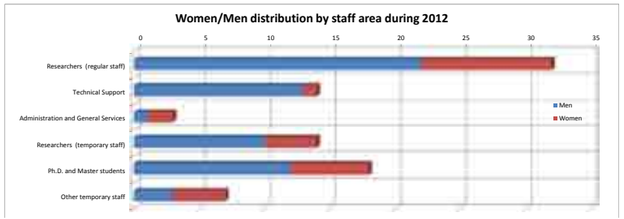
HUMAN RESOURCES

The personnel at the IMSE-CNM permanently or temporarily engaged in the Institute's activities includes nearly 100 people. Most of them work for the CSIC and the Universidad de Sevilla, but there are also teachers and students from other organisms on research internships. These internships do not imply any kind of employer-employee relationship with the CSIC.



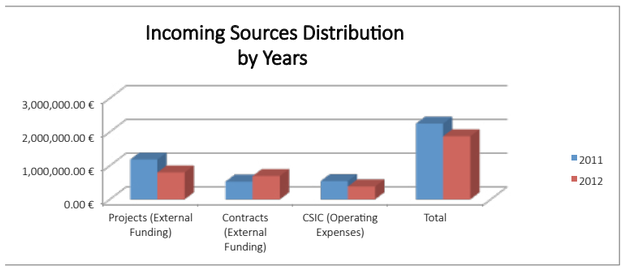


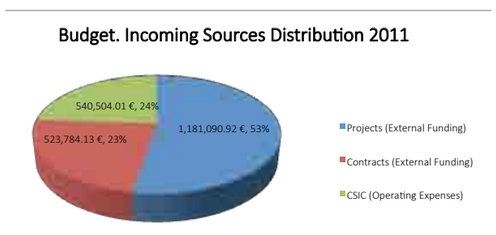


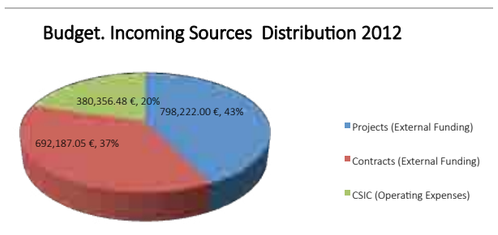


BUDGET

Incoming resources, distributed by concepts, for years 2011 and 2012 are shown in the following graphs (excluding staff costs). External funding is obtained either from competitive public projects or industrial contracts. Operating expenses are provided by CSIC.







INFRASTRUCTURE

LABORATORIES

IMSE-CNM has its own laboratories and workshops, specifically habilitated for research, development and innovation tasks carried out at the Institute. The laboratories are well fitted out with equipment and instrumentation, and are run by a permanently employed team of specialists.

Head of Unit

Juan Ramos Martos
jramos@imse-cnm.csic.es

Laboratory Manager

Joaquín Ceballos Cáceres
joaquin@imse-cnm.csic.es

Device Characterization Laboratory
Chief Technician: Juan Manuel Repiso (*repiso@imse-cnm.csic.es*)

This lab, equipped with high performance LCR meters and Semiconductor Parameter Analyzers, is mainly devoted to the characterization of passive and semiconductor devices. It also has a Climatic Chamber for testing systems and devices at temperatures ranging from -70ºC to 180ºC, and a Probe Station for acquiring internal signals both from already packaged circuits and directly form on-wafer circuits at frequencies of up to 1 GHz.

Optoelectronics Laboratory
Chief Technician: Elisenda Roca (*eli@imse-cnm.csic.es*)

This lab is equipped with the instrumentation needed to characterize visible light sensors and integrated circuits made up of discrete sensors or visible light matrices. A dark chamber is also available for sensor characterization.

Radiofrequency Laboratory
Chief Technician: Rafaella Fiorelli (*fiorelli@imse-cnm.csic.es*)

Apart from the general radiofrequency and microwave instrumentation for measuring frequencies of up to 26GHz, this lab is also equipped with an Anechoic Chamber. The facility, capable of measuring directivity, sensitivity and radiation patterns, etc. for low gain antennas at frequencies ranging between 700 MHz and 18 GHz, provides a powerful tool for designing devices over a wide range of RFs. An RF Cascade Microtech Probe Station with on-wafer and on-PCB test capability is also available in the lab.

Mixed-Signal Test Laboratory
Chief Technician: Juan Manuel Repiso (*repiso@imse-cnm.csic.es*)

This laboratory is the largest at the IMSE. It has twelve mobile, fully reconfigurable test booths for analogue, digital and mixed-signal devices. Twelve additional mobile carts carrying different specific instruments can be incorporated to each workbench according to specific measurement requirements.

Pulsed Laser Laboratory
Chief Technician: Gildas Léger (*leger@imse-cnm.csic.es*)

This laboratory is devoted to the study of the single-event effects (SEEs) produced by high energy particles in semiconductor devices and circuits. To study these effects, single-photon techniques and 1064-nm wavelengths are used, both of which are very suitable analyzing SEEs in medical, nuclear and space-related applications.

ATE Agilent 93000
Chief Technician: José Miguel Mora (*jmiguel@imse-cnm.csic.es*)

The principal piece of equipment in this lab is the Agilent 93000 C200e SOC Test System. It is mainly used here as a prototype test unit, although it is very capable of testing a huge number of samples simultaneously. Using the system in this way, the IMSE technical staff has acquired sufficient expertise to be able to offer external consultation services (technical support and training) on how this equipment can be used to design test boards for the implementation and debugging of test procedures in both analog and digital domains.

Complex Systems Workshop
Chief Technician: Juan Manuel Repiso (*repiso@imse-cnm.csic.es*)

This lab was designed to accommodate those systems which, due to either their size or their special characteristics, require greater space or an isolated environment. This workshop also has a hazardous chemicals cabinet and a security cabinet in which to store these products.

Packaging Workshop
Chief Technician: Juan Manuel Repiso (*repiso@imse-cnm.csic.es*)

This room is devoted to bonding chip and package. It has all the required resources necessary to meet the challenges posed by deep-submicron technologies, allowing connections with pitch sizes as low as 50 µm. This workshop also features two semi-automatic ultrasound micro-soldering machines, with thread diameters of up to 17 µm, for ball-bonding and wedge-bonding. To verify the quality of connections, there is also a micro-soldering test system for evaluating thread-resistance and solder ball shear. The lab also has two semiconductor storage units for keeping ICs at optimal temperatures and levels of humidity.

Special Assembly Workshop
Chief Technician: Miguel Ángel Lagos (*mlagos@imse-cnm.csic.es*)

The Special Assembly Workshop has equipment for soldering and desoldering high density packaging components, such as BGAs, mini-BGAs and fine-pitch surface-mount components.

PCB Assembly Workshop
Chief Technician: Juan Manuel Repiso (*repiso@imse-cnm.csic.es*)

The PCB Assembly Workshop has all the equipment needed for soldering and desoldering thru-hole circuits mounted on PCBs, perforated matrix plates, and, in general, on any circuit-test development plates that do not require special welding techniques.

INFORMATION TECHNOLOGY

The IMSE-CNM IT infrastructure was established to support research, development and innovation in the design and testing of integrated circuits, and to help the Institute control its lab equipment and other general-purpose applications more efficiently.

Structured as several virtual local networks (VLAN) with different security features and levels, it is capable of supporting all the different design tools and services available at the Institute.

Head of Unit & System Administrator

Adrián Estrada Pérez
estrada@imse-cnm.csic.es

Research Network

This network comprises a set of Solaris servers, storage systems and user terminals which facilitate implementation of the Institute's various activities, and a Linux cluster system for accelerating the different stages in the integrated circuit design process. More specifically, its features include:

- A central Sun server plus four Solaris-based departmental servers
- A Linux cluster made up of 15 RedHat-based units
- Workstations, PCs and Sun Ray network terminals
- A disk storage system and a backup tape library

Laboratory Network

This network connects the general purpose computers installed in the Institute's different laboratories which are used for data acquisition tasks, control, instrumentation and the automation of test processes. It also includes lab instrumentation with operating systems and communication interfaces similar to those of conventional computers such as:

- PCs
- Logic Analyzers
- Modular Analysis Systems
- Wave generators
- Arbitrary Function Generators
- Oscilloscopes

Virtualized Services Network

This network is based on an IBM BladeCenter virtualization system comprising four Blade servers, and features:

- Windows Applications
- Long Term Storage
- Remote Access Interface
- Support computer rooms

Administrative Services Network

This network comprises two application servers in a redundant configuration and eight clients. It supports the management programs, databases and office applications used by the Institute's administrative services.

Demilitarized Zone (DMZ)

This is the perimeter network made up of all the systems and services requiring access from outside the building:

- Web server
- Email Server
- VPN access server
- System for training sessions corresponding to the Master in Microelectronics

NETWORKING AND COMMUNICATIONS

IMSE's IT Support Unit administers and manages local area network and IP address routing completely autonomously. As a research center belonging to the CSIC (Spanish National Research Council), the IMSE connects to the Internet through the CICA (Scientific Computer Centre of Andalusia) via a dedicated, 1 Gb/s fiberoptic link.

The network is based on Twisted Pair cabling, shielded in certain areas of the laboratories and, gathered together in communications racks on each floor. It supports a local area network of more than 400 connection points, all of which support speeds of up to 1 Gb/s.

The IMSE also provides primary network services for the Centro Andaluz de Biología Molecular y Medicina Regenerativa (CABIMER - Andalusian Center for Molecular Biology and Regenerative Medicine) and to the Estación Biológica de Doñana (EBD - Doñana Biological Station).

Wi-Fi Network

To provide access to systems with wireless interfaces and support Fast Ethernet connections with the computers on the communications network, 6 access points have been installed. These connections are also available through the Eduroam network, thus further facilitating mobility for wireless users.

Internet Access

The computer network connecting IMSE-CNM to the other CSIC institutes located in the vicinity and to the whole Spanish R&D network (RedIRIS) operates via two fiber-optic connections. One of these links the CSIC centers in Cartuja directly to CICA while the other connects the CSIC centers to the Universidad de Sevilla network.

VPN Access

To increase the security level of the IMSE computer network, a mechanism has been put in place to remotely access the IMSE-CNM via a virtual private network (VPN) using personal digital certificates.

VoIP

As an alternative to conventional telephone communications, an IP based telephony solution has been installed. This solution, besides offering a wide range of integrated services, takes full advantage of the building's infrastructure by sharing voice and data communications on the same wiring system.

CAD TOOLS

Most of the software tools used at the IMSE-CNM are design tools which cover several stages of the integrated circuit design process, from automatic HDL-based synthesis to the completion of full-custom layouts. As a member of the European consortium EUROPRACTICE, IMSE-CNM holds many of the licenses required by these design tools. The CAD software tool library at IMSE-CNM also includes in-house CAD tools and free-distribution tools from universities and other research centers.

CAD Manager

Dolores Vázquez Boza
lola@imse-cnm.csic.es

COMMERCIAL TOOLS

Cadence Design Framework II
Analog and digital semi/full-custom design

Cadence provides a complete integrated circuit environment allowing both analog design flows (schematic capture, electrical simulation, layout editing, design rule checking, parasitic extraction, LVS verification, etc.) and digital flows (functional description, automatic synthesis, logic simulation, automatic place & route, etc.). The environment also includes tools and languages for describing and simulating mixed analog-digital designs (AHDL, hierarchy editor, etc.).

Mentor Graphics
Analog and digital semi/full-custom design

Mentor Graphics provides a complete integrated circuit environment allowing full digital design flow (functional description, automatic synthesis, logic simulation). This tool also covers semi-custom and full-custom layout design.

Synopsys
Simulation and VHDL synthesis

Synopsys provides a series of HDL simulation and synthesis tools (VHDL and Verilog) for designs in both ASIC and FPGA technologies. The current distribution of this tool includes also packages for high-level synthesis, low-power synthesis, design for testability, test files and test vector generation, formal verification, temporal analysis and the use and development of IP modules.

Xilinx
FPGAs development

Xilinx provides different tools for FPGA system design: Integrated Software Environment (ISE), a basic set of tools that facilitates the description, synthesis, implementation and verification of designs created on Xilinx CPLDs and FPGAs; Embedded Development Kit (EDK) for programmable embedded system design; ChipScope Pro, which makes it possible to display all the signals and internal nodes of an FPGA; and DSP System Generator, for developing digital signal processing systems on FPGAs.

Saber
Electrical simulator for mixed-signal designs

Among other utilities, this includes: SaberHDL, a tool for simulating complex mixed-signal systems or technologies; SaberDesigner, for creating and editing designs, controlling simulations interactively and displaying and analyzing waveforms; SaberGuide, for behavioral simulation; SaberSketch, a graphical user interface; and MAST, a mixed-signal hardware description language.

Coventor
Integrated development of systems combining ICs and MEMS devices

This software package implements an integrated platform for designing, simulating and developing products with MEMS and MEMS+ technology. It allows designers to integrate behavioral models for MEMs using a 3D graphical interface and to simulate them using MATLAB Simulink or Cadence Virtuoso.

Agilent Advanced Design System
Design tool for high frequency design

The Advanced Design System (ADS) is an electronic design automation tool for RF, microwave and signal integrity applications. It uses cutting edge technologies such as 3D EM and X-parameter simulators. This tool is used by leading developers of wireless applications for communications and networks, and also by leading aerospace and defense technology companies. In one single integrated platform ADS provides design and verification standards, with wireless design libraries and EM circuit-system co-simulation, for WiMAX, LTE, multi-gigabit links and radar and satellite communications applications.

Coware
Hardware-software codesign

CoWare is a System-C based graphical design tool for concurrent system-on-chip design with embedded software, allowing optimal creation and implementation of virtual hardware platforms for software development and validation. CoWare supports processor design, application subsystems, DSPs, algorithms, etc. It also allows platform verification during software development.

Hspice
Electrical simulator

The standard tool for simulating circuits at electrical level, this simulator makes it possible to incorporate certified device models from leading MOS device manufacturers. Featuring latest--generation simulation and analysis algorithms, it has become one of the most reliable and best known industrial circuit simulators.

Matlab/Simulink
High-level technical computing language and interactive prototype design and development. Dynamic and embedded multi-domain simulation environment

MATLAB is a high-level technical computing language and an interactive platform for algorithm design, numerical computation and data analysis and visualization. Simulink is a tool for multi-domain simulation and design based on dynamic and embedded system models.

IN-HOUSE CAD TOOLS

Xfuzzy
Design of fuzzy-inference systems

Xfuzzy, the design environment for fuzzy systems, includes a set of tools that help with the design of fuzzy-logic inference-based systems, from initial description right through to final implementation. Based on the XFL specification language, Xfuzzy has tools for describing, verifying and synthesizing fuzzy systems (both software and hardware). It also features tools which allow the easy editing of package operators and hierarchical structures, tools for generating 2-D and 3-D data graphics and tools for monitoring inference processes.

SIMSIDES
SIMulink-based SIgma-DElta Simulator

SIMSIDES is a time-domain behavioral simulator for ΣΔMs that was developed as a toolbox in the MATLAB/SIMULINK environment. SIMSIDES can be used for simulating any arbitrary ΣΔM architecture implemented with discrete-time (DT) or continuous-time (CT) circuit techniques.

Fridge
Circuit optimization using simulated annealing techniques

FRIDGE is an analog circuit optimization tool with many innovative features. It was developed to streamline the process of designing integrated circuits. FRIDGE is used to size analog circuits automatically according to the designer's requirements. The optimization process takes place in two stages: in the first, statistical optimization techniques are applied, while deterministic techniques are applied in the second. Computational costs are drastically reduced by correctly formulating the cost function (where the designer's requirements are established) and adjusting the movement generator to match the nature of the analog sizing problem. All this can be done thanks to FRIDGE's innovative features, which include: preliminary exploration of the design space using a coarse grid to determine the best regions for further exploration, adaptive control of the temperature in the simulated annealing statistical techniques, synchronization of movement amplitude in parameter space with the temperature, etc.

RESEARCH LINES

The Instituto de Microelectrónica de Sevilla is structured into four Research Units whose scientific objectives focus primarily on the implementation and experimental verification of innovative concepts related to the design of micro- and nano-electronic circuits and systems.

The research lines developed at IMSE-CNM aim to provide solutions both in traditional sectors, such as communications, processing systems or instrumentation, and in emerging sectors, such as medical engineering, environment or space technology. These lines also consider the introduction of new devices, such as nano-sensors and micro-electromechanical systems (MEMS), and the use of unconventional computing paradigms, such as neural networks or fuzzy logic.

20 ***Research Unit of*** DESIGN AND TEST OF MIXED-SIGNAL INTEGRATED CIRCUITS

22 Analog, Mixed-Signal (AMS) and RF Circuits and Systems

24 Testing and Design-For-Test Techniques for Analog, Mixed-Signal and RF Circuits

26 Biomedical Circuits and Systems

28 Circuit Design Using Emerging Devices and Non-Conventional Logic Concepts

31 Neuromorphic Systems

34 Design Methodologies For Space Applications

36 ***Research Unit of*** ANALOG AND MIXED-SIGNAL MICROELECTRONICS

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44 Wireless Implantable and Wearable Intelligent Biosensor Devices

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58 Digital Embedded Systems

60 Microelectronic Systems for Computational Intelligence

62 Microelectronics For Security

64 ***Research Unit of*** MICRO/NANOMETRIC CIRCUITS AND SYSTEMS

66 Adaptive/Reconfigurable Nanometer CMOS Analog/ RF ICs and Systems for Multi-Standard Wireless Transceivers and SDR

68 High-Efficiency Sigma-Delta Data Converters

70 Mixed-Signal Integrated Circuits for Space Applications

72 High Performance Acoustic Micro Electromechanical Systems (MEMS)

74 Design Technologies for Analog, Mixed-Signal, RF and Heterogeneous Circuits and Systems

Research Unit of

DESIGN AND TEST OF MIXED-SIGNAL INTEGRATED CIRCUITS

RESEARCH LINES

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PEOPLE

1. Yaisel L. Domínguez Cordero
2. Cristina Aledo González
3. Juan Núñez Martínez, PhD
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10. Gloria Huertas Sánchez, PhD
11. Eduardo Peralías Macías, PhD
12. Teresa Serrano Gotarredona, PhD
13. Ricardo Doldán Lorenzo, PhD
14. Diego Vázquez García de la Vega, PhD
15. Adoración Rueda Rueda, PhD
16. Joaquín F. Ceballos Cáceres

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ANALOG, MIXED-SIGNAL (AMS) AND RF CIRCUITS AND SYSTEMS

KEYWORDS

Analog design
Analog-to-digital converters
Radio frequency front-end
Digital calibration
Self-correction
Wireless and space applications

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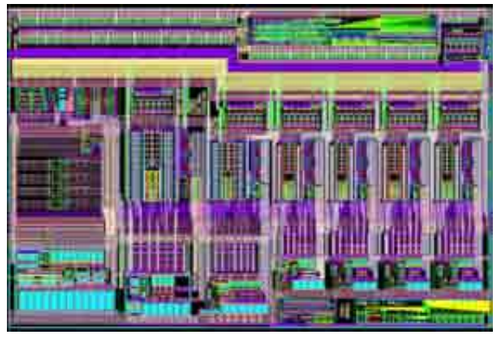
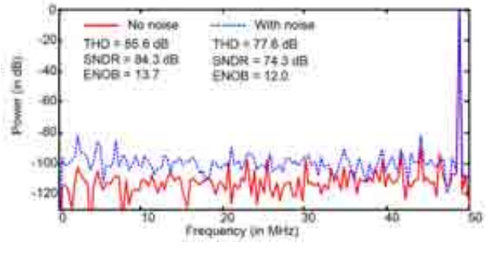
The activities in this research line are related to design techniques and methodologies for analog, mixed-signal and radio frequency circuits in advanced CMOS technologies, with special emphasis on Analog-to Digital Converters (ADCs) and IPs for demanding low-power, high-resolution and high-speed signal processing applications.

Concepts such as robustness against technological and environment variability, digital calibration, self-correction, and self-tuning are also developed in the context of advanced systems for wireless communication and space applications.

Recent activities concern:





1.8V 15-bit 100Msps Pipeline ADC: layout and post-layout simulation results of Nyquist performance with and without transient noise.

- Background digital calibration techniques for ADCs to increase their performance and their robustness against technological and environment variability
- Calibration for pipeline A/D converters with emphasis in background techniques
- Design of high resolution low-power mixed-signal CMOS IPs for space applications
- Design methodology for RF front-end optimization considering power and noise trade-offs
- Design of low-power CMOS RF front- ends for wireless applications
- New techniques to evaluate the sensitivity of mixed-signal circuits to Single-Event Effects

RESEARCH HIGHLIGHTS

A. J. Ginés, E.J. Peralías and A. Rueda.**"Novel Swapping Techniques for Background Calibration of Capacitor Mismatching and amplifier finite DC-gain in Pipeline ADCs"**. *Analog Integrated Circuits and Signal Processing, vol 57, pp. 57-68. Kluwer Academic Publisher. 2008, ISSN 0925-1030.*

A. J. Ginés, R. Doldán, A. Villegas, A. J. Acosta, M. A. Jalón, D. Vázquez, A. Rueda, E. Peralías. **"A 1.2V 5.14mW Quadrature Frequency Synthesizer in 90nm CMOS Technology for 2.4GHz ZigBee Applications"**. *IEEE Asian Pacific Conference on Circuits and Systems APCCAS, Macao (China) Dec. 2008.*

G. Leger, A. J. Ginés, E. J. Peralías, A. Rueda, **"On Chopper Effects in Discrete time Sigma Delta Modulators"**, *IEEE Trans. on Circuits and Systems I, vol 57, nº 9, pp. 2438-2449. September 2010*

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A. Villegas, D. Vázquez, E. J. Peralías, A. Rueda, **"A 3.6mW @ 1.2V high linear 8th-order CMOS complex filter for IEEE 802.15.4 standard,"** *ESSCIRC 2011- European Solid-State Circuits Conference, pp. 99-102. Helsinki, Finlandia, 2011.*

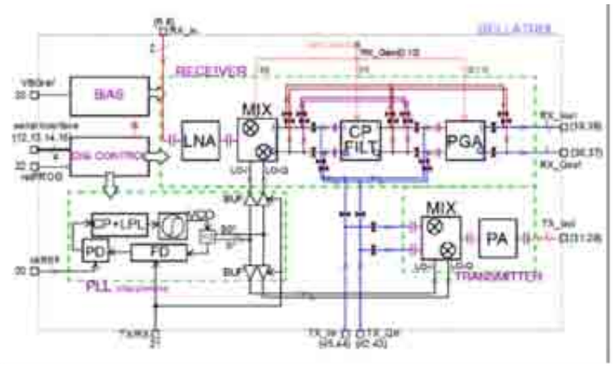
KEY PROJECTS & CONTRACTS

Adapting Mixed-signal and RF ICs Design and Test to Process and Evironment Variability (DANTE) (TEC2011-28302)
F Ministerio de Ciencia e Innovación (national public funding)
D 1/1/2012 - 31/12/2014
P Adoración Rueda Rueda

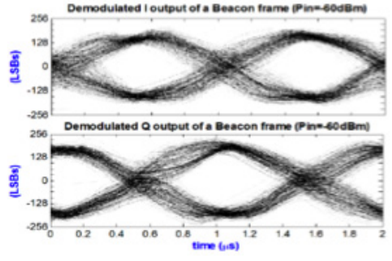
Self-calibration & Self-Test in Analog, Mixed-Signal and RF ICs (P09-TIC-5386)
F Junta de Andalucía - Proy. de Excelencia (regional public funding)
D 3/3/2010 – 3/2/2014
P Adoración Rueda Rueda

SR2 :Short Range Radio (2A105- Catrene) (TSI-020400-2008-71, TSI-020400-2010-55)
F Catrene European Program (European public funding) and MITyC Programa Avanza+ (national public funding)
D 1/2008 – 12/2011
P Adoración Rueda Rueda

F Funded by D Duration P Project leader



Prototype of a Zigbee/ IEEE 802.15.4 transciever, implemented in a 1.2V 90nm CMOS technology.



TESTING AND DESIGN-FOR-TEST TECHNIQUES FOR ANALOG, MIXED-SIGNAL AND RF CIRCUITS

KEYWORDS

Mixed-signal integrated circuits
Test
Testing
Design-for-Test (DfT)
Built-In-Selft-Test (BIST)

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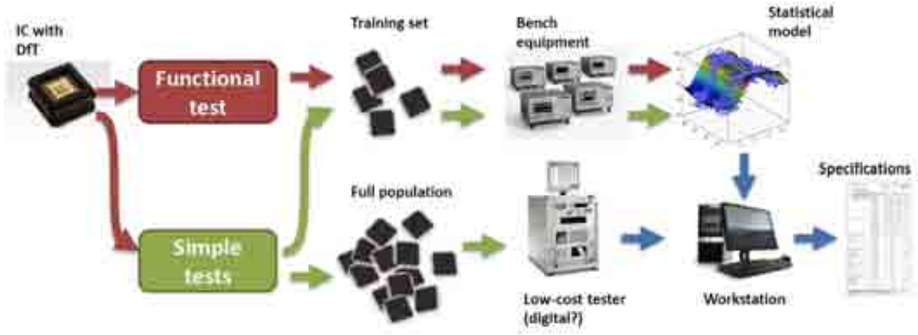
In general, this research line embraces all the activities related to the development of several simple and low-cost functional testing techniques and structural design-for-test in the context of advanced CMOS technologies and the development of BIST techniques to reduce test complexity and to manage access to the internal IP blocks in SoCs (Systems on Chip).

Main recent topics of interest are:

- On-line test and BIST for mixed-signal and RF components
- Characterization of periodic analog signals and on-chip generation of analog sinusoidal signals for application in analog and mixed-signal BIST
- Low cost testing techniques for Analog-to-Digital Converters
- Alternate test applied to mixed-signal circuits
- Extension of the OBT technique and its applications



Statistical post processing for Alternate Test. From a completely characterized subset of circuits, a machine-learning algorithm extracts the non-linear and multi-dimensional relations between simple signatures and specifications. This model is further used to test the rest of circuits with the simple signatures only.

RESEARCH HIGHLIGHTS

G. Leger, A. Rueda. **"Low-cost Digital Detection of Parametric Faults in Cascade Sigma-Delta Modulators"**. *IEEE Trans. on Circuits and Systems I, vol 56, nº 7, pp.1326-1338. July 2009.*

M. A. Jalón , A. Rueda, E. J. Peralías. **"Enhanced Double-histogram Test"**. *Electronics Letters, Vol 45, nº 7, 26th March 2009.*

M. A. Jalón, E. J. Peralías, **"ADC Non-Linearity Low-Cost Test Through A Simplified Double-Histogram Method"**. *Journal of electronic testing, pp 47-58, 2010.*

M. J. Barragán, D. Vázquez, A. Rueda, **"Analog Sinewave Signal Generators For Mixed-Signal Built-In Test Applications"**. *Journal of electronic testing, vol 27, 3, pp 305-320, 2010.*

A. J. Ginés, E. J. Peralías, A. Rueda, **" Blind Adaptive Estimation of Integral Nonlinear Errors in ADCs Using Arbitrary Input Stimulus"**. *IEEE Transactions on Instrumentation and Measurement, pp 452-461, January 2011.*

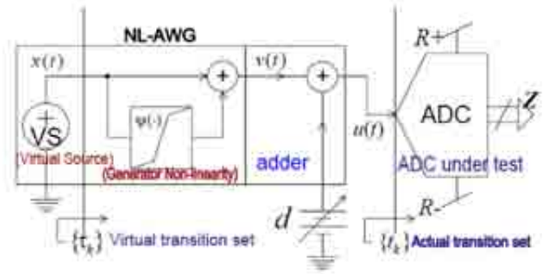
KEY PROJECTS & CONTRACTS

Adapting Mixed-signal and RF ICs Design and Test to Process and Evironment Variability (Dante) (TEC2011-28302)
- F Ministerio de Ciencia e Innovación (national public funding)
- D 1/1/2012 - 31/12/2014
- P Adoración Rueda Rueda

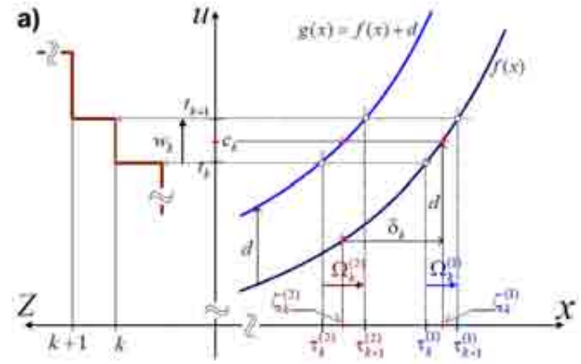
Self-calibration & Self-Test in Analog, Mixed-Signal and RF ICs (P09-TIC-5386)
- F Junta de Andalucía - Proy. de Excelencia (regional public funding)
- D 3/3/2010 - 3/2/2014
- P Adoración Rueda Rueda

TOEST: Towards One European Test Solution
- F CATRENE European Program – CT302 (European public funding)
- D 2009 - 2011
- P José Luis Huertas

F Funded by D Duration P Project leader



Measurement method for ADCs based on double-histogram. From the histograms (output code density) obtained for a non-linear monotonous input signal and its replica with an additive offset, the INL of a high-resolution ADC can be retrieved at low cost.



BIOMEDICAL CIRCUITS AND SYSTEMS

KEYWORDS

Biomedical Circuits and Systems
Bio-Sensors
Laboratory on-a-Chip (LoC)
Bioimpedance
Microelectrode

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This research line embraces all the activities related with the development of alternative bio-instrumentation circuits and systems required to reproduce classical and to propose new measurement techniques at bio-medical labs to improve the quality of acquired biosignals.

Targets design for bio-instrumentation systems are focused also to reduce the human effort and cost of biomedical assays, to obtain the minimum size and weight of biosystems (Lab-on-a-Chips, LoCs), to research new measurement methods based on high performance integrated circuits design with low-power consumption, wide bandwidth, reduced power supply levels and wireless communication capability. Electrical modeling of sensors required as signal transducers and interfaces must be incorporated to circuit design flow to obtain full system characterization. This research line also considers the modeling of heterogeneous systems for full system simulations.

Main recent activities are:

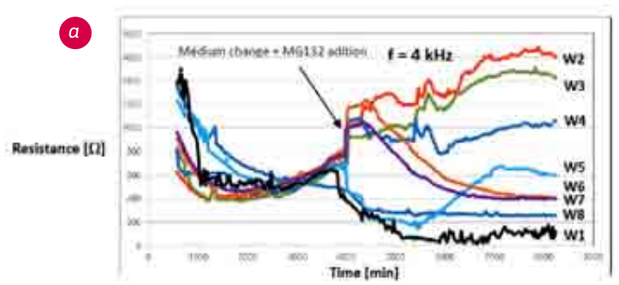
» Alternative bio-signals acquisition techniques

» Development of CMOS circuits and systems blocks

» To exploit classical sensors and look for new sensor issues for solving biosignals and biomarkers measurement problem

» Modeling sensor performance and incorporate it into heterogeneous system simulation in a full-system design process

» Developing multidisciplinary working skills



(a) Cell growing and toxicity curves for several dosis obtained by our group. It is represented the resistance measure with commercial sensors versus time. (b) Commercial sensors. (c) Photograph of a cell culture over a 250 µm diameter microelectrode.

RESEARCH HIGHLIGHTS

A. Yúfera, A. Rueda, **"A Close-Loop Method for Bio-Impedance Measurement with Application to Four and Two-Electrode Sensor Systems"** *Chapter 15 in New Developments in Biomedical Engineering, IN-TECH, Edited by: Domenico Campolo. ISBN: 978-953-7619-57-2, pp: 263-286. 2010.*

A. Yúfera, A. Rueda, **"Design of a CMOS Closed-Loop System with Applications to Bio-Impedance Measurements,"** *Microelectronics Journal, vol 41, n. 4, pp: 231-239, 2010.*

P. Daza, A. Olmo, D. Cañete, A. Yúfera, **"Monitoring Living Cell Assays with Bio- Impedance Sensors,"** *Sensors and Actuators B: Chemical. Elsevier, pp: 605-610, vol. 176. January 2013.*

A. Yúfera, D. Cañete, P. Daza, **"Modeling Microelectrodes Sensors for Cell Culture Monitoring"**, *IEEE Sensors Conference, Limerick, Ireland, 2011*

A. Yúfera, G. Huertas, A. Olmo, **"A Microscopy Technique Based on Bio- Impedance Sensors,"** *26th European Conference on Solid-State Transducers. Eurosensors 2012. pp: 1049-1052. Krakow. Poland. Sep. 2012.*

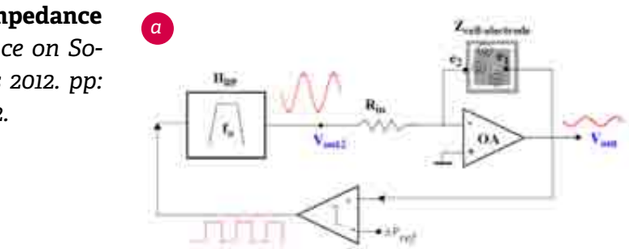
KEY PROJECTS & CONTRACTS

DANTE: Adapting Mixed-signal and RF ICs Design and Test to Process and Eviron-ment Variability (TEC2011-28302)
F Ministerio de Ciencia e Innovación (national public funding)
D 1/1/2012 - 31/12/2014
P Adoración Rueda Rueda

Self-calibration & Self-Test in Analog, Mixed-Signal and RF ICs (P09- TIC-5386)
F Junta de Andalucía - Proy. de Excelencia (regional public funding)
D 3/3/2010 - 3/2/2014
P Adoración Rueda Rueda

Sistema Integrado para la Monitorización y Caracterización de Cultivos Celulares en Tiempo Real
F Universidad de Sevilla (regional public funding)
D 2012
P Alberto Yúfera García

F Funded by D Duration P Project leader



Proposed circuit blocks for bio-impedance sensing: (a) Oscillation Based Test (OBT) proposed technique: impedance magnitude is obtained from oscilacion frequency parameters. (b) Closed-loop approach: magnitude and phase are obtained from signals V_m and $V_{\square}$ respectively.

CIRCUIT DESIGN USING EMERGING DEVICES AND NON-CONVENTIONAL LOGIC CONCEPTS

KEYWORDS

Emerging Devices, Non Conventional Logic
Resonant Tunneling Diodes (RTDs)
Negative Differential Resistance (NDR)
MOS NDR, Tunnel Transistors, Memristor,
Monostable to Bistable Logic Operation (MOBILE), Nanopipelining, Threshold Logic,
Multi-Threshold Threshold Gates
Multi-Valued Logic (MVL)

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The research main target is the development, analysis and design of circuits using emerging devices and non conventional logic models. In particular, we explore circuit design based on Resonant Tunnel Diodes (RTDs). These quantum devices exhibit Negative Differential Resistance (NDR) in their I-V characteristic which is very attractive from the point of view of circuit design. The incorporation of RTDs into transistor technologies has demonstrated improved circuit performance: higher circuit speed, reduced component count, and/or lowered power consumption.

NDR supports implementation of logic functionality on the basis of the Monostable-to-Bistable operating principle (MOBILE). We investigate and exploit MOBILE operation from a double perspective:

1. MOBILE suits extremely well the implementation of non conventional threshold logic models. On its basis, efficient transistor-RTD gate topologies for threshold gates, multi-threshold gates, generalized threshold gates and multi-valued gates, able to implement complex functions, have been proposed, as well as design methodologies both in HFET-RTD and in CMOS-RTD technologies
2. MOBILE gates are self-latching allowing implementation of pipeline at the gate level (nanopipeline) without adding memory elements. Different clock schemes are being developed for these nano- architectures taking robustness into account.

NDR can be also exploited in simple circuits to obtain extremely complex non-linear behaviors. In particular, we explore its application to the implementation of analog dividers for high speed applications.

Emulation of NDR using transistor circuits (MOS-NDR) is also addressed. Different configurations have been explored which are applied to prototype RTD-based design concepts, but also in a number of CMOS applications including ultra-low power logic circuits or compact C-Mullers.

Recently, we have started to explore other emerging devices. In particular, we are working in the analysis of logic circuits realized with tunnel transistors and in the implementation of threshold logic with memristors.

RESEARCH HIGHLIGHTS

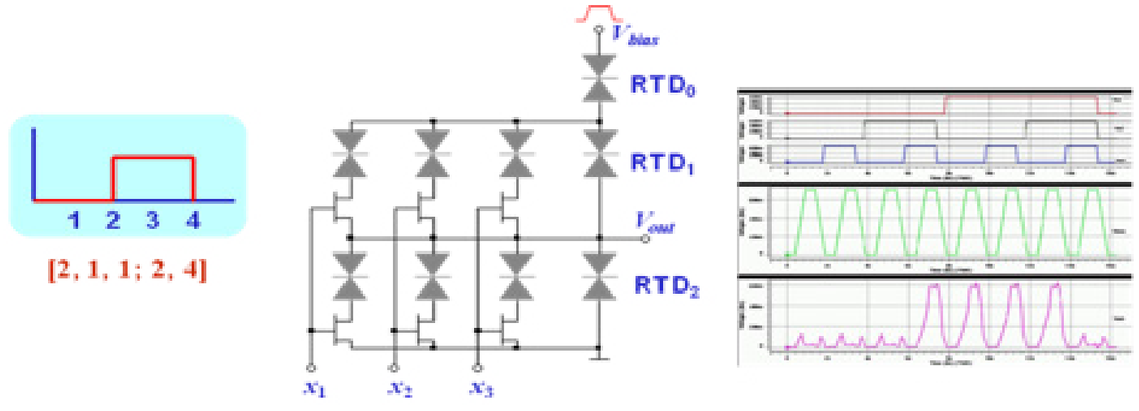
J. Núñez, M. J. Avedillo, J. M. Quintana, **"Two-Phase RTD-CMOS Pipelined Circuits"**. *IEEE Transaction on Nanotechnology. 11 - 6, pp. 1063 - 1069. 2012.*

H. Pettenghi, M. J. Avedillo, J. M. Quintana, **"Improved Nanopipelined RTD Adders using Generalized Threshold Gates"**. *IEEE Transaction on Nanotechnology. 10 - 1, pp. 155 - 162. 2011.*

J. Núñez, M. J. Avedillo, J. M. Quintana, **"RTD-CMOS Pipelined Networks for Reduced Power Consumption"**. *IEEE Transaction on Nanotechnology. 10 - 6, pp. 1217 -1220. 2011.*

M. J. Avedillo, J. M. Quintana, H. Pettenghi, **"Increased Logic Functionality of Clocked Series-Connected RTDS"**. *IEEE Transaction on Nanotechnology. 5 - 5, pp. 606 - 611. 2006.*

V. Beiu, J. M. Quintana, M. J. Avedillo, "**VLSI Implementations of Threshold Logic - A Comprehensive Survey**". IEEE Transactions on Neural Networks. 14 - 5, pp. 1217 -1243. 2003.



Link MTTG–MOBILE. Multi-Threshold Threshold Gates are implemented on the basis of the Monostable to bistable operation of clocked series-connected RTDs. In the figure circuit realization of $x_1+x_2x_3$

KEY PROJECTS & CONTRACTS

Arquitecturas y Circuitos con RTDS para Aplicaciones Lógicas y No Lineales (TEC2010/18937)

F PLAN NACIONAL I+D
Gobierno de España
(national public funding)
D 01/01/2011
P María José Avedillo de Juan

Diseño e Implementación de Circuitos Nano-Microelectrónicos Usando Dispositivos con Características NDR (TEC2007-67245/MIC)

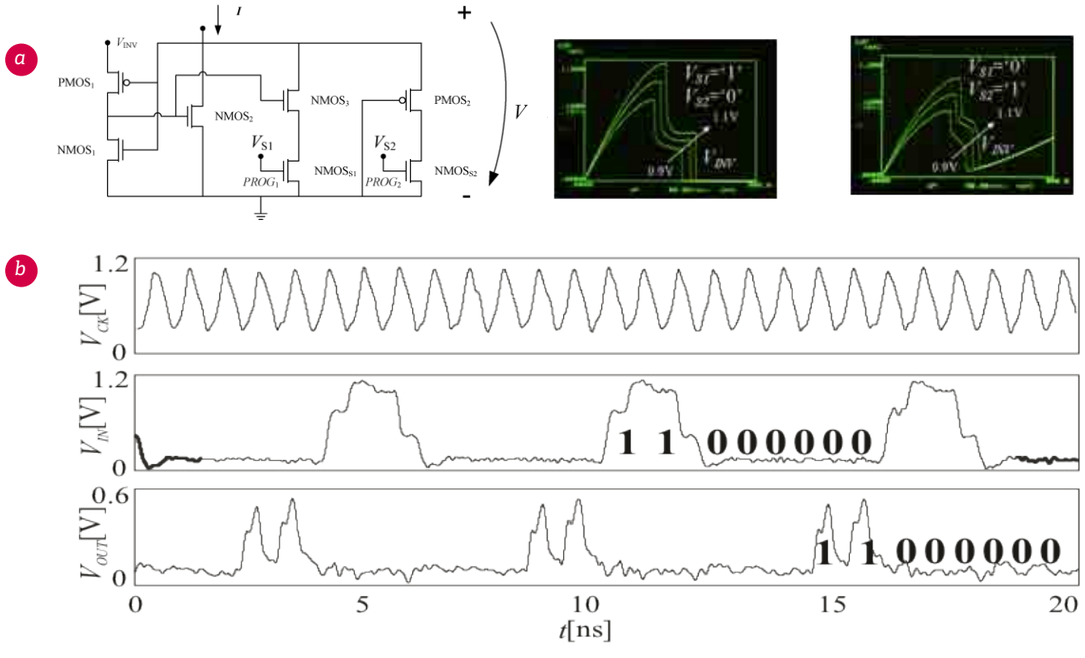
F PLAN NACIONAL I+D
Gobierno de España
(national public funding)
D 01/10/2007
P María José Avedillo de Juan

QUDOS: Quantum Tunneling Device Technology on Silicon

F CE (IST-2001-32358)
(European public funding)
D 01/01/2002
P Werner Prost
José María Quintana Toledo

F Funded by D Duration P Project leader

a) Programmable MOS-NDR exhibiting Negative Differential Resistance b) Experimental results of a two-phase MOBILE-based gate-level pipelined network implemented with MOS-NDR devices.



NEUROMORPHIC SYSTEMS

KEYWORDS

Spiking neural circuits, Spiking signal processing
Spike based learning, Pulsed neural networks
Address Event Communication (AER)
Spiking learning, Spike Time Dependent Plasticity
Low power, Frame-free vision sensing and processing
Convolutional Neural Networks

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The IMSE Neuromorphic group develops sensory and processing microchips that mimic sensing and processing in biological beings. It also develops multi-chip and hybrid chip-FPGA systems to scale up to higher complexity systems. The group also works on algorithms and sensory processing for spiking information sensing, coding and processing. Chips use mixed signal, low current, and/or low power, circuit techniques, as well as high speed communication techniques. The group uses mixed or digital CMOS technologies, as well as application projections exploiting emergent nanoscale technologies or new devices like memristors.

At present, the group focuses mainly on event-driven (spiking) frame-free vision systems, developing sensing retinas for spatial or temporal contrast (such as DVS – Dynamic Vision Sensors), as well as event-driven convolution processors, which allow to assemble for example large scale spiking "Convolutional Neural Networks" for high speed object recognition. These chips and systems use AER (Address Event Representation) communication techniques.

Event-driven retinas do not produce sequences of still frames, as conventional video cameras do. Instead, each pixel senses light and computes a given property (spatial contrast, temporal change) continuously in time. Whenever this property exceeds a given threshold, the pixel sends out an event (which usually consists of the pixel x,y coordinate and the sign of the threshold), which is written onto one (or more) high speed bus with asynchronous handshaking. This way, sensors produce continuous event flows, and subsequent processors process them event by event.

RESEARCH HIGHLIGHTS

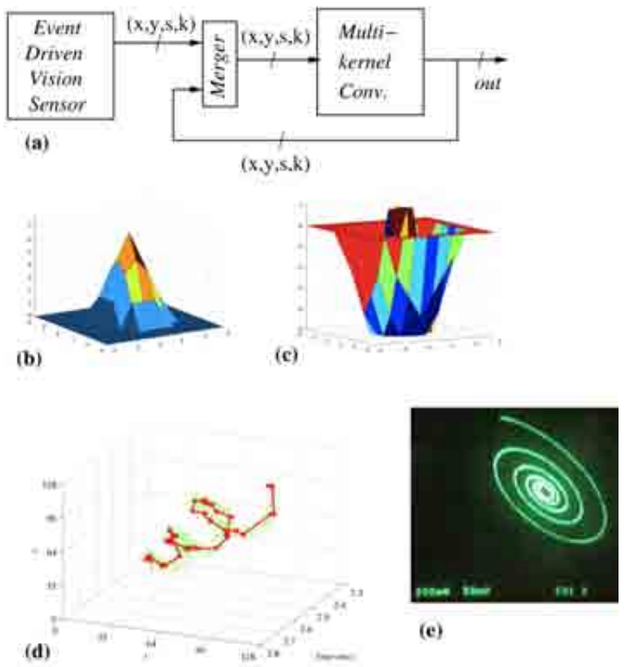
L. Camuñas-Mesa, C. Zamarreño-Ramos, A. Linares-Barranco, A. Acosta-Jiménez, T. Serrano-Gotarredona, and B. Linares-Barranco, **"An Event-Driven Multi-Kernel Convolution Processor Module for Event-Driven Vision Sensors,"** *IEEE J. of Solid-State Circuits, vol. 47, No. 2, pp. 504-517, Feb. 2012. (ieexplore)*

S. Chen, P. Akselrod, B. Zhao, J. A. Pérez-Carrasco, B. Linares-Barranco and E. Culurciello, **"Efficient feedforward categorization of objects and human postures with address-event image sensors,"** *IEEE Trans. on Pattern Analysis and Machine Intelligence, vol. 34, No. 2, pp. 302-314, Feb. 2012. (ieexplore)*

F. Alibart, S. Pleutin, O. Bichler, C. Gamrat, T. Serrano-Gotarredona, B. Linares-Barranco and D. Vuillaume, **"A memristive nanoparticle/organic hybrid synapstor for neuro-inspired computing,"** *Advanced Functional Materials, DOI: 10.1002/adfm.201101935, published online 13-Dec-2011.*

G. Indiveri, B. Linares-Barranco, T. J. Hamilton, A. van Schaik, R. Etienne-Cummings, T. Delbrück, S.-C. Liu, P. Dudek, P. Häfliger, S. Renaud, J. Schemmel, G. Cauwenberghs, J. Arthur, K. Hynna, F. Folowosele, S. Saïghi, T. Serrano-Gotarredona, J. Wijekoon, Y. Wang, K. Boahen, **"Neuromorphic Silicon Neuron Circuits,"** *Frontiers in Neuromorphic Engineering (inaugural issue), Front. Neurosci. 5:73. doi: 10.3389/fnins.2011.00073, 31 May 2011. (free open access link)*

"Circuito de ganancia de transimpedancia de bajo consumo y bajo desapareamiento para sistemas de fotosensado diferenciador temporal en sensores dinámicos de visión" *Inventors: Teresa Serrano Gotarredona, Bernabé Linares Barranco / Applicants: CSIC / Priority number: 201130862 / Priority date: 26.05.2011*



Event-based sensor-procesor with (a) retina-DVS and (b,c) multi-kernel convolutioner. It senses a (e) 500Hz spiral from the oscilloscope generating events (x, y, t) that represent (d) the spatio-temporal trajectory.

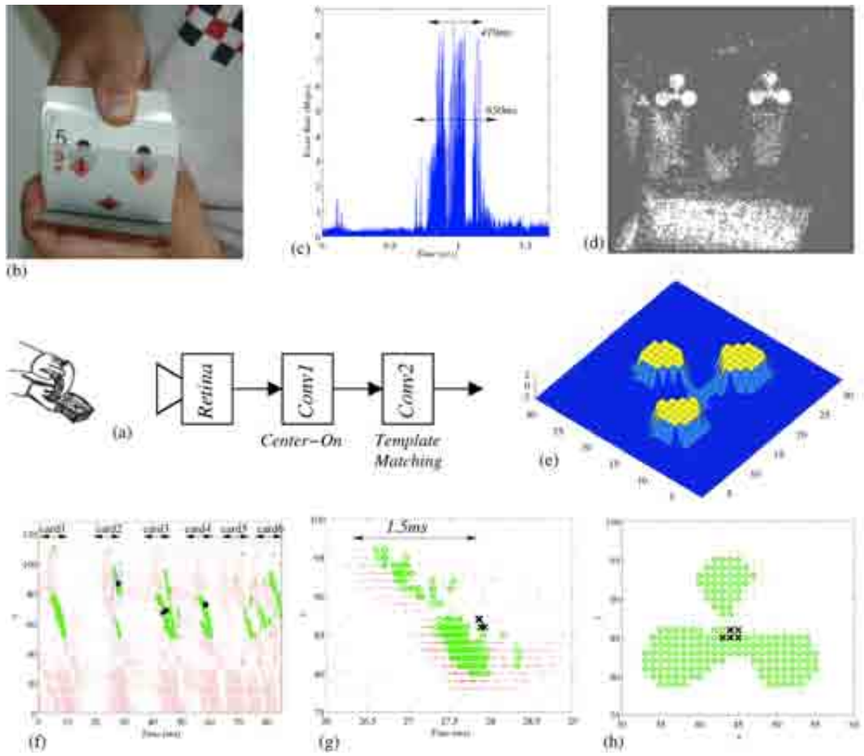
KEY PROJECTS & CONTRACTS

Convolution AER Vision Architecture (CAVIAR)
- F IST (VPM) (European public funding)
- D 06/2002 - 06/2006
- P Bernabé Linares Barranco (Consortium Coordinator)

Nanocomputing building Blocks with acquired Behaviour (NABAB)
- F ICT (FP7) (European public funding)
- D 04/2007 - 04/2010
- P Teresa Serrano Gotarredona (Consortium Coordinator)

Plasticity in Neural Memristive Architectures (PNEUMA)
- F ERANET Program (European public funding)
- D 09/2011 - 09/2014
- P Bernabé Linares Barranco

F Funded by D Duration P Project leader



Event-based shape sensing and recognition (a) system, (b) stimulus, (c) events, (d-f) output of the different stages, showing the real-time recognition of the clover pattern.

DESIGN METHODOLOGIES FOR SPACE APPLICATIONS

KEYWORDS

Radiation Hardening
Aerospace
Total Ionization Dose
Single Event Effects
CMOS Mixed-signal design

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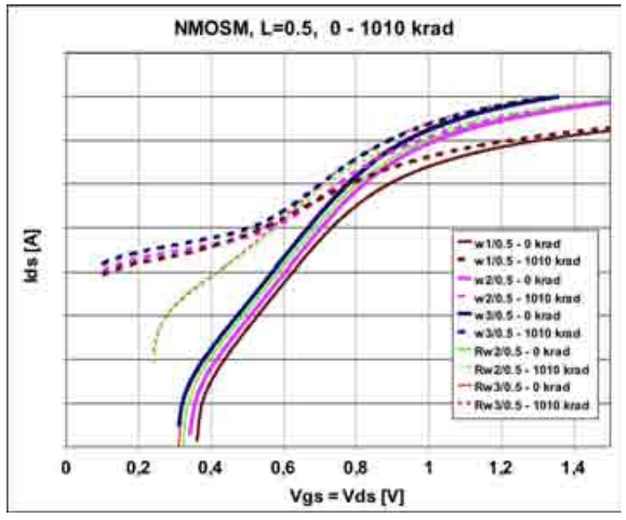
Circuits designed for aerospace need to take into account the effect on circuit operation of radiation and low temperature. This research line studies design methodologies to harden mixed-signal circuits against the long term (TID) and transient (SEE) effects of radiation. One technology (AMS 0.35µm CMOS) has been characterized and the results applied in the development of a RHBD digital library that is being used in the design of circuits for interplanetary missions. CMOS circuits for analog and digital rad-hard interfaces have been also developed.

This is a horizontal research line, aiming to develop design techniques adapted to the special environmental requirements of space applications, which can be combined with the specific knowledge in other vertical research lines developed in the Institute.



I_{ds}–V_{gs} characteristics for thick-oxide transistors with standard and hardened layouts.

RESEARCH HIGHLIGHTS

J. Ramos-Martos, A. Arias-Drake, A. Ragel-Morales, J. Ceballos-Cáceres, J. M. Mora-Gutiérrez, B. Piñero-García, M. Muñoz-Díaz, M. A. Lagos-Florido, and S. Espejo-Meana, **"Radiation Characterization of the austriamicrosystems 0.35 um CMOS Technology,"** *presented at the Radiation Effects on Circuits and Systems, RADECS, Sevilla, Spain, 2011.*

J. Ramos-Martos, A. Arias-Drake, A. Ragel-Morales, J. Ceballos-Cáceres, J. M. Mora-Gutiérrez, B. Piñero-García, M. Muñoz-Díaz, M. A. Lagos-Florido, and S. Espejo-Meana, **"Evaluation of the AMS 0.35 um CMOS Technology for Use in Space Applications,"** *presented at the Fourth International Workshop on Analog and Mixed-Signal Integrated Circuits for Space Applications, AMICSA, ESA/ESTEC, Noordwijk, The Netherlands, 2012.*

J. Ramos-Martos, A. Arias-Drake, A. Ragel-Morales, J. Ceballos-Cáceres, J. M. Mora-Gutiérrez, B. Piñero-García, M. Muñoz-Díaz, M. A. Lagos-Florido, S. Espejo-Meana, I. Arruego-Rodríguez, J. Martínez Oter, M. T. Álvarez, **"OWLs: A Mixed Signal ASIC for Optical Wire Less Links in Space Instruments"**, *presented at the Fourth International Workshop on Analog and Mixed-Signal Integrated Circuits for Space Applications, AMICSA, ESA/ESTEC, Noordwijk, The Netherlands, 2012.*

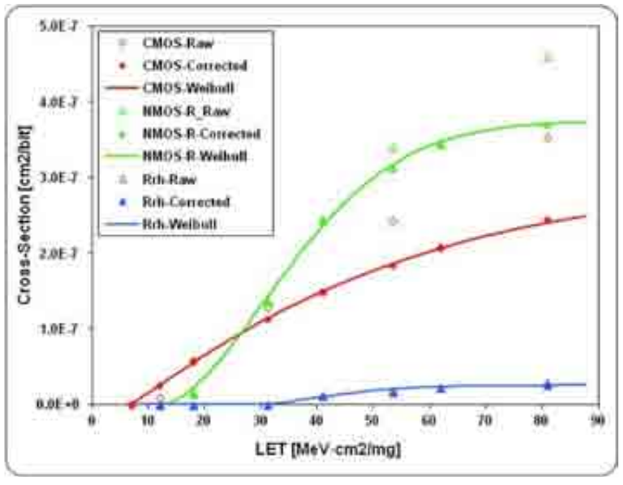
KEY PROJECTS & CONTRACTS

Radiation Tolerant Analogue/Mixed-Signal Technology Survey and Test Vehicle Design (ESTEC Contract No. 4000101621l0/NL/AF)
F European Space Agency (subcontract with ARQUIMEA) (European private funding)
D 18/9/2010 - 17/9/2012
P Gildas Leger

Diseño y Testado de ASICs para el Espacio para la Misión a Marte "MEIGA-METNET PRECURSOR" (AYA2008-06420-C04-02)
F Ministerio de Ciencia e Innovación (national public funding)
D 1/2009 - 12/2009
P Servando Espejo Meana

Mars Environmental Instrumentation for Ground and Atmosphere - MEIGA (AYA2009-1412-C05, AYA2009-1412-C05)
F Ministerio de Ciencia e Innovación (national public funding)
D 1/2010 - 12/2013
P Servando Espejo Meana

F Funded by D Duration P Project leader



Experimental results of SEU cross-section for standard, hardened and DICE registers.

Research Unit of

ANALOG AND MIXED-SIGNAL MICROELECTRONICS

RESEARCH LINES

40 Low-Voltage and Low-Power Analog and Mixed-Signal Design in Deep Submicron and Nanometer CMOS Technologies

43 Design of Analog-to-Digital Converters and Mixed-Signal Interfaces

44 Wireless Implantable and Wearable Intelligent Biosensor Devices

47 CMOS Smart Imagers and Vision Chips

50 Heterogeneous Sensory-Processing Systems and 3-D Integration

PEOPLE

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Óscar Guerra Vinuesa, PhD
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LOW-VOLTAGE AND LOW-POWER ANALOG AND MIXED-SIGNAL DESIGN IN DEEP SUBMICRON AND NANOMETER CMOS TECHNOLOGIES

KEYWORDS

Analog, Mixed-signal circuits synthesis
Modeling and design
Low-Voltage, Ultra Low-Power
High-Frequency, Communications
Sensor Interfaces, Calibration

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This research line embraces all activities related to the conception and design of basic building blocks and mixed-signal subsystems for system-on-chip implementation in CMOS nanometric technologies. Emphasis is placed on topologies and methods for low-voltage operation with very low power consumption. This is a transversal line whose activities intersect and provide support to the other research lines of the group. Typically building blocks and subsystems are designed for inclusion into chips implementing different system-level functions.

Activities in this line include:

- Conception of new topologies for analog and mixed-signal building blocks suitable for deep submicron technologies
- Modeling of second-order phenomena for these topologies. Embodiment of these models to support analog design flows
- Development of design plans aimed to achieving high-performance with minimum power budget
- Identification and exploration of fundamental limits and scaling performance of these building bocks
- Exploration of architectural solutions for low-power operation, including power optimization, power management, smart stand-by control, etc.
- Conception of optimum architectural solutions for block programmability, error correction and calibration

All application areas are covered, namely, from low-noise sensor interfaces to high-frequency communications. All major analog and mixed-signal functions embedded into systems are explored. The group has been active in analog and mixed-signal design since the late eighties and through these years have devised many different kind of building blocks for smart imaging chips, automotive sensors, wireline and wireless communications, RFID, neuro-fuzzy adaptive systems, etc.

RESEARCH HIGHLIGHTS

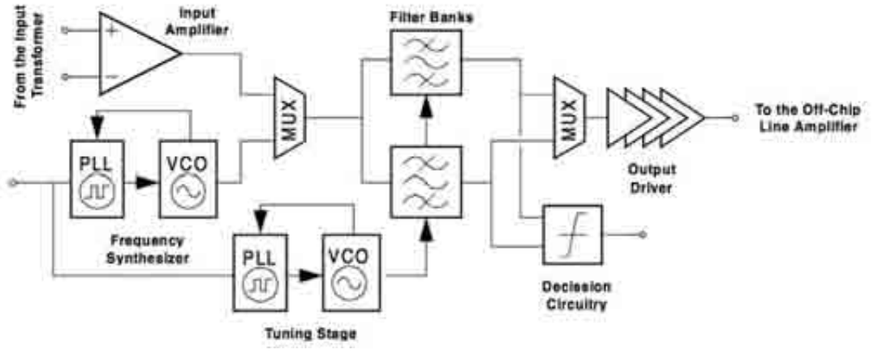
J. A. Rodríguez-Rodríguez, M. Delgado-Restituto, **"Advances in RFID Tags"**. *A. N. Laskovski (Ed.), ISBN: 978-953-307-678-4, InTech 2011. Chapter "A Low-Power Baseband Processor for Passive RFID Tags Employing Low-Power Design Techniques", 2011.*

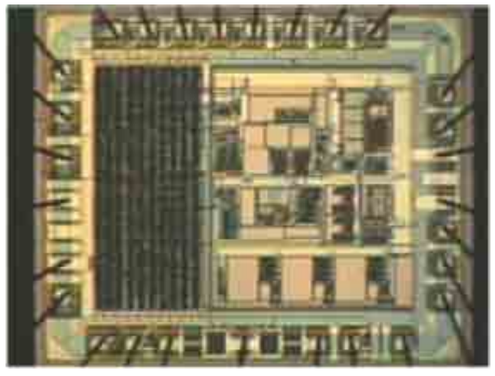
A. Rodríguez-Pérez, J. Ruíz-Amaya, M. Delgado-Restituto, A. Rodríguez-Vázquez, **"A low-Power Programmable Neural Spike Detection Channel with Embedded Calibration and Data Compression"**. *IEEE Transactions on Biomedical Circuits and Systems, Vol 6, pp. 87-100, April 2012.*

J. A. Rodríguez-Rodríguez, M. Delgado-Restituto, J. Masuch, A. Rodríguez-Pérez, E. Alarcón, Á. Rodríguez-Vázquez, **"An Ultra Low-Power Mixed-Signal Back End for Passive Sensor UHF RFID Transponders"**. *IEEE Transactions on Industrial Electronics, vol. 59, pp. 1310-1322. February 2012.*

J. Ruíz-Amaya, M. Delgado-Restituto, Á. Rodríguez-Vázquez, **"A 1.2V 10-Bit 60-MS/s 23mW CMOS Pipeline ADC with 0.67pJ/Conversion-Step and OnChip Reference Voltage Generator"**. *Analog Integrated Circuits and Signal Processing, vol. 71, Issue 3, pp. 371-381, June 2012; doi: 10.1007/s10470-011-9749-8.*

J. Fernández-Berni, R. Carmona-Galán, F. Pozas-Flores, Á. Zarándy, Á. Rodríguez-Vázquez, **"Multi-Resolution Low-Power Gaussian Filtering by Reconfigurable Focal-Plane Binning"**. *Proc. SPIE Vol. 8068, Prague, Czech Republic, 2011; doi: 10.1117/12.886555.*





A Mixed-Signal CMOS Modem ASIC for Data Transmission on the Low-Voltage Power Line.

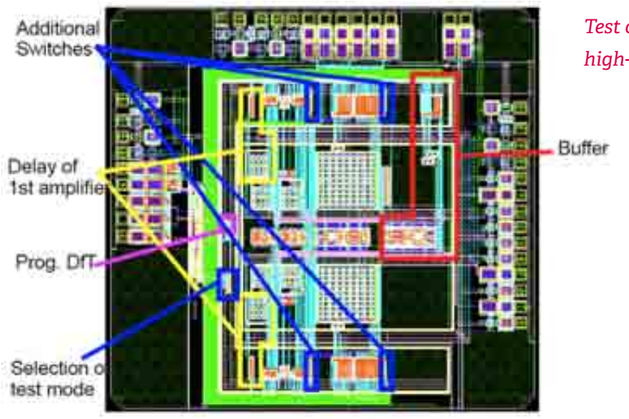
KEY PROJECTS & CONTRACTS

Mixed Mode in Deep Submicron Technologies (ESPRIT-29261)
- F European Union (European public funding)
- D 01/09/1998 – 31/08/2001
- P Ángel Rodríguez Vázquez

Aportaciones para la Implementación Monolítica de Dispositivos de Comunicación Inalámbricos con Consumos de Potencia Ultrabajos para Aplicaciones Biomédicas (TIC-02818)
- F Junta de Andalucía - Proy. de Excelencia (regional public funding)
- D 31/01/2008 – 31/12/2012
- P Manuel Delgado Restituto

Diseño Microelectrónico de un Sensor Lineal de Alta Velocidad para Aplicaciones de Inspección de Procesos Industriales (0619/0076)
- F Innovaciones Microelectrónicas (national private funding)
- D 10/01/2010 – 10/05/2011
- P Óscar Guerra Vinuesa

F Funded by D Duration P Project leader



Test cirtuitry for high-resolution ADCs.

DESIGN OF ANALOG-TO-DIGITAL CONVERTERS AND MIXED-SIGNAL INTERFACES

KEYWORDS

ADCs, DACs, Mixed-Signal Interfaces
Nyquist, Sigma-Delta
Pipeline, SAR
Current-Steering
Design Methodologies
Behavioral Modeling
Performance Optimization

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Research, development, and innovation regarding the implementation of high-performance mixed-signal interfaces, including front-end amplifiers, ADCs and DACs, in mainstream CMOS technological processes.

Covered activities include:

- Exploration of novel architectural and circuital techniques for ADCs and DACs that are specially suited for low-voltage low-power operation in deep-submicron and nanometer CMOS processes
- Modeling of second-order phenomena and exploration of fundamental operation limits and constraints
- Development of top-down methodologies that support their optimized performance from the early design phases, including accurate behavioral modeling of mixed-signal circuital blocks
- Exploration of reconfiguration strategies and programmability techniques at the architecture and circuit level for adaptive interface performance
- Exploration of calibration techniques and architectures
- Optimum chip implementation and verification

The areas of application include wireline, wireless and optoelectronic communications, sensor interfaces, and medical electronics.

Expertise is supported by a long-term tradition (over 20 years) in the field of mixed-signal design, with special emphasis on sigma-delta, pipeline, ramp and SAR ADCs and several chips successfully transferred to industry. The accumulated know-how drives R&D, cooperation, and dissemination activities with both academia and world-leader industrial partners.

RESEARCH HIGHLIGHTS

J. Ruiz-Amaya, M. Delgado-Restituto, and A. Rodríguez-Vázquez, **Device-Level Modeling and Synthesis of High-Performance Pipeline ADCs**. ISBN: 978-1-4419-8845-4, Springer, 2011.

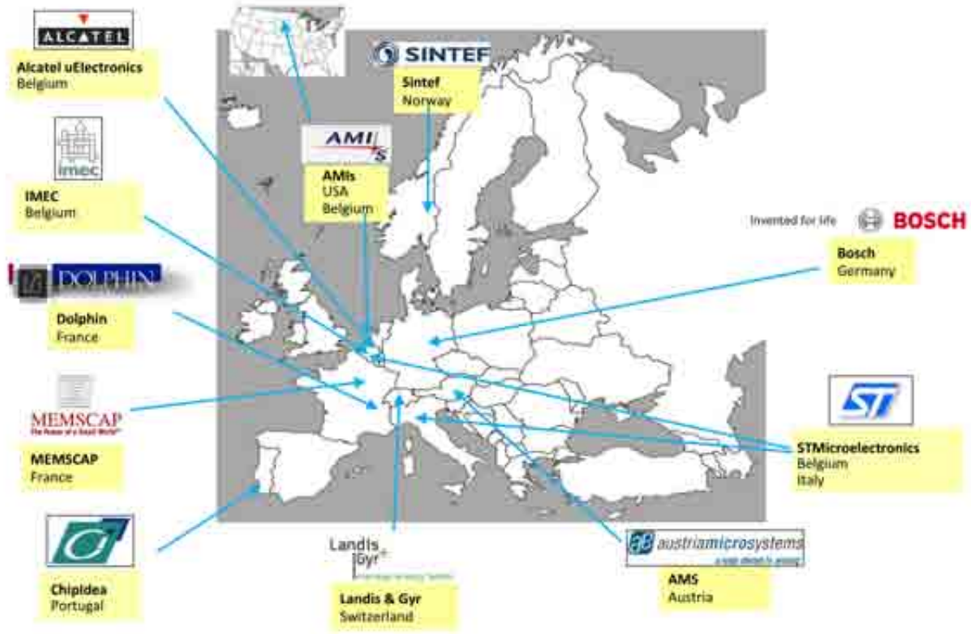
R. del Río, F. Medeiro, B. Pérez-Verdú, J.M. de la Rosa, A. Rodríguez-Vázquez, **CMOS Cascade Sigma-Delta Modulators for Sensors and Telecom: Error Analysis and Practical Design**. ISBN: 978-1- 4020-4775-6, Springer, 2006.

J. Ruiz-Amaya, J.M. de la Rosa, F.V. Fernández, F. Medeiro, R. del Río, B. Pérez-Verdú, A. Rodríguez-Vázquez, "**High-Level Synthesis of Switched-Capacitor, Switched-Current and Continuous-Time ΣΔ Modulators Using SIMULINK-Based Time-Domain Behavioral Models**". *IEEE Transactions on Circuits and Systems—I, Vol. 52, (9), pp. 1795-1810, Sept. 2005. (doi: 10.1109/TCSI.2005.852479)*

A. Rodríguez-Vázquez, F. Medeiro and E. Janssens (Eds.), **CMOS Telecom Data Converters**. ISBN 978-1-4020-7546-9, Springer, 2003.

Transference of a high-performance sigma-delta converter designed by our research group to Alcatel Microelectronics and ST-Microelectronics for its incorporation into the ADSL2+ modem chipset ST20190 Utopia for CPE applications (massive production in 2004).

Industrial partners of R&D activities in the field of analog-to-digital interfaces.



KEY PROJECTS & CONTRACTS

Design of Up-Stream and Down-Stream Data Converter for New Generation ADSL6

F Alcatel Microelectronics
(European private funding)
D 2001 - 2003
P Ángel Rodríguez Vázquez

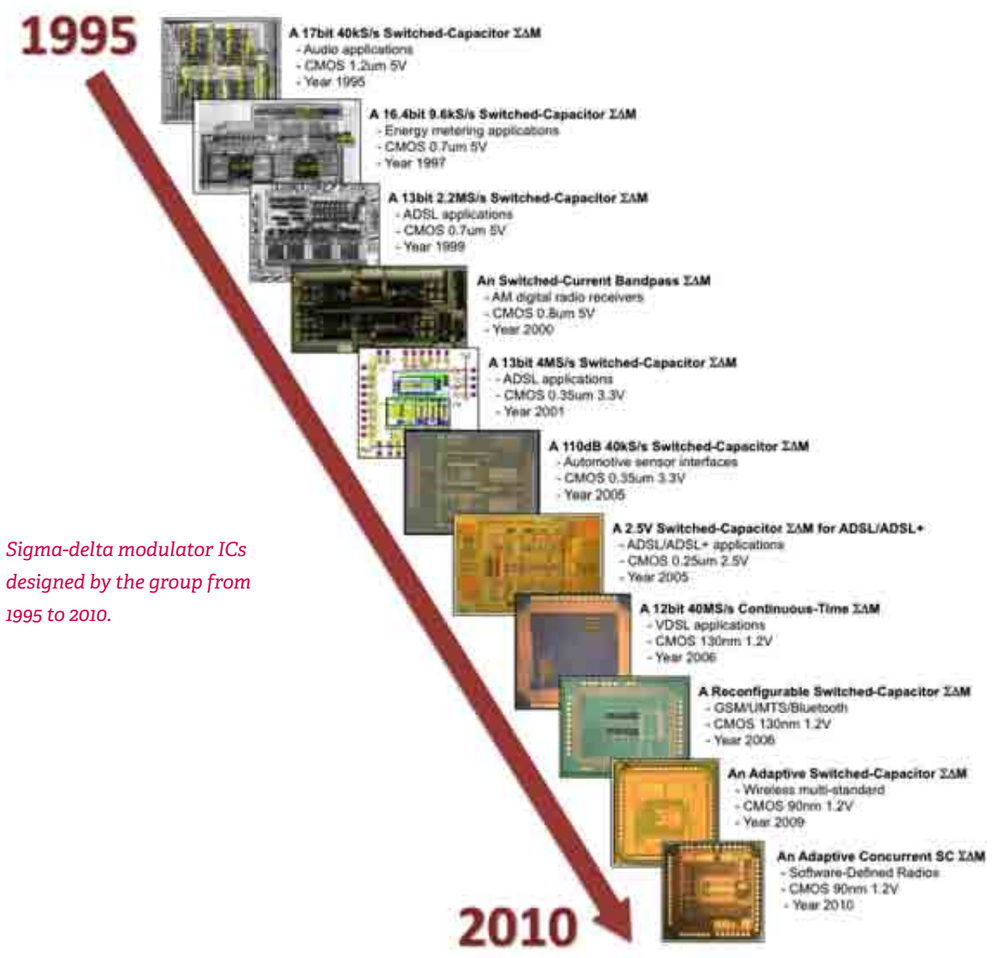
TAMES-2: Testability of Analog Macrocells Embedded into System-on-Chip (IST 2001-34283)

F European Union
(European public funding)
D 2002 - 2004
P Belén Pérez Verdu

SPIRIT: Secured Platform for Intelligent and Reconfigurable Voice and Data Terminals (MEDEA+ 2A101)

F MEDEA+
(European public funding)
D 2006 - 2009
P Manuel Delgado Restituto

F Funded by D Duration P Project leader



Sigma-delta modulator ICs designed by the group from 1995 to 2010.

WIRELESS IMPLANTABLE AND WEARABLE INTELLIGENT BIOSENSOR DEVICES

KEYWORDS

Biomedical circuits and systems
Neuro-engineering
Low-noise sensor readout
Low-power wireless interfaces
Telemetry systems
Energy harvesting

CONTACT

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Research on bioengineering including integrated sensing/read-out circuitry for the detection and recording of neural signals, wearable electronic devices for healthcare monitoring, and efficient wireless interfaces for intelligent medical devices (IMD). The common denominator to these research lines is the need to achieve high precision, low-noise analog read-out and very low power dissipation, in order to enable solutions which can be powered through small-capacity batteries and/or harvesting techniques.

Different activities are being developed in this area:

» Definition of enabling technologies for the integration and miniaturization of biomimetic systems, which can be used for building neurocortical implants suitable for scientific (to allow new advances in neuroscience), clinical (to provide neuroprosthesis for the treatment of neurological diseases), and translational application (to pave the way for brain-machine interfaces) issues.

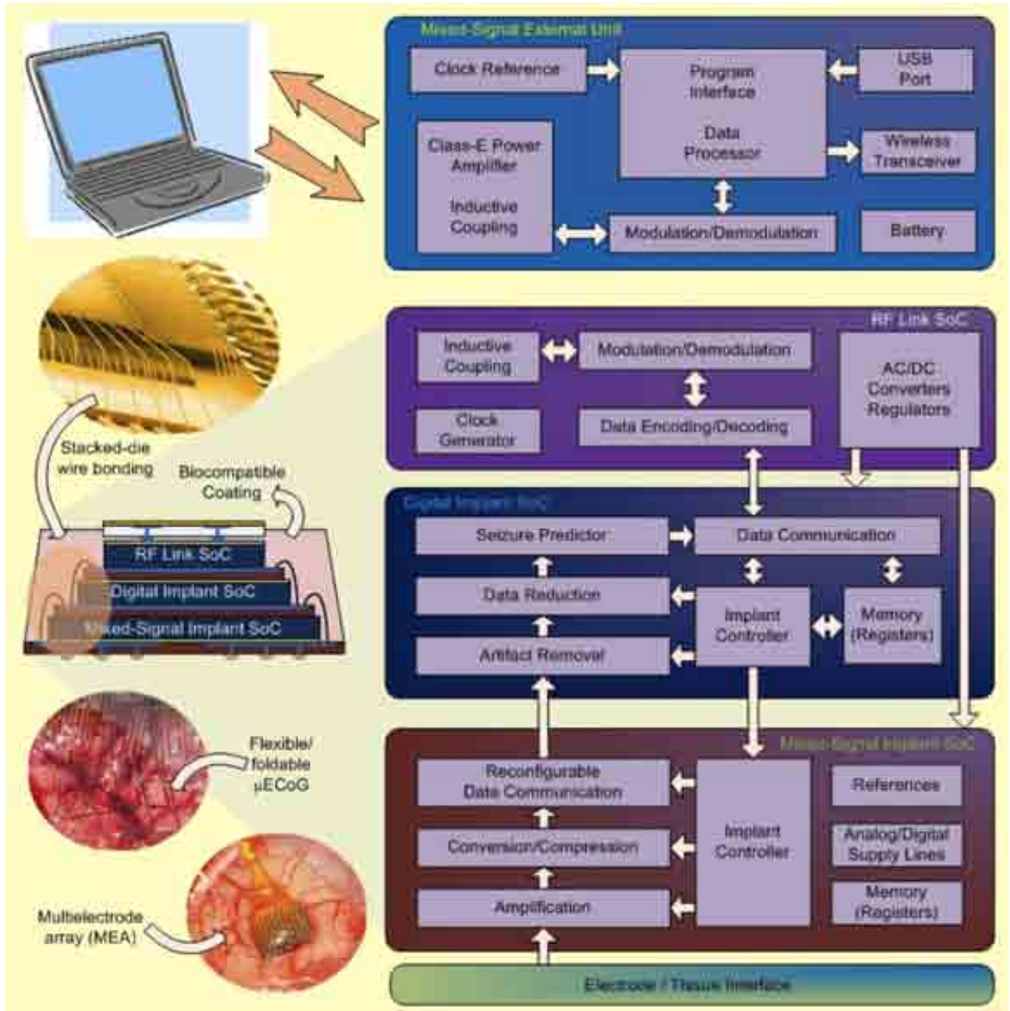
» Development of novel neurological data processing algorithms, including data compression, artifact suppression and seizure prediction processors, suitable for closed-loop therapeutic systems for refractory epilepsy and movement disorder diseases.

» Implementation of wireless sensor nodes (WSN) to quantify the impairments of the neuromuscular function and movement observed in Parkinson disease patients including means of surface electromyography (EMG) or kinematic measurements.

» Fabrication of passive radio-frequency identification (RFID) biomedical sensor tags, including mechanisms for remotely powering, suitable for the acquisition and conditioning of biomedical signals such as body temperature, blood glucose level or ECG information.

» Design of standard-compliant transceivers for wireless body area network (WBAN) applications, including novel architectures and circuit techniques for phase domain modulation.

More details can be found in http://www2.imse-cnm.csic.es/~mandel/.



Fully implantable multichannel cortical implant for seizure prediction based on heterogeneous integration and 3D stacking.

KEY PROJECTS & CONTRACTS

BIO-TAG: Monolithic Implementation of Passive RFID Transponders for Biomedical Applications

F Junta de Andalucía TIC-02818 (regional public funding)
D 7/12/2007 - 6/12/2011
P M. Delgado-Restituto

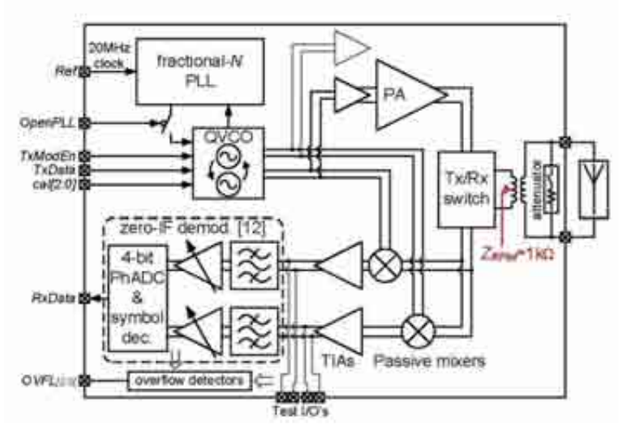
POWDERS: Ultra-Low Power Wireless Motes for the Remote Sensing of Biomedical Signals

F MICINN TEC2009-08447 (national public funding)
D 1/1/2010 - 31/12/2012
P M. Delgado-Restituto

CLEPSYDRA: Towards a Closed-Loop Epileptogenic Prediction System based on sub-Dural Recording Arrays

F MICINN TEC2012-33634 (national public funding)
D 1/1/2013 - 31/12/2015
P M. Delgado-Restituto

F Funded by D Duration P Project leader



Schematic diagram of the fabricated ultra-low power transceiver for Bluetooth Low Energy (BLE).

RESEARCH HIGHLIGHTS

J. A. Rodríguez-Rodríguez, J. Masuch, A. Rodríguez-Pérez, M. Delgado-Restituto, E. Alarcón, Á. Rodríguez-Vázquez, **"An Ultra Low-Power Mixed-Signal Back-end for Passive Sensor UHF RFID Transponders,"** *IEEE Transactions on Industrial Electronics, Vol. 59, pp. 1310 – 1322, Feb. 2012.*

A. Rodríguez-Pérez, J. Ruiz-Amaya, M. Delgado-Restituto, F. Medeiro, **"A Low-Power Programmable Neural Spike Detection Channel with Embedded Calibration and Data Compression."** *IEEE Transactions on Biomedical Circuits and Systems, Vol. 6, No. 2, pp. 87 – 100, April 2012.*

J. Masuch, M. Delgado-Restituto, **"A 190-µW zero-IF GFSK Demodulator with a 4-bit Phase-Domain ADC."** *IEEE Journal of Solid-State Circuits, Vol. 47, No. 11, pp. 2796 – 2806, November 2012.*

J. Masuch, M. Delgado-Restituto, **"A 1.1-mW-RX, -81.4 dBm Sensitivity CMOS Transceiver for Bluetooth Low Energy."** *IEEE Transactions on Microwave Theory and Techniques, Vol. 61, No. 4, pp. 1660 – 1673, April 2013.*

Jens Masuch, Manuel Delgado-Restituto, Dusan Milosevic and Peter Baltus, **"Co-Integration of an RF Energy Harvester Into a 2.4 GHz Transceiver."** *IEEE Journal of Solid-State Circuits, Vol. 48, No. 8, August 2013.*

CMOS SMART IMAGERS AND VISION CHIPS

KEYWORDS

Smart CMOS Imagers
HDR Imagers
Real-Time Vision Systems-on-Chip
Data Converters for Imagers
Silicon Retinas

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IMAGE HANDLING is instrumental in many applications, including consumer electronics, surveillance, robotics, machine vision, etc. Some of them demand high quality images, while others require fast analysis and interpretation of the image flow. Despite the specific target, all applications benefit from embedding processing circuitry together with optical sensors in the same silicon substrate.

CMOS technologies allow the incorporation of digital processing on-chip to correct image artifacts or to analyze and interpret the scene in real-time. Using CMOS technologies enables the implementation of cameras and vision systems with reduced power consumption and reduced size. This permits the incorporation of vision in applications where it was previously considered to be economically prohibitive or technically unfeasible.

This research line embraces different activities related to the incorporation of intelligence into image sensors, namely:

» New pixel topologies for enhanced sensitivity and reduced noise

» Front-side and Back-side illuminated sensors

» Pixels for single-photon detection and time-of-flight calculations

» Pixels for high-dynamic range image acquisition

» In-pixel processing and memory for feature extraction at the focal-plane

» Re-configurable read-out channels for high-performance digital imagers

» Data converters for high-speed and high accuracy (low noise) image downloading

» Architectures and algorithms for on-chip image correction

» Distributed, progressive processing architectures for vision systems

» Sensors for 3-D image capture

Different application areas are covered like automotive, unmanned vehicle navigation, distributed smart cameras and vision-enabled wireless sensor networks. These applications have been benchmarked by using real systems. Significant parts of the technology have been transferred to industry, including the creation of spin-off companies.

RESEARCH HIGHLIGHTS

J. Fernández-Berni, R. Carmona-Galán, Á. Rodríguez-Vázquez, Low-Power Smart Imagers for Vision-Enabled Sensor Networks, Springer, New York, May 2012. ISBN 978-1-4614-2391-1.

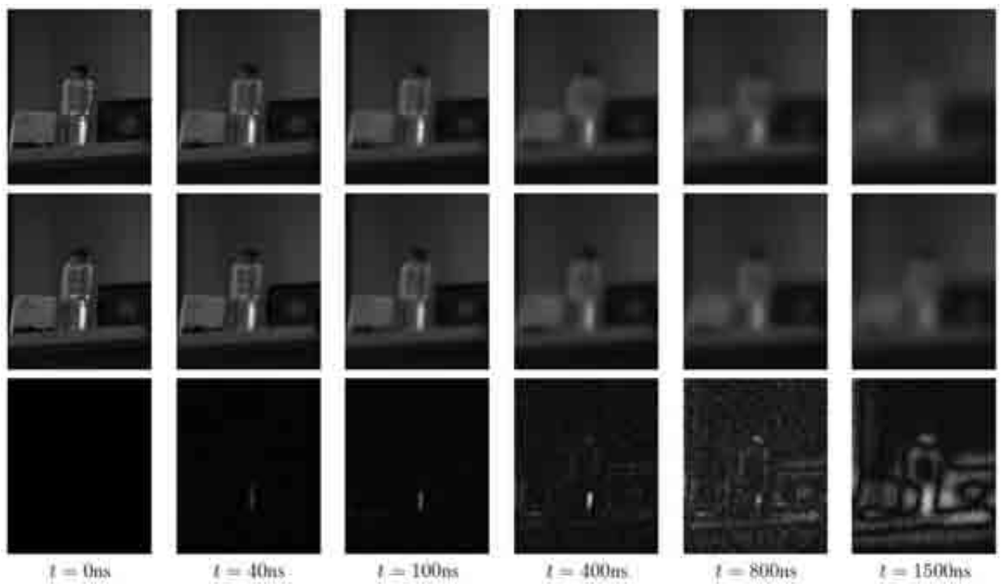
T. Roska and A. Rodríguez-Vázquez (Editors): Towards the Visual Microprocessor: VLSI Design and the Use of Cellular Neural Network Universal Machine Computers, pp. 213-237. John Wiley & Sons, Chichester, 2001. ISBN 0-471-95606-6.

J. Fernández-Berni, R. Carmona-Galán and L. Carranza González, **"FLIP-Q: A QCIF Resolution Focal-Plane Array for Low-Power Image Processing"**. *IEEE Journal of Solid-State Circuits, Vol. 46, No. 3, pp. 669-680, March 2011. ISSN: 0018-9200.*

G. Liñán, A. Rodríguez-Vázquez, R. Carmona, F. Jiménez, S. Espejo and R. Domínguez-Castro, **"A 1000FPS@128x128 Vision Processor with 8-bit Digitized I/O"**. *IEEE Journal of Solid-State Circuits , Vol. 39, No. 7, pp. 1044-1055, July 2004. ISSN: 0018-9200.*

A. Rodríguez-Vázquez, G. Liñán, L. Carranza, E. Roca, R. Carmona, F. Jiménez-Garrido, and R. Domínguez-Castro, **"ACE16k: the Third Generation of Mixed-Signal SIMD-CNN ACE Chips towards VSoCs"**. *IEEE Transactions on Circuit and Systems—I: Fundamental Theory and Applications , Vol. 51, No. 5, pp. 851-863, May 2004. ISSN 1057- 7122.*

On-chip generated scale-space (upper row) compared to ideal (middle row). Gaussian filters are implemented by time-controlled diffusion.



KEY PROJECTS & CONTRACTS

3DHVC: Design of high-performance heterogeneous, ultra high speed cellular sensor-processors for multispectral light sensing (BAA-11-001)

- F Office of Naval Research, USA (USA public funding)
- D 01/2011 - 12/2013
- P A. Rodríguez-Vázquez

WiVisNet: Wireless and smart vision sensors for networked surveillance and monitoring (TEC2009-11812)

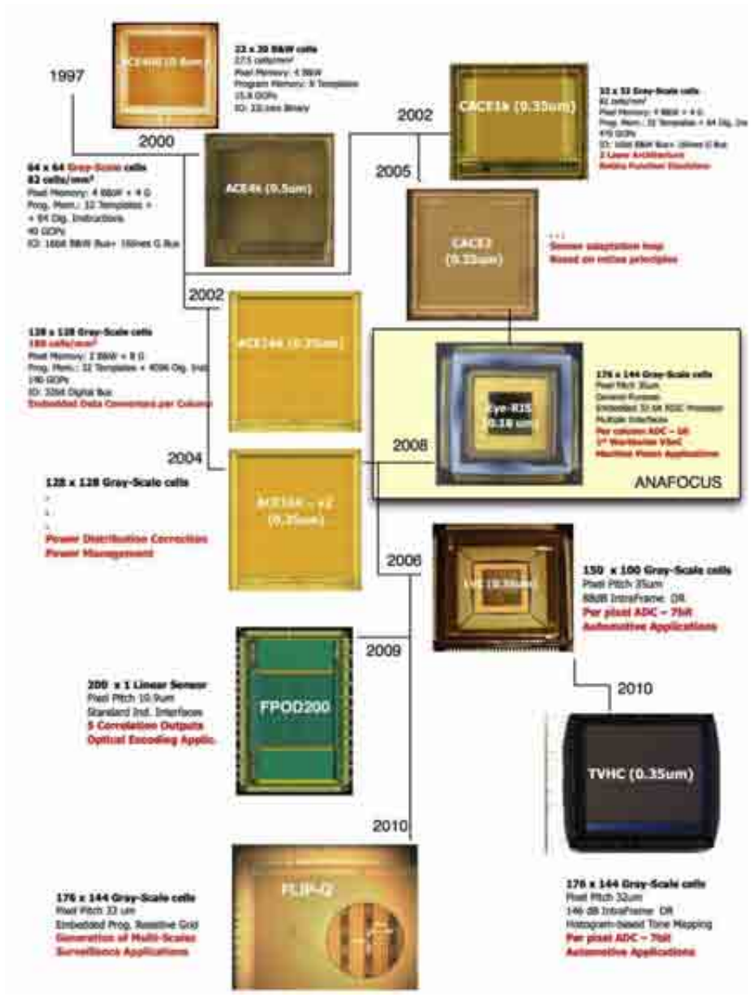
- F Ministry of Science and Innovation, Spain (national public funding)
- D 01/2010 - 12/2012
- P R. Carmona-Galán

VISTA: Design of sensing-processing-actuation systems on-a-chip: 4th generation vision systems

- F Ministry of Science and Technology, Spain (national public funding)
- D 12/2003 - 11/2006
- P A. Rodríguez- Vázquez

F Funded by D Duration P Project leader

Chronology of the vision chips designed by the group, from 1997 to 2010.



HETEROGENEOUS SENSORY-PROCESSING SYSTEMS AND 3-D INTEGRATION

KEYWORDS

3D Integrated Circuits
Sensory-Processing Microsystems
Through-Silicon-Vias
Vertically-Interconnected Systems
Heterogeneous Integration

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3D Integration technologies enable vertical interconnection of different wafers and thus the allocation of different subsystems and functions into dedicated, specialized layers. Both features have significant impact on performance. On the one hand, different technologies and materials can be combined, for instance nano-antennas for THz radiation detectors. On the other hand, form factors can be improved and larger function densities can be achieved; for instance, image pixels with embedded processing can be effectively implemented without penalizing the fill factor and the pixel pitch.

This research comprises different activities concerning heterogeneous sensory-processing systems using 3D IC with emphasis on technologies employing TSVs.

Activities include the following:

- Prospective analysis and identification of suitable 3D technology candidates
- Multi-spectral, 3D-compatible sensing materials and devices
- Interface circuitry between these sensors and the processing layers, including the electrical interface itself as well as the time multiplexing which may be required to handle different signal granularities at the different layers
- Architectures for optimum exploitation of the potentials of 3D heterogeneous technologies. Emphasis is on vision systems and the usage of different spatial resolutions and scales at each layer in the vertically-interconnected architecture
- Identification of constitutive functional operators for the different layers of the vertical processing chain, with emphasis on vision
- Circuit topologies for the different layers of the processing chain

Regarding vision systems, the basic challenge is to achieve sensors with million pixel counts, pixel pitch around 6 μm and operating speed in the range of 10,000 Frames/second.

RESEARCH HIGHLIGHTS

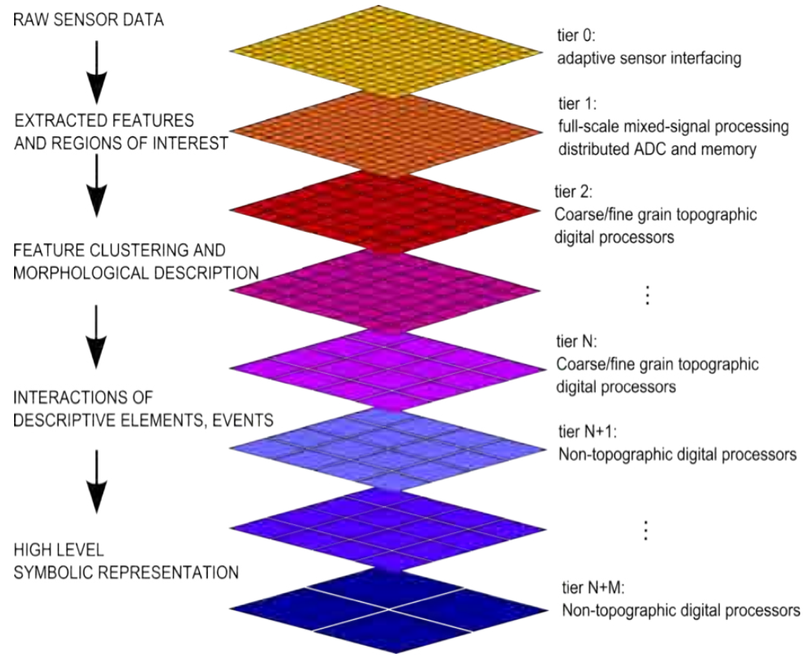
Á. Zarándy, Cs. Rekeczky, P. Földesy, R. Carmona-Galán, G. Liñán-Cembrano, G. Sós, Á. Rodríguez-Vázquez, T. Roska, **"VISCUBE: a multi-layer vision chip"**, *in Á. Zarandy (Editor): Focal-Plane Sensor-Processor Chips, pp. 181- 208. Springer, New York, 2011. ISBN 978-1-4419-6474-8.*

Á. Zarandy, P. Földesy, R. Carmona, Cs. Rekeczky, J. Bean, W. Porod, **"Cellular Multi-core Processor Carrier Chip for Nanoantenna Integration and Experiments"**, *in Ch. Baatar, W. Porod and T. Roska (Editors): Cellular Nanoscale Sensory Wave Computing, pp-147-168. Springer, New York, 2010. ISBN 978-1-4419-1010-3.*

R. Carmona-Galán, Á. Zarándy, Cs. Rekeczky, P. Földesy, A. Rodríguez-Pérez, C. Domínguez-Matas, J. Fernández-Berni, G. Liñán-Cembrano, B. Pérez-Verdú, Z. Kárász, M. Suárez-Cambre, V. M. Brea-Sánchez, T. Roska and Á. Rodríguez-Vázquez, **"A hierarchical vision processing architecture oriented to 3D integration of smart camera chips"**. *Journal of Systems Architecture, Vol. 59, no. 10, part A, pp. 908-919, 2013. (DOI: 10.1016/j.sysarc.2013.03.002) ISSN: 1383-7621.*

M. Suárez, V. M. Brea, J. Fernández-Berni, R. Carmona-Galán, G. Liñán, D. Cabello and Á. Rodríguez-Vázquez, **"CMOS-3D Smart Imager Architectures for Feature Detection"**. *IEEE Journal on Emerging and Selected Topics in Circuits and Systems, Vol. 2, No. 4, pp. 723-736, Dec. 2012. (DOI: 10.1109/JETCAS.2012.2223552) ISSN: 2156- 3357.*

R. Maldonado-Lopez, F. Vidal-Verdu, G. Linan, A. Rodriguez-Vazquez, **"Integrated Circuitry to Detect Slippage Inspired by Human Skin and Artificial Retinas,"** *IEEE Transactions on Circuits and Systems I: Regular Papers, Vol. 56, No. 8, pp. 1554-1565, Aug. 2009.*



Functional/physical mapping in a multilayer structure.

KEY PROJECTS & CONTRACTS

Sensores Inteligentes en Tecnologías CMOS-3D de Chips Apilados (IPT-2011-1625-430000)

F Ministerio de Ciencia e Innovación OPN-INNPACTO (national public funding)
D 05/2011 - 12/2014
P A. Rodríguez-Vázquez

3DHVC: Design of high-performance heterogeneous, ultra high speed cellular sensor-processors for multispectral light sensing (BAA-11-001)

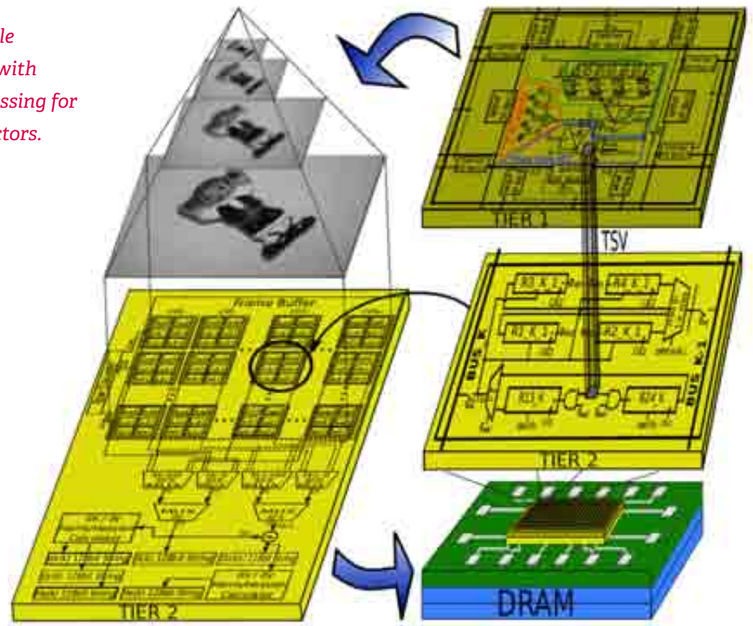
F Office of Naval Research, USA (USA public funding)
D 01/2011 - 12/2013
P A. Rodríguez-Vázquez

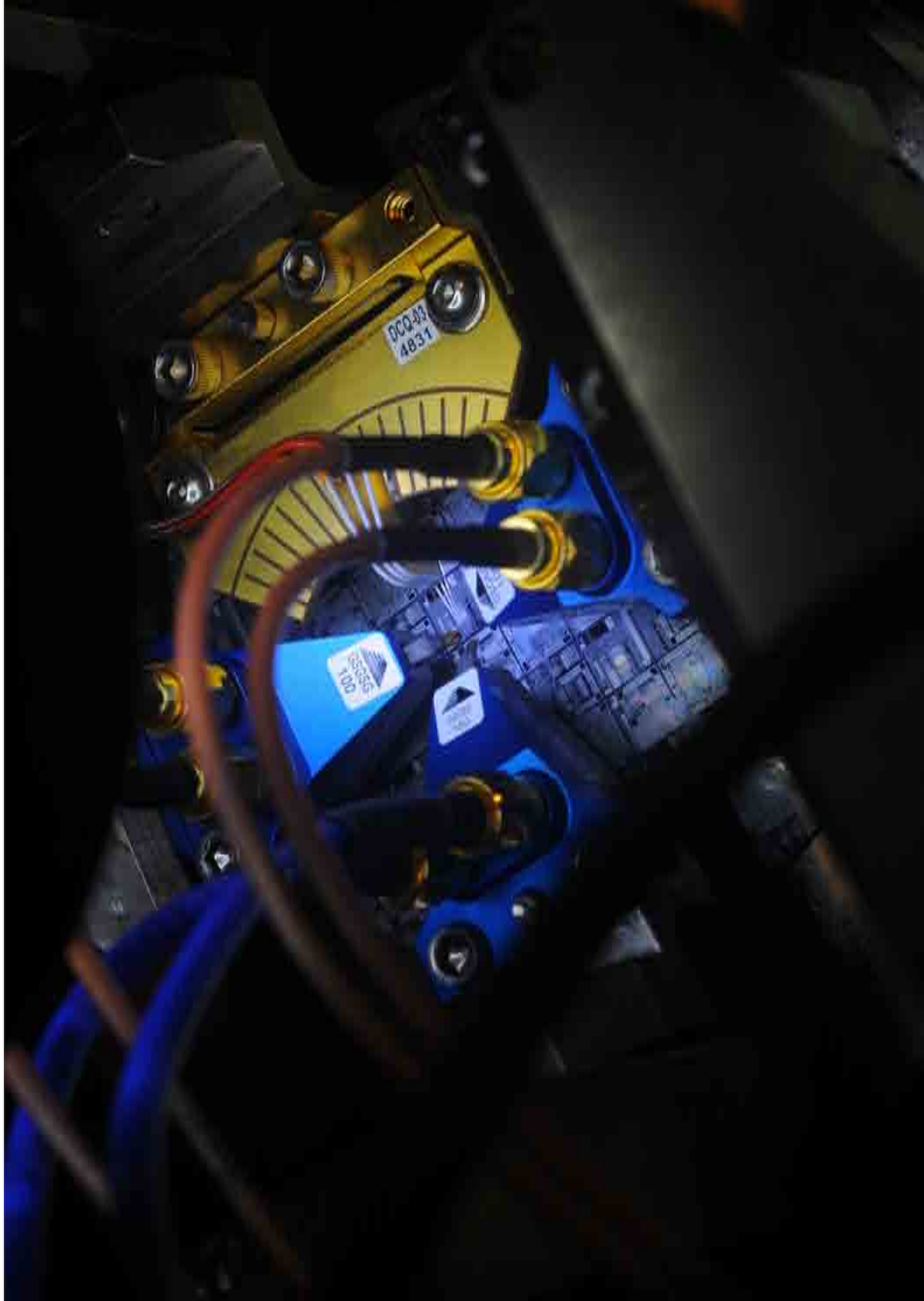
Study and design of interfaces for CMOS-compatible sensing nanostructures for the integration of nanoelectronic systems

F Ministry of Education and Science (national public funding)
D 10/2006 - 09/2007
P R. Carmona-Galán

F Funded by D Duration P Project leader

A CMOS-3D Reconfigurable Architecture with In-pixel processing for Feature Detectors.





Research Unit of

DESIGN OF DIGITAL AND MIXED-SIGNAL INTEGRATED CIRCUITS

RESEARCH LINES

56 CMOS Digital Integrated Circuits

58 Digital Embedded Systems

60 Microelectronic Systems for Computational Intelligence

62 Microelectronics for Security

PEOPLE

1. Antonio José Acosta Jiménez, PhD
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3. María del Rosario Arjona López
4. Ángel Barriga Barros, PhD
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11. Erica Tena Sánchez
12. Elisa Calvo Gallego
13. Susana Eiroa Lorenzo
14. Piedad Brox Jiménez, PhD
15. Miguel Ángel Prada Delgado
16. Manuel Valencia Barrero, PhD
17. José Miguel Mora Gutiérrez
18. María del Carmen Baena Oliva, PhD
19. Iluminada Baturone Castillo, PhD
20. Laurentiu Acasandrei

Not in the photo:
Javier Castro Ramírez, PhD
Gashaw Sassaw Teshome, PhD

CMOS DIGITAL INTEGRATED CIRCUITS

KEYWORDS

High-performance digital design
ASICs, Timing problems
Low-power and low-noise techniques
Design of digital cells

CONTACT

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This research topic has as main aim the efficient implementation of digital integrated circuits on ASICs at several abstraction levels: at a transistor level, designing basic digital cells with a full-custom methodology; at a gate level, finding optimum solutions for combinational and sequential circuits; at a circuit level, developing architectures and timing strategies. Transversal optimization mechanisms are employed in all these implementations, such as for instance, switching activity analysis, minimization of power consumption, low switching-noise generation, design of cells with data-independent power consumption, design for high-speed applications, etc.

Work in this topic faces:

- Design of digital ASICS in nanometer technologies
- Design of digital cells optimized for several parameters (i.e., dynamic power consumption, leakage, speed, area, noise, ...)
- Timing problems in digital circuits: metastability, design of arbiters and synchronizers, generation and distribution of clock signal in synchronous circuits, design of asynchronous circuits, etc.
- Combined techniques for power and noise reduction in digital circuits.

Main results achieved include:

- Design of digital ASICs following full-custom and semi-custom methodologies, in different technologies, including nanometric ones.
- Development of an automatic and systematic methodology for testing ASICs in the laboratory.
- Design of robust cells and circuits against timing failures.
- Design of differential circuits with power consumption independent on data, with immediate application in secure hardware against DPA attacks.
- Development of different combined noise-power (dynamic and leakage) reduction techniques.

(left page) Test board and ASIC incorporating a double-memory programmable and configurable PWAG controller.

RESEARCH HIGHLIGHTS

A. J. Acosta, I. Baturone, J. Castro, C. J. Jiménez, P. Brox, M. C. Martínez, **"Método para generar funciones multivariables afines a tramos con computación on-line del árbol de búsqueda y dispositivo para implementación del método"**, *Spanish Patent Application P201200608, 2012.*

P. Brox, J. Castro, M. C. Martínez, E. Tena, C. J. Jiménez, I. Baturone, A. J. Acosta: **"A Programmable and Configurable ASIC to Generate Piece-wise-Affine Functions Defined Over General Partitions"**, *Aceptado en IEEE Trans. on Circuits and Systems-Part I. 2013. DOI: 10.1109/TCSI.2013.2265962*

M. Valencia, M. J. Bellido, J. L. Huertas, A. J. Acosta, S. Sánchez-Solano: **"Modular Asynchronous Arbiter Insensitive to Metastability"**, *IEEE Transactions on Computers, Vol. 44, No. 12, pp. 1456-1461, December 1995. DOI: 10.1109/12.477251*

A. J. Acosta, M. Valencia, Á. Barriga, M. J. Bellido, J. L. Huertas: **"SODS: A New CMOS Differential-type Structure"**, *IEEE Journal of Solid- State Circuits, Vol. 30, No. 7, pp. 835-838, July 1995. DOI: 10.1109/4.391127*

P. Parra, A. J. Acosta, M. Valencia: **"Selective Clock-Gating for Low- Power Synchronous Counters"**, *Journal of Low Power Electronics, Vol. 1, No. 1, pp. 11-19, April 2005. DOI: http://dx.doi.org/10.1166/jolpe.2005.003*

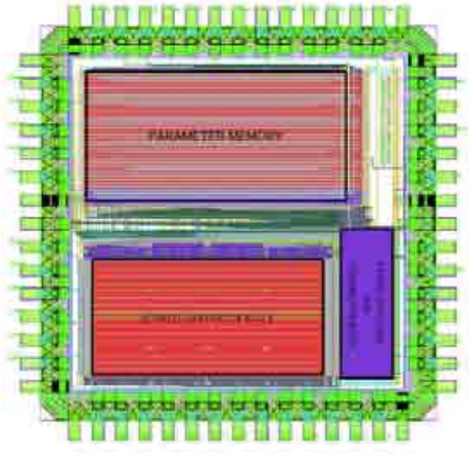
KEY PROJECTS & CONTRACTS

MOBY-DIC: Model-Based Synthesis of Digital Electronic Circuits for Embedded Control (EC-IST-VIIPM No-248858)
F Seventh Framework Programme (FP7), (European public funding)
D 01/12/2009 – 30/11/2012
P Dr. Antonio J. Acosta Jiménez

TICOCO: Integrated techniques for the management of supply current in nanometric digital and mixed-signal integrated circuits (TEC2007-65105/MIC)
F Ministry of Science and Innovation, (national public funding)
D 01/10/2007 – 31/12/2010
P Dr. Antonio J. Acosta Jiménez

Design of High-Performance Micro-Nanoelectronic Digital Systems (TIC2006-635)
F Junta de Andalucía (regional public funding)
D 01/04/2006 – 31/03/2009
P Dr. Ángel Barriga Barros

F Funded by D Duration P Project leader



Layout of a 4-input 2-output PWA controller designed in a 90nm technology.

DIGITAL EMBEDDED SYSTEMS

KEYWORDS

Embedded systems
Design methodologies
Systems on chip (SoC)
Hardware & software codesign
Reconfigurable devices
CAD tools

CONTACT

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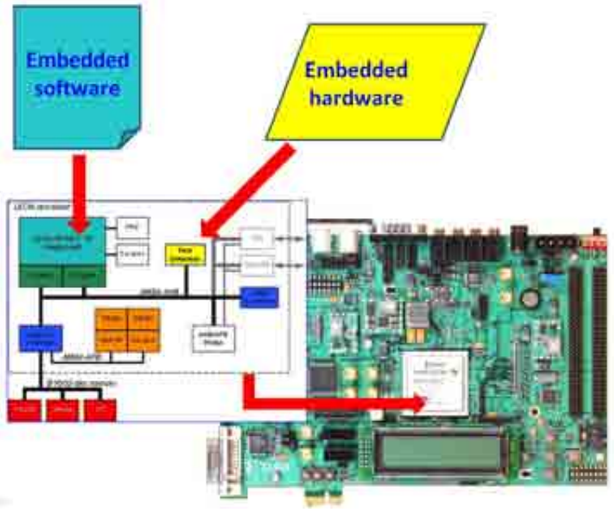
This research line is focused on the design of digital embedded systems implemented on programmable devices (FPGAs) and on application-specific integrated circuits (ASICs). The aim is to solve problems related to size constraints, power consumption and computation that characterize such systems, as well as to provide the tools and design methodologies that facilitate and accelerate its development.

The highlights of the developed solutions are the design of specific processing architectures, hardware/software codesign techniques, the use of reconfigurable devices, and the employment of Intellectual Property (IP) modules for reusability. The transversal nature of this research line allows that its results can be used in different application domains related to other research activities of the group.

The topics of interest that are covered by this research line are:

- Development of design methodologies for embedded digital systems
  - Specification languages
  - Hardware & software codesign
  - CAD tools development
- Architectures for specific application systems
  - Architectures and design of data/signal processing modules
  - Development of IP modules
  - Reconfigurable systems
- Applications of embedded digital systems
  - Biometric systems based on fingerprint, face recognition and voice identification
  - Embedded cryptographic systems
  - Image processing and artificial vision
  - Emerging applications of smart cards, communications networks, industrial control systems and wireless sensor networks



FPGA-based embedded system to implement Viola-Jones face detection algorithm.

RESEARCH HIGHLIGHTS

A. Cabrera, S. Sánchez-Solano, P. Brox, A. Barriga, R. Senhadji, **"Hardware/software codesign of configurable fuzzy control systems"**. *Applied Soft Computing, Vol. 4, No 3, pp. 271-285, Aug. 2004.*

A. Barriga, S. Sánchez-Solano, P. Brox, A. Cabrera, I. Baturone, **"Modelling and Implementation of Fuzzy Systems based on VHDL"**. *International Journal of Approximate Reasoning "Advances in Fuzzy Sets and Rough Sets", V. 41/ 2, pp. 164-178, Feb. 2006.*

A. Barriga, Carlos J. Jiménez, and Manuel Valencia, Logic Synthesis, Encyclopedia of Computer Science and Engineering, editor is Benjamin W. Wah; ISBN for the 5- Volume set is 978-0-471-38393-2; Arto. no 190; pp.1753-1762; John Wiley&Sons, Inc,January 2009.

L. Acasandrei, A. Barriga, **"Accelerating Viola-Jones Face Detection for Embedded and SoC Environments"**, *Fifth ACM/IEEE International Conference on Distributed Smart Cameras (ICDSC'2011), Ghent, Belgium, Aug. 2011.*

P. Brox, I. Baturone, S. Sánchez-Solano, **"Fuzzy logic-based embedded system for video de-interlacing"**. *Applied Soft Computing, vol. 14, part C, pp 338-346, 2014.*

FPGA-based embedded system for video de-interlacing: (a) Block diagram (b) Experimental setup.

b

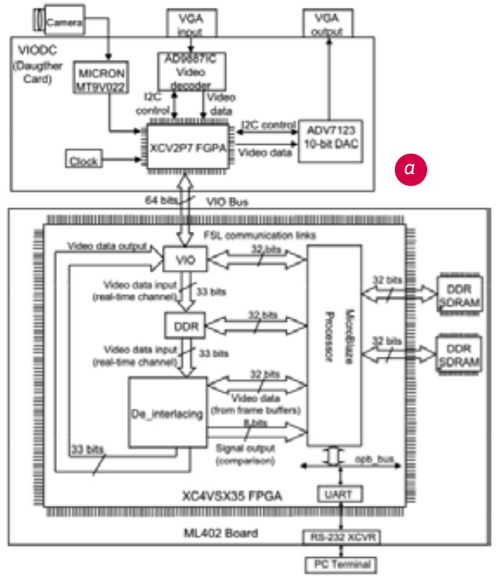
KEY PROJECTS & CONTRACTS

Microelectronic design of vision systems for smart sensor networks (TEC2008-04920)
F Ministry of Science and Innovation, (national public funding)
D 2009 – 2011
P Dr. Santiago Sánchez Solano

Model-based synthesis of digital electronic circuits for embedded control (EC-IST-VII-PM No-248858)
F Seventh Framework Programme (FP7), (European public funding)
D 01/12/2009 – 30/11/2012
P Dr. Antonio J. Acosta Jiménez

Hardware design for embedded systems in intelligent environments (TEC2011-24319)
F Ministry of Science and Innovation, (national public funding)
D 2012 – 2014
P Dr. Santiago Sánchez Solano

F Funded by D Duration P Project leader



a

MICROELECTRONIC SYSTEMS FOR COMPUTATIONAL INTELLIGENCE

KEYWORDS

Intelligent Systems
Soft-Computing
Neuro-Fuzzy Circuits
CAD Tools
Model-Based Design
Fuzzy Control & Image Processing
Intelligent Sensor Networks

CONTACT

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This research line focuses on the development of new design methodologies and circuit elements for Computational Intelligence applications. Computational Intelligence includes a set of techniques inspired by natural processes that allow addressing complex problems more efficiently than through traditional approaches.

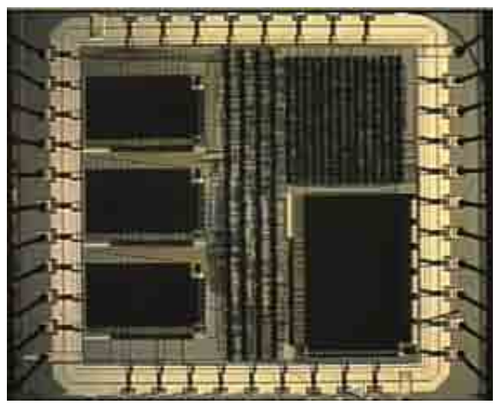
Specifically, our interest is mainly focused towards efficient hardware implementation of neuro-fuzzy systems and its use in applications that take advantage of their ability to describe a system with linguistic terms, as well as to cope with the inaccurate, vague or incomplete information that appears in many real-world problems.

In recent years, the developed activities in this line have addressed the following three main objectives:

1. The development of architectures for efficient implementation of fuzzy-inference systems on ASICs and FPGAs, as well as the proposal of a model-based design methodology that accelerates the stages of functional verification and synthesis of fuzzy modules and facilitates their integration in embedded systems.

2. The generation of a development environment for fuzzy systems, Xfuzzy, which facilitates the tasks of design, verification and synthesis, both software and hardware, of fuzzy logic-based systems.

3. The application of the above techniques and circuits to different problems of robotics, industrial control, food technology, communications systems, image processing, and intelligent sensor networks for applications related to the areas of safety and environmental control.



VLSI implementation of a 3-imput 1-output fuzzy inference system using an active rule-based architecture.

RESEARCH HIGHLIGHTS

I. Baturone, A. Barriga, S. Sánchez-Solano, C. J. Jiménez-Fernández, D.R. López, Microelectronic Design of Fuzzy Logic-Based Systems. CRC Press, March 2000.

P. Brox, I. Baturone, S. Sánchez-Solano, Fuzzy Logic-Based Algorithms for Video De-Interlacing. Series: Studies in Fuzziness and Soft Computing, Vol. 246, Springer, 2010.

F. Montesino Pouzols, D. R. Lopez, A. Barriga, Mining and Control of Network Traffic by Computational Intelligence. Series: Studies in Computational Intelligence, Vol. 342, Springer, 2011.

S. Sánchez-Solano, A. J. Cabrera, I. Baturone, F. J. Moreno-Velo, M. Brox, **"FPGA Implementation of Embedded Fuzzy Controllers for Robotic Applications"**. *IEEE Trans. on Industrial Electronics, Vol. 54, No 4, pp. 1937-1945, Aug. 2007.*

S. Sánchez-Solano, E. del Toro, M. Brox, P. Brox, I. Baturone, **"Model-Based Design Methodology for Rapid Development of Fuzzy Controllers on FPGAs"**. *IEEE Trans. on Industrial Informatics, 2012.*

More publications in: http://www.imse-cnm.csic.es/Xfuzzy/xfpapers.html

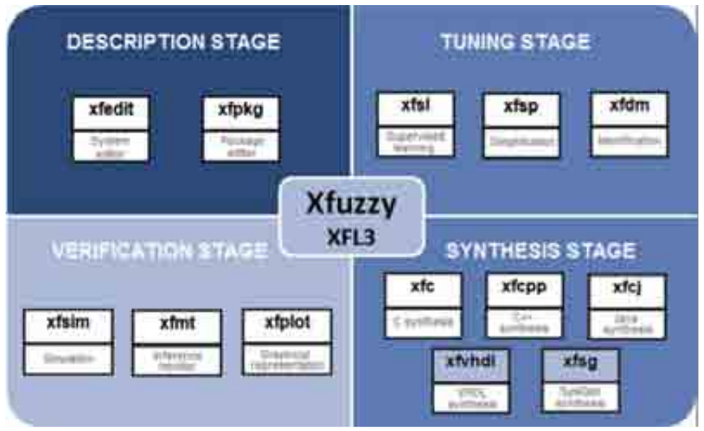
KEY PROJECTS & CONTRACTS

Microelectronic design of intelligent systems for sensory information processing (TIC2001-1726-C02-01)
F Spanish Government (national public funding)
D 2001 – 2004
P Dr. Santiago Sánchez Solano

Microelectronic implementation of fuzzy circuits for intelligent vision microsystems (TEC2005-04359/MIC)
F Ministry of Science and Education, (national public funding)
D 2006 – 2008
P Dr. Ángel Barriga Barros

Hardware design for embedded systems in intelligent environments (TEC2011-24319)
F Ministry of Science and Innovation, (national public funding)
D 2012 – 2014
P Dr. Santiago Sánchez Solano

F Funded by D Duration P Project leader



Components of the Xfuzzy environment, which integrates tools to facilitate the different stages involved in the design process of fuzzy logic-based systems.

MICROELECTRONICS FOR SECURITY

KEYWORDS

Hardware for cryptography
Biometry and crypto-biometry
Physical unclonable functions (PUFs)
Secure FPGAs and integrated circuits
Hardware attacks
Authentication and secure communications

CONTACT

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This research line focuses on microelectronic solutions for security applications. The objectives are to verify the identity of hardware devices and users as well as to store and communicate sensitive information, resorting to the use of techniques from cryptography, biometry, and their combination (crypto-biometry). Security against hardware attacks is especially analyzed, particularly side-channel attacks such as differential power analysis (DPA). Microelectronic solutions are aimed at constructions and algorithms providing security together with efficient features of size, power consumption and operation speed.

The activities within this research line are devoted to:

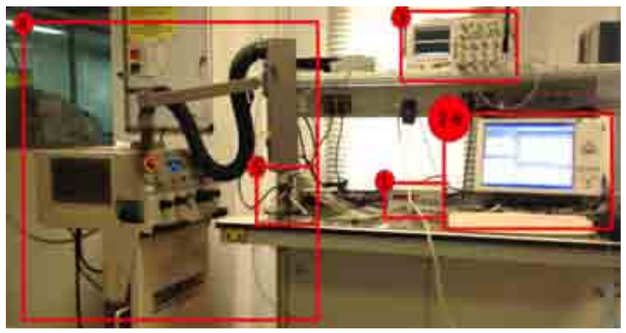
1. Exploration of cryptographic algorithms from a secure hardware implementation point of view. Development of architectures for such algorithms with optimized features in terms of VLSI design and resistance against attacks.

2. Analysis of side-channel attack sources. Development of experimental and simulation setups and benchmarks to measure the security of microelectronic realizations against attacks.

3. Design of modules based on PUFs (within programmable devices and/or integrated circuits) to implement security primitives particularly related to key generation, identifiers, and random numbers.

4. Hardware implementation of algorithms to process and recognize biometric features such as fingerprints, faces, gait, voice, etc. Design of microelectronic solutions for biometric, multi-biometric, and crypto-biometric systems.

5. Application of the above solutions to devices such as smart cards, tokens, tags, consumer electronic devices, control systems, etc.



Experimental setup to measure hardware security: (1) Power supply, (2) Logic analyzer, (3) Osciloscope, (4) Temperature control system, (5) Device under test, (6) Software to automate measurements.

RESEARCH HIGHLIGHTS

J. Castro, P. Parra, A. Acosta, **"An improved differential pull-down network logic configuration for DPA resistant circuits"**, *International Conference on Microelectronics, El Cairo, 2010, pp. 311-314. DOI: 10.1109/ICM.2010.5696147*

L. Acasandrei and A. Barriga-Barros, **"Accelerating Viola-Jones face detection for embedded and SoC environments,"** *in 5th ACM/IEEE Int. C. on Distributed Smart Cameras, Ghent, Belgium, 2011. DOI: 10.1109/ICDSC.2011.6042932*

S. Eiroa, J. Castro, M. C. Martínez-Rodríguez, E. Tena, P. Brox, I. Baturone, **"Reducing bit flipping problems in SRAM physical unclonable functions for chip identification"**, *Proc. 19th Int. Conf. on Electronics, Circuits and Systems, 2012. DOI: 10.1109/ICECS.2012.6463720*

R. Arjona, I. Baturone, **"A Hardware Solution for Real-Time Intelligent Fingerprint Acquisition"**, *Journal of Real-Time Image Processing, Nov. 2012. DOI: 10.1007/s11554-012-0286-1*

J. M. Mora-Gutiérrez, C.J. Jiménez-Fernández, M. Valencia-Barrero, **"Low Power Implementation of Trivium Stream Cipher"**, *LNCS 7606, pp. 113–120, 2013, Springer- Verlag Berlin Heidelberg 2013. DOI: 10.1007/978-3-642-36157-9_12*

More information available at: http://www.imse-cnm.csic.es/~cripto-bio/ and http://cb-doc.ximdex.com

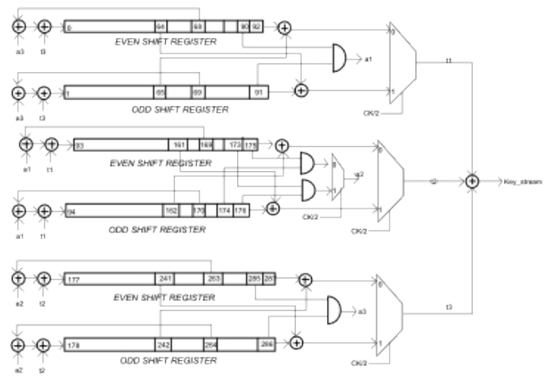
KEY PROJECTS & CONTRACTS

CRIPTO-BIO: Microelectronic design for crypto-biometric authentication (P08-TIC-03674)
F Junta de Andalucía - Proy. de Excelencia (regional public funding)
D 2009 - 2013
P Iluminada Baturone Castillo

CITIES: Integrated circuits for secure transmission of information (TEC2010-16870)
F Ministerio de Ciencia e Innovación (national public funding)
D 2011 - 2013
P Carlos Jesús Jiménez Fernández

CB-DOC: Content management system with secure hardware-based crypto-biometric authentication (IPT-2012-0695-390000)
F M. de Economía y Competitividad Proyecto INNPACTO (national public funding)
D 2012 - 2014
P Iluminada Baturone Castillo

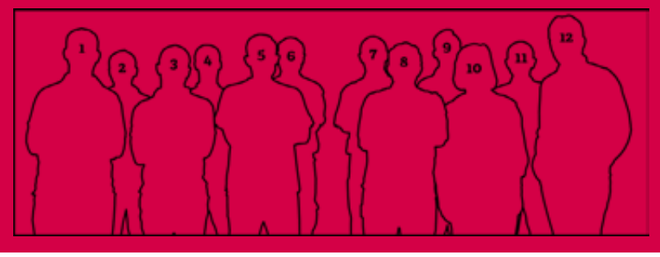
F Funded by D Duration P Project leader



Low-power implementation of Trivium stream cipher.

Research Unit of

MICRO/NANOMETRIC CIRCUITS AND SYSTEMS



RESEARCH LINES

66 Adaptive/Reconfigurable Nanometer CMOS Analog/RF ICs and Systems for Multi-Standard Wireless Transceivers and SDR

68 High-Efficiency Sigma-Delta Data Converters

70 Mixed-Signal Integrated Circuits for Space Applications

74 High Performance Acoustic Micro Electromechanical Systems (MEMS)

76 Design Technologies for Analog, Mixed-Signal, RF and Heterogeneous Circuits and Systems

PEOPLE

1. Manuel Muñoz Díaz
2. Luis Carranza González, PhD
3. Samuel Sordo Ibáñez
4. Antonio Toro Frías
5. Manuel Velasco Jiménez
6. Servando Espejo Meana, PhD
7. Francisco V. Fernández Fernández, PhD
8. Rafael Castro López, PhD
9. Alonso Morgado García de Polavieja, PhD
10. Elisenda Roca Moreno, PhD
11. José M. de la Rosa Utrera, PhD
12. Reinier González Echevarría

ADAPTIVE/RECONFIGURABLE NANOMETER CMOS ANALOG/RF ICS AND SYSTEMS FOR MULTI-STANDARD WIRELESS TRANSCEIVERS AND SDR

KEYWORDS

Flexible integrated circuits
RF-to-Digital Converters
Software Defined Radio
LNAs
Nanometer CMOS circuits
RF Passive devices

CONTACT

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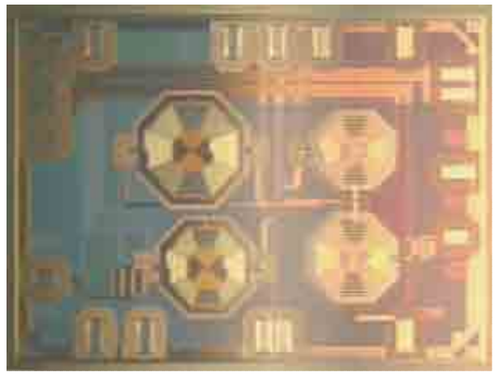
This research line focuses on the systematic design of adaptive, reconfigurable analog and RF CMOS integrated circuits and systems for multi-standard wireless transceivers and next-generation software-defined-radio based mobile terminals.

The main activities carried out in this research topics can be grouped into two main categories:

» Development of highly programmable analog front-end suitable for SDR receivers, based on an extensive use of digitally- assisted RF circuits, with minimized system complexity, maximization of shared building blocks, high robustness to circuit imperfections and reduced power consumption.

» Design, implementation and experimental characterization of reconfigurable analog/RF ICs using nanometer (65-45nm) CMOS technologies, capable of being continuously tunable and adaptable to a variable set of radio environment parameters, standard specifications, signal conditions and battery status.

The design activities are being supported and fueled by suitable design methodologies and CAD tools, specifically developed to systematize the synthesis and verification procedure and to optimize the performance of RF circuits and systems in terms of their target specifications with minimized power consumption. A good example is a SIMULINK block set specifically developed for the behavioral modeling and high-level simulation of RF receiver front-ends.



A 1-V 90-nm CMOS continuously-tuned 1.75-2.23GHz adaptive inductively-degenerated comon-source LNA.

RESEARCH HIGHLIGHTS

E.C. Becerra-Alvarez, F. Sandoval-Ibarra and J.M. de la Rosa: **"Flexible Nanometer CMOS Low-Noise Amplifiers for the Next-Generation Software-Defined-Radio Mobile Systems"**. *Chapter in Integrated Circuits for Analog Signal Processing (edited by E. Tielo-Cuautle), Springer, 2012.*

E.C. Becerra-Alvarez, F. Sandoval-Ibarra and J. M. de la Rosa: **"Design Considerations and Experimental Characterization Results of Continuously-Tuned Reconfigurable CMOS LNAs"**. *Proceeding of the 2011 IEEE International Symposium on Circuits and Systems (ISCAS), Río de Janeiro, Brazil, May 2011.*

J.M. Dores, E. Becerra-Alvarez, M.A. Martins, J.M. de la Rosa and J.R. Fernandes: **"A Comparative Study of Biasing Circuits for an Inductorless Wideband Low Noise Amplifier"**. *Proceeding of the 2011 IEEE Int. Midwest Symposium on Circuits and Systems (MWSCAS). Seoul, Korea, August 2011.*

J. Esteban-Muller, R. Gonzalez-Echevarría, C. Sánchez-López, R. Castro-López, E. Roca, F.V. Fernández, , J.M. López- Villegas, J. Sieiro and N. Vidal, **"Multi-objective optimization of planar inductors"**, *Proc. Int. Workshop on Symbolic and Numerical Methods, Modeling and Applications to Circuit Design, Gammarth (Tunisia), 2010, (ISBN: 978-1-4244-6815-7).*

José M. de la Rosa: **"Nanometer CMOS Wireless Transceivers – Application to the Next Generation of Software-Defined-Radio Mobile Terminals."** *Escuela Argentina-Uruguaya de Micro- Nanoelectrónica, Tecnología y Aplicaciones, October 2010.*

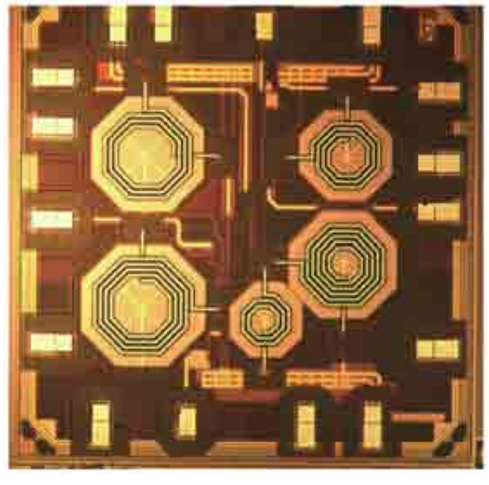
KEY PROJECTS & CONTRACTS

ARAMIS – Adaptive RF and Mixed-signal Integrated Systems for 4G Wireless Telecom (TEC2007-67247-C02- 00/MIC)
F C.I.C.Y.T. (national public funding)
D 10/2007 - 09/2010
P Prof. José Manuel de la Rosa Utrera

PLATFORM4G: Desarrollo de una Plataforma de Diseño de Sistemas Adaptables para Sistemas de Telecomunicación de Cuarta Generación
F Secretaría General de Universidades, Investigación y Tecnología, Junta de Andalucía (regional public funding)
D 12/2007 - 12/2010
P Prof. Francisco V. Fernández Fernández

FENIX-SDR: Flexible Nanometer CMOS Analog Integrated Circuits for the Next Generation of Software-Defined-Radio Mobile Terminals (TEC2010-14825/MIC)
F C.I.C.Y.T. (national public funding)
D 01/01/2011 - 31/12/2013
P Prof. José Manuel de la Rosa Utrera

F Funded by D Duration P Project leader



A 1-V 90-nm CMOS folded-cascode LNA for multi-standard wireless transceivers.

HIGH-EFFICIENCY SIGMA-DELTA DATA CONVERTERS

KEYWORDS

Oversampling converters
Switched-capacitor circuits
Switched-current circuits
Continuous-time circuits
Behavioral modeling and simulation
Nanometer CMOS circuits

CONTACT

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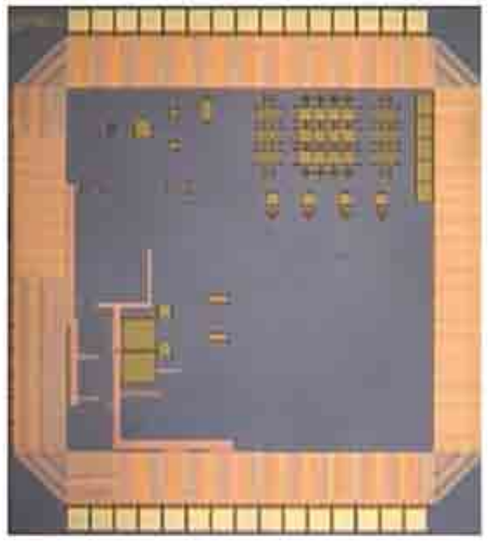
This research line deals with the analysis, modeling, design, implementation and experimental characterization of Sigma-Delta Modulators (SDMs) integrated in nanometer CMOS technologies. Different application scenarios are considered, spanning from sensor interfaces to broadband wireless communications. In these applications, a number of integrated circuits have been (or are being) developed, considering several circuit techniques, namely: discrete-time (switched-capacitor and switched-current), continuous-time (active-RC, Gm-C) and hybrid continuous- time/discrete-time circuits.

The research activities carried out in the last 5 years have been focused on the design of SDMs intented for next-generation mobile communications and software defined radio. In these topics, a number of state-of-the-art Integrated Circuits (IC) prototypes have been designed in cutting-edge nanometer CMOS technologies. The design of these ICs have been supported and fueled by diverse methodologies and CAD tools, specifically developed to systematize the synthesis and verification procedure and to optimize the performance in terms of target specifications with minimized power consumption.

An example of these CAD tools is SIMSIDES, a time- domain behavioral simulator for SDMs developed in the MATLAB/SIMULINK environment. Since the first version of SIMSIDES was developed in 2003, the tool has been continuously updated and improved with new models and facilities, and has been freely distributed (under confidential conditions described in a NDA agreement) to a number of universities, research institutes and companies all over the world.



A 130-nm CMOS 12-bit 40-MS/s 3-2 cascade continuous-time sigma-delta modulator.

RESEARCH HIGHLIGHTS

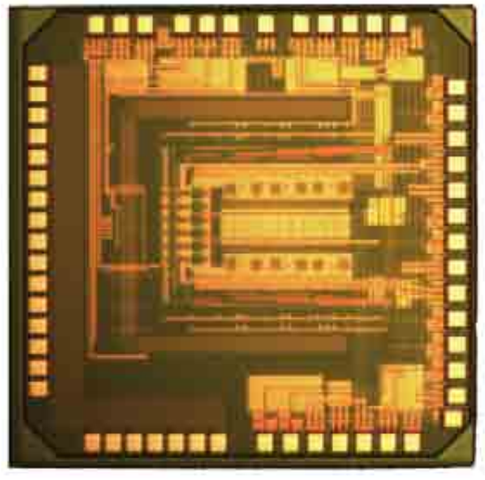
J.M. de la Rosa and R. del Río, CMOS Sigma-Delta Converters: Practical Design Guide, Wiley-IEEE Press, 2013.

J.M. de la Rosa: **"Sigma-Delta Modulators: Tutorial Overview, Design Guide and State-of-the-Art Survey."** *IEEE Trans. on Circuits and Systems - I: Regular Papers, vol. 58, pp. 1-21, January 2011.*

J.G. García-Sánchez and J.M. de la Rosa: **"Multirate Downsampling Hybrid CT/DT Cascade Sigma-Delta Modulators,"** *IEEE Trans. on Circuits and Systems-I: Regular Papers, vol. 59, pp. 285-294, February 2012.*

A. Morgado, R. del Río, J.M. de la Rosa, L. Bos, J. Ryckaert and G. V. Der Plas: **"A100kHz-10MHz BW, 78-to-52dB DR, 4.6- to-11mW Flexible SC Sigma-Delta Modulator in 1.2- V 90-nm CMOS."** *Proceeding of the 2010 IEEE ESSCIRC, Sevilla, September 2010.*

José M. de la Rosa: **"Overview of Sigma-Delta Modulators: Fundamentals, State-of-the-Art Survey and Practical Design Guide"**, *Advanced Topics in Microelectronic Engineering, Tyndall National Institute, Cork, Ireland (co-sponsored by the IEEE Solid-State Circuits Society, UK&RI Chapter), April 2013.*



A 90-nm CMOS power-scalable concurrent cascade 2-2-2 SC sigma-delta modulator for SDR.

KEY PROJECTS & CONTRACTS

ARAMIS – Adaptive RF and Mixed-signal Integrated Systems for 4G Wireless Telecom (TEC2007-67247-C02- 00/MIC)

F C.I.C.Y.T.
D October 2007 - September 2010
P Prof. José Manuel de la Rosa Utrera

PLATFORM4G: Desarrollo de una Plataforma de Diseño de Sistemas Adaptables para Sistemas de Telecomunicación de Cuarta Generación

F Secretaría General de Universidades, Investigación y Tecnología, Junta de Andalucía (regional public funding)
D 12/2007 - 12/2010
P Prof. Francisco V. Fernández Fernández

FENIX-SDR: Flexible Nanometer CMOS Analog Integrated Circuits for the Next Generation of Software-Defined-Radio Mobile Terminals (TEC2010-14825/MIC)

F C.I.C.Y.T.
D 01/01/2011 - 31/12/2013
P Prof. José Manuel de la Rosa Utrera

F Funded by D Duration P Project leader

MIXED-SIGNAL INTEGRATED CIRCUITS FOR SPACE APPLICATIONS

KEYWORDS

Radiation Hardness
Wide Temperature Ranges
Reliability
Total Integrated Dose
Single Event Effects
Redundancy
Latch-up Prevention

CONTACT

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This research line is oriented to the development of analog and mixed-signal integrated circuits and systems for space applications. Secondary application fields include those related with radiation environments, wide temperature ranges, and high reliability requirements. The focus is placed on standard CMOS technologies, following the radiation-hardening by design (RHBD) concept.

Specific activities include the characterization of the effects of high-energy electromagnetic radiation and high energy particles (Total Integrated Dose-TID and Single-Event Effects-SEE) on IC production technologies, devices, and circuits, and the development of robust circuits, systems, and design strategies. Other aspects of interest include circuit tolerance to wide temperature ranges, and structural resistance of the packaged systems to extreme thermal cycles, impacts, and vibration.

Ongoing and carried out works include the following:

» Characterization of a specific 0.35 µm CMOS technology for radiation effects and wide temperature range.

» Development of a digital cells-library for radiation tolerance.

» Development of equivalent simulation models of MOS transistors with specific layouts for radiation hardness.

» Design and test of a specific mixed-signal ASIC for diffuse-light optical communications within satellites.

» Design and test of a specific mixed signal ASIC for a three-axes magnetometer and accelerometer.

» Tests of packaging robustness under specific thermal cycles conditions

» Ongoing process of qualification of the two ASICs for space use.

KEY PROJECTS & CONTRACTS

Diseño y testado de ASICs para el espacio para la misión a Marte "MEIGA-METNET Precursor" (AYA2008-06420-C04-02/ESP)
F Ministerio de Ciencia e Innovación (national public funding)
D 01/01/2009 - 31/12/2009
P Servando Espejo Meana (US-IMSE)

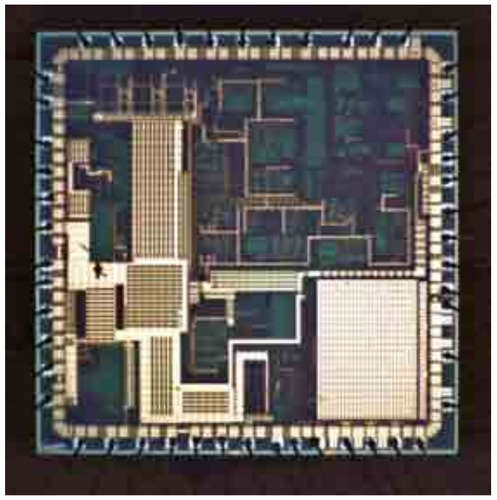
Diseño y testado de ASICs para el espacio para la misión a Marte "MEIGA-METNET Precursor" (AYA2009-14212-C05-04)
F Ministerio de Ciencia e Innovación (national public funding)
D 01/01/2010 - 31/12/2011
P Servando Espejo Meana (US-IMSE)

Diseño y testado de ASICs para el espacio para la misión a Marte "MEIGA-METNET Precursor" (AYA2011-29967-C05-05)
F Ministerio de Ciencia e Innovación (national public funding)
D 01/01/2012 - 31/12/2012
P Servando Espejo Meana (US-IMSE)

F Funded by D Duration P Project leader

RESEARCH HIGHLIGHTS

J. Ramos-Martos, A. Arias-Drake, A. Ragel-Morales, J. Ceballos-Cáceres, J. M. Mora-Gutiérrez, B. Piñero-García, M. Muñoz-Díaz, M. A. Lagos-Florido, S. Espejo-Meana, **"Radiation Characterization of the austriamicrosystems 0.35 µm CMOS Technology"**, *Conference on Radiation Effects on Components and Systems, RADECS 2011.*



OWLS asic layout.

Test setup for the OWLS asic.

HIGH PERFORMANCE ACOUSTIC MICRO ELECTROMECHANICAL SYSTEMS (MEMS)

KEYWORDS

MEMS sensors and actuators
Piezoelectric MEMS
Ultrasound imaging
Radiation and detection
Array beamforming
CMOS-MEMS integration

CONTACT

Jorge Mendoza

This research line focuses on the design, simulation and test of innovative MEMS devices, paying particular attention to the areas of acoustic MEMS transducers and integration with conventional CMOS electronics.

The activities carried out to date have focused on piezoelectric transducers, transducer array signal processing and ultrasound imaging sensor design. Near future research objectives include development of new ultrasonic pulse-echo beamforming signal processing techniques, experimental application to recently developed MEMS transducers and optimization of acoustic MEMS systems.

CMOS-MEMS integration constitutes an absolute need for experimentation and the link to other local experimental research lines and therefore is included as a necessary gateway for innovation.

The design and simulation activities carried out are supported by purpose-specific MEMS design software acquired at the Institute which includes finite element method (FEM) tools and electromechanical simulation capabilities thanks to the local computing cluster. Existing test facilities are being adapted to MEMS and experimental ultrasonic MEMS measurement tools are being pursued.

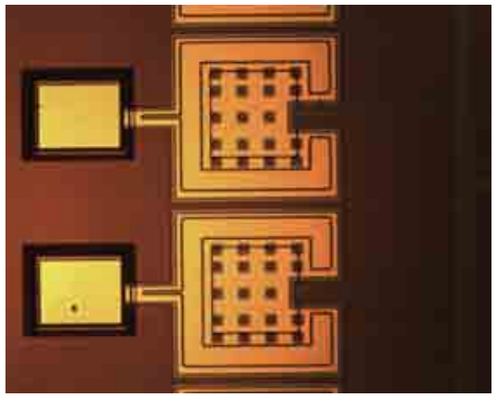
RESEARCH HIGHLIGHTS

J. Mendoza-López, S. Sánchez-Solano, J.L. Huertas-Díaz: **"Characterization and Modeling of Piezoelectric Integrated Micro Speakers for Audio Acoustic Actuation"**, *World Academy of Science, Engineering and Technology, v 58, pp183-189, 2011.*

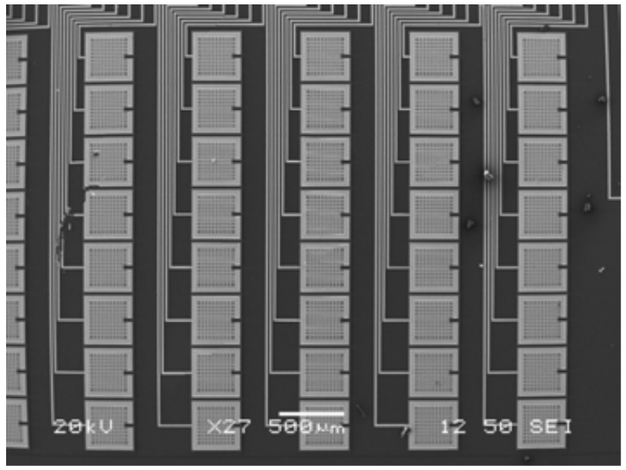
J. Mendoza-López, S. Sánchez-Solano, J.L. Huertas-Díaz: **" Characterization and Modeling of Circular Piezoelectric Micro Speakers for Audio Acoustic Actuation"**, *ISRN Mechanical Engineering, v2012, DOI: 10.5402/2012/635268.*

J. Mendoza-López, C. Sánchez-López, S. Sánchez-Solano, J.L. Huertas-Díaz: **" A noise shaping beamforming piezoelectric micros-peaker digital-to-acoustic array system"**, *submitted for publication to the IEEE Transactions on Audio Speech and Language Processing, Jan 2012.*

J. Mendoza-López: **"Micro membrane arrays for digital wave field reconstruction: towards the MEMS loudspeaker"**, *submitted testimonial by invitation to the EUROPRACTICE annual report, 2011.*



Optical microscope images of fabricated micro membrane arrays.



Custom micro membrane array SEM image inspired by CMUT etch- hole release design technique.

DESIGN TECHNOLOGIES FOR ANALOG, MIXED-SIGNAL, RF AND HETEROGENEOUS CIRCUITS AND SYSTEMS

KEYWORDS

Systematic Design Methodologies
Single-objective Optimization
Multi-objective Optimization
Reconfigurable design
Layout-aware design
Variability-aware design

CONTACT

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The general objective of this research line is to develop new systematic design methodologies for analog, mixed-signal, RF and heterogeneous integrated circuits and systems, aiming at higher performances, smaller cost and smaller power consumption.

More specifically, the work include activities in different aspects of the circuit design flow, as well as their application in industrial-class designs:

» Behavioral modeling and simulation methods supporting top- down specification transmission.

» Layout-aware synthesis methodologies for analog/RF circuits, showing the importance of the early inclusion of physical design effects in the design flow.

» Systematic reconfigurable circuit design for optimum use of area and power in multi-mode circuits and systems.

» Electromagnetic simulation-based performance modeling of passive devices, providing the best trade-offs among performances and cost for radiofrequency circuit design.

» Incorporation of time-zero and time-dependent variability effects in the design flow.

The research line also includes the investigation of new design paradigms, like bottom-up design methodologies, where complex systems are decomposed hierarchically and performance models from the lower blocks (known as Pareto-fronts) are used to build up the performance trade-offs of the upper blocks of the system. Specific aspects addressed are: generation of performance models, composition rules of performance models, multi-model generation, modeling of reconfiguration ability, incorporation of physical design and variability effects.

RESEARCH HIGHLIGHTS

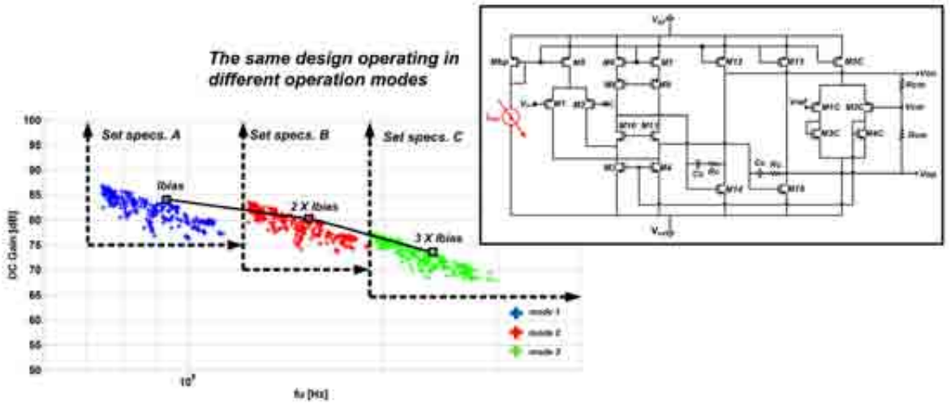
B. Liu, Q. Zhang, F. V. Fernández-Fernández, G. Gielen, **"An efficient evolutionary algorithm for chance-constrained bi-objective stochastic optimization and its application to manufacturing engineering"**, *IEEE Trans. on Evolutionary Computation, 2013. ISSN 1089-778X. DOI: 10.1109/TEVC.2013.2244898*

B. Liu, F. V. Fernández, G. Gielen, **"Efficient and accurate statistical analog yield optimization and variation-aware circuit sizing based on computational intelligence techniques"**, *IEEE Trans. on Computer-Aided Design, vol. 30/6, pp. 793-805, 2011.*

R. Castro-López, E. Roca, F. V. Fernández, **"Multi-mode Pareto fronts for the design of reconfigurable analog circuits"**, *IEE Electronic Letters, vol. 45(2), pp. 95-96, 2009.*

R. Castro-López, O. Guerra, E. Roca, F. V. Fernández, **"An Integrated Layout-Synthesis Approach for Analog ICs,"** *IEEE Trans. on Computer-Aided Design, vol. 27, no. 7, pp. 1179-1189, Jul. 2008.*

J. Ruiz-Amaya, J. M. de la Rosa-Utrera, F. V. Fernández-Fernández, F. M. Medeiro-Hidalgo, R. del Río-Fernández, M. B. Pérez-Verdú, Á. Rodríguez-Vázquez, **"High-Level Synthesis of Switched-Capacitor, Switched-Current and Continuous-Time SD Modulators Using SIMULINK-based Time-Domain Behavioral Models"**, *IEEE Trans. on Circuits and Systems, Part I.52 - 9, pp. 1795 - 1810, 2005.*



The concept of Multi-mode Pareto-optimal fronts for reconfigurable circuits.

KEY PROJECTS & CONTRACTS

RAPID: Retargetability for Reusability of Application-Driven Quadrature D/A Interface Block Design

F ESPRIT 29648
(European public funding)
D 1998 - 2001
P Ángel Rodríguez Vázquez

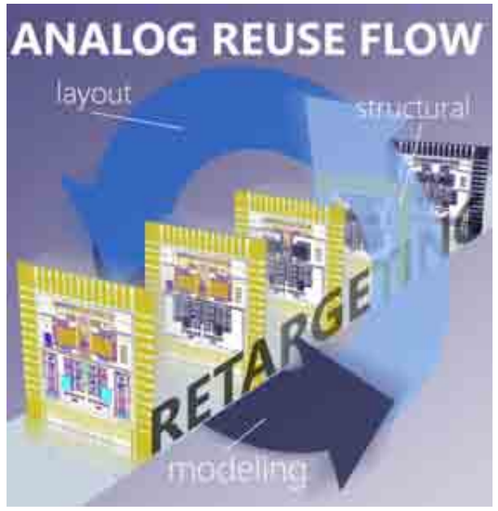
Entrefases Analógico-Digitales Reconfigurables para la Convergencia de Sistemas de Comunicaciones Inalámbricos y Alámbricos

F TEC2007-67247-C02-01
C.I.C.Y.T. (national public funding)
D 2004 - 2007
P Francisco V. Fernández

PLATFORM4G: Desarrollo de una Plataforma de Diseño de Sistemas Adaptables para Sistemas de Telecomunicaciones de Cuarta Generación

F TIC 2532 - Junta de Andalucía
(regional public funding)
D 2008 - 2011
P Francisco V. Fernández

F Funded by D Duration P Project leader



The concept of reuse in analog and mixed-signal circuits.

EDUCATION

PHD PROGRAM

Universities and Research Centres are instrumental agents for meeting the goals of the European Research Space. The role of such agents is defined at the document "The Role of the Universities in the Europe of Knowledge", released by the European Commission. According to this document, universities and research centres are entitled to:

- Educate scientists and technicians, particularly strengthening their skills for innovation and research.
- Promote and support the cooperation with industry through R&D project partnership and the transferring of technology and IP.
- Contribute to the leverage of the local and regional development, including "spin-offs" launching.

Among other instruments, doctorate programs are crucial to meeting these objectives and thus achieving convergence within the High Education European Space and the European Research Space.

The topic of Microelectronics embraces a large variety of scientific and technological disciplines with a very strong industrial profile and large impact on economy and society. Microelectronics is also the ultimate engine of Information Society and has hence a huge impact on many disciplines. As stated in the "Strategic Research Agenda of the European Technological Platform on Nano-Electronics", developments in micro- and nano-electronics are key for modern advanced societies. Particularly these technologies are the backbone of many industrial sectors where Europe has significant leadership, namely: telecommunications, energy, transportation and logistics, security/safety, health, etc. Advances made during the last few years in micro- and nano-electronics require the education of qualified human capital ready to confront the associated challenges are help maintaining and even increasing the European leadership. On the one hand, the Society needs qualified researchers capable of devising new knowledge and technology. On the other hand, specialized industries require qualified human resources for successful development of ever more sophisticated and complete products which can compete within worldwide markets.

The nano-electronics strategic agenda of the European Union highlights the strategic nature of deep sub-micron technologies and defines two basic edges for future advances, namely: i) "More-Moore", focused on the continued scaling down of main-stream VLSI digital technologies and logic circuits; ii) "More-than-Moore", focused on the enrichment of logic-based processors through the incorporation of diverse functions such as RF communications, sensing and actuation, energy harvesting/scavenging, etc: "More-than-Moore" includes also the technologies required for the effective and efficient implementation of these functions.

The Doctorate Program in Microelectronics offered by the University of Seville and implemented cooperatively by this University and the Spanish Council of Research, is conceived to meet professional and researchers in micro- and nano- electronics by simultaneously promoting values such as gender equality, lack of discrimination by class and race, and promotion of the human rights, among many others. The Program got the Excellence Label in 2011.

Students participating in the Program are entitled to devise a dissertation pushing the state-of-the-art and to produce prime line papers and IP products. Basic objectives of the program include:

- To reinforce students knowledge regarding the essences of the operation of microelectronic devices; for logic as well as for analog applications. Such comprehension should lay the foundations to confront R&D challenges following a critical and innovative approach.
- To understand the performance metric figures and the current state-of-the-art on the different topics addressed by the program. Students should develop skills to identifying research challenges and defining research endeavors on the basis of such understanding.
- To reinforce students knowledge regarding microelectronic design flows and methodologies, including all levels of microelectronic design; namely: system-level, function level, block level, circuit level and physical level.
- To learn reporting scientific results and to practice these skills through the reporting of research results at prime, peer-reviewed international journals.
- To develop advanced knowledge and/or methods on a selected research topic and to produce tangible results in the form of IP products, journal papers, research monographs and methodologies.
- To promote and reinforce teaming skills though the participation in coordinated projects.
- To get awareness of industry requirements and industrial project planning.
- To promote a culture relying on science-technology and innovation as the only of way of sustaining societal well-fare.

Our PhD Program includes the following research lines:

1. CMOS VLSI logic circuit design for "More-Moore"
2. "Beyond-CMOS" circuits and systems design
3. Bio-inspired and Bio-electronic circuits and systems
4. Heterogeneous circuits and systems and Microsystems
5. Analog, mixed-signal and RF circuit design

6. Microwave circuits and antennas
7. Microelectronic design flows
8. Soft computing circuits and systems
9. Test and design for test of microelectronic circuits and systems
10. Embedded microsystems

MASTER PROGRAM

The Master Program in Microelectronics, Design and Applications of Micro/Nanometric Systems (*http://www.imse-cnm.csic.es/master/*) is an official title offered by the Universidad de Sevilla. It is registered as No. 4312169 in the Spanish Catalogue of Universities, Centres and Degrees. It has been offered since 2007, accordingly to the RD1393/2007 normative.

The primary objective of this master is to train students to reach a high scientific and technical qualification in circuit and system design for modern submicron integrated circuits. The goal is to train students for conceiving, designing, verifying, fabricating, and testing integrated circuits and systems, with special emphasis on submicron technologies, and their integration in specific applications.

Training profiles include:

» CAD tools, methodologies and techniques for micro/nano IC design

» Technologies for micro/nano devices

» Design, integration, and test of analog, digital, mixed signal and radio frequency (RF) integrated circuits and systems

» Conception and evaluation techniques of integrated systems and their applications

» Project management in the semiconductor industry

The Master is intended for both students with research interests and workers employed in microelectronics-related companies willing to increase their knowledge and abilities. Participation modalities include fully virtual web-based e-learning, with the possibility of presence access to labs and facilities in Seville. In this sense, the Master can be considered as Blend-Learning.

The master is organized by personnel from the University of Seville and from the Instituto de Microelectrónica de Sevilla (IMSE). Over 30 professors and researchers are involved, whose research activities include: advanced analog, digital and RF circuit design, new paradigms for design with emergent devices, bio-inspired sensing and processing, integrated microsystems, telecommunication circuits and systems, antennas and microwave circuits, CAD tools and methodologies for micro/nanoelectronics, fuzzy and neuromorphic systems, design for test and testability, embedded system architectures on ASICs and FPGAs. Based on this experience, the students can face Doctorate Studies on Microelectrónica, University of Seville, in one of the following research areas:

» High performance CMOS VLSI digital design

» Circuits and systems design with post-CMOS nanoelectronic devices

» Bio-electronics systems

» Integrated and heterogeneous microsystems

» Design of analog integrated circuits and systems, mixed-signal and RF

» Antennas and microwaves circuits

» Techniques for systematic design of integrated circuits and systems

» Soft Computing based systems

» Test and design for testability of integrated circuits and systems

» Embedded Systems

The studies extent is 60 European ECTS Credits, equivalent to one academic year (~300 teaching hours, ~1500 student hours). The program includes several mandatory courses imparted during first semester:

» Micro/nanometric devices and technologies

» Design of analog, digital, mixed-signal and RF ICs

» Information processing techniques, systems, and applications CAD tools and methodologies

And three available specializations, with three 6 ECTCS courses each for the second semester:

» Circuits and systems for wireless communications
  - Wireless Transceivers: Standards, Techniques and Architectures
  - RF front-end circuit design
  - Electromagnetic foundations of RF design

» Circuits and systems for acquisition and processing of sensory signals
  - Sensors on Integrated Technologies
  - Bio-Inspired Processing: Algorithms and Circuits
  - Neuromorphic and Fuzzy Systems

» Advanced design and test techniques for nanometric circuits, devices, and emergent applications
  - Advanced design techniques
  - Test and design for test
  - Emerging technologies

If the three selected courses belong to different specializations, a so-called “Generic Specialization” is given. Optional External practices and stays in research centres are

also offered (6 ECTS). A Master Thesis (12 ECTS) is mandatory at the end of the Master.

The e-learning platform of the University of Seville (WebCT) is used for the on-line teaching. Embedded master classes, power-point and pdf materials, videos, virtual classes, virtual tutorials, self-evaluation mechanisms are the most usual on-line teaching activities. Presencial classes are intended for more practical and experimental aspects. All the materials are available in Spanish and English.

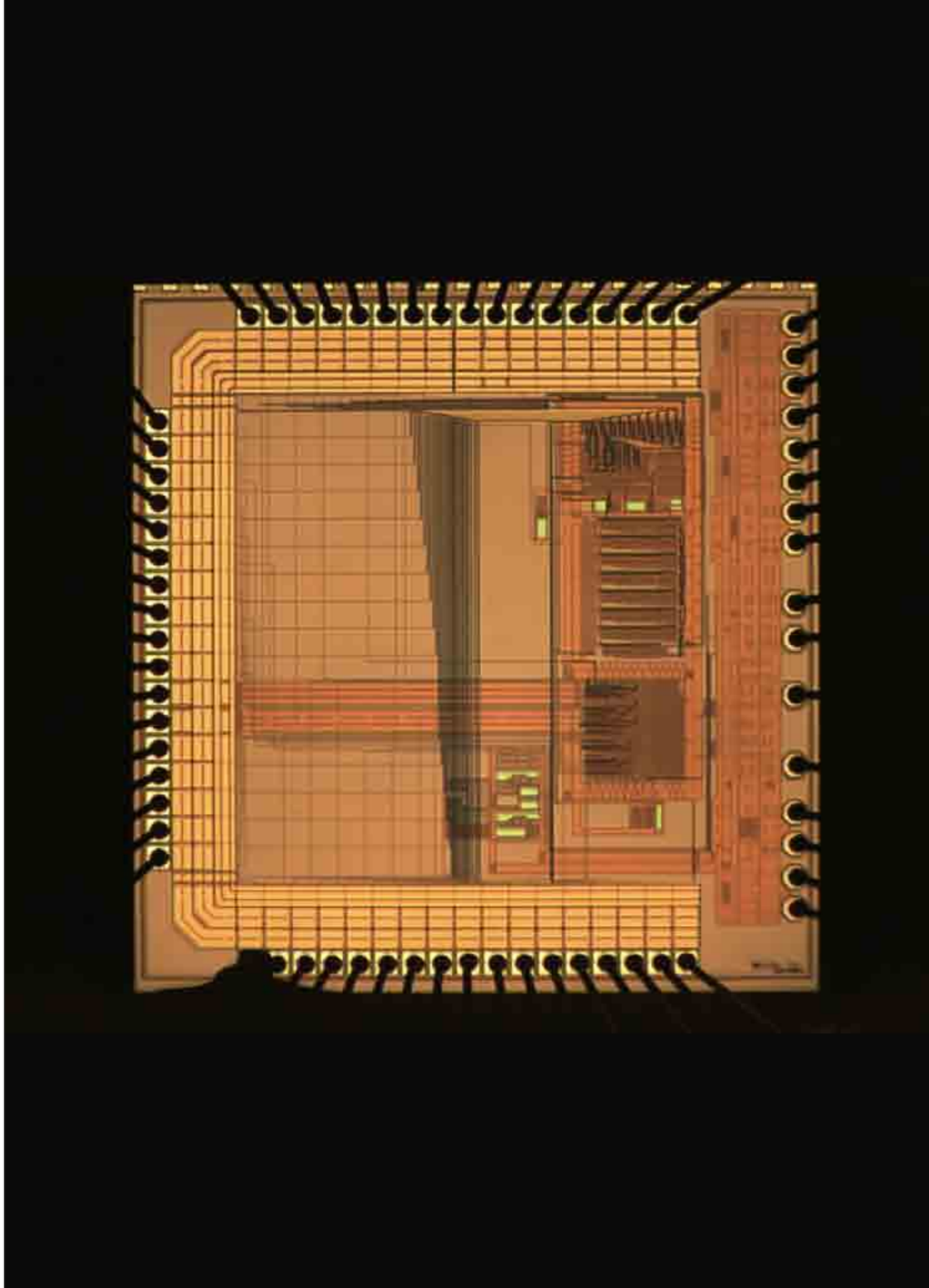
Since the beginning, the number of registered students range from 15 to 25. Students come from Seville (20-30%), Spain (30-40%), Europe (20-30%) and Latin America (20- 30%), meaning than 70-80% is abroad. International participation is about 40-50%.

The participation of CSIC members as Master professors is the following: 9 researchers involved, 17 ECTS out of 72 ECTS (23%). The participation of University Professors is the following: 22 professors, 55 ECTS out of 72 ECTS (77%). Only two professors do not belong to IMSE (6 ECTS).

INTERNSHIP PROGRAM

At the beginning of academic course 2011-2012 the Institute of Microelectronic of Seville started his Internship Program in cooperation with the University of Seville aimed to complement the student's academic background with the experience of a real job in a research institute. Though this program, students can develop the knowledge acquired during their Master studies while other very important aspect as responsibility and team ability are strengthened, improving their prospect of future employment.

Students who have joined the program (9 for years 2011 and 2012) have gained expertise in a wide variety of topics related to microelectronics, like handling of high-performance integrated circuit test equipment, analog and digital IC design flow, printed circuit board design or ICs demonstrators.



FUNDED PROJECTS

Funding for the research activities carried out at IMSE-CNM comes primarily from the participation in competitive tender processes. The research is then conducted out via agreements, projects and contracts with national and international public organizations and private companies and organizations.

MOBY-DIC

Model-based synthesis of digital electronic circuits for embedded control

PI: Antonio J. Acosta Jiménez
Reference: FP7-248858
Funding Body: Unión Europea

Start date: 01/12/2009
End date: 30/11/2012
Funding: 450.000 €

MOBY-DIC project is related to embedded control systems, providing a methodology and associated tool chain encompassing in a unique framework: modelling of the physical process, design of the control algorithms, design of embedded circuits, and the assessment of the overall performance properties of the system. MOBY-DIC will develop a core methodology based on 'piecewise affine' representations, providing a flexible structure for control functions, and directly mapped into digital architectures. The effectiveness of the developed embedded control design approach will be demonstrated on a set of challenging applications arising in the automotive industry.

NABAB

Nanocomputing building blocks with acquired behaviour

PI: Teresa Serrano Gotarredona
Reference: CE 216777
Funding Body: Unión Europea

Start date: 01/01/2008
End date: 31/03/2011
Funding: 316.625,30 €

Targeting the development of computing solutions complementing logic functions based on CMOS, the main objective of the NABAB project consists of 'demonstrating that it is possible to obtain useful computing functions as the result of a post-fabrication learning/adaptation process taking advantage of the rich functionality provided by interconnected nano devices'.

The NABAB project will explore the feasibility of a functional nano computing block (NAB) that will be built by interconnecting devices based on new nanoscale organic field-effect transistors (FET), functionalised nanotubes FET or ZnO FET that provide a rich combination of functions (memory and gain, sensitivity to various local or global stimuli).

The project will show, as a primary target, that such a NAB can acquire a specific, non-trivial, computing function by means of an internal adaptation process (learning, reconfiguration, self-organization). Besides, an important aspect of the project is to show that the acquired functionality of the NAB is exploitable within a realistic and larger computing system. To this extent an appropriate scheme for electrical and logical interfaces will be devised so as to make the function available at higher levels and relevant to realistic application concerns. Indeed competing advantages are sought on the one hand for reasons such as enabling the use of high parameter variability technologies, on the other hand for reasons such as providing novel functionalities (i.e. associative memory, classifiers) complementing classical logic functions.

In order to achieve the ambitious objectives of the NABAB project, the consortium involves 5 complementary research organisations with the necessary excellence in domains like nano and molecular electronics devices, computing architecture, neural networks and analogue design.

CB-DOC

Content management system with secure authentication by cripto-biometric techniques based on hardware

PI: Iluminada Baturone Castillo
Reference: IPT-2012-0695-390000
Funding Body: M. de Economía y Competitividad

Start date: 17/07/2012
End date: 31/12/2014
Funding: 141.790 €

The main objective of this project is to achieve that the components of a content management system (CMS) form a chain of trust thanks to the inclusion of hardware solutions besides software solutions. The consequences of an insecure CMS can be dramatic not only from a personal point of view, but also for the enterprises or corporations, beca use the lost of sensitive information carries out economic and/or legal problems. The project will develop a mixed software/hardware platform (referred to as CB-DOC) to

manage contents and documents, which will be highly secure beca use it will apply cryptographic and biometric techniques from a hardware element (referred to as epadlock) that will be difficult to be cloned.

RTDS

Architectures and circuits for logic and non-linear applications using RTDs

PI: María J. Avedillo de Juan
Reference: TEC2010-18937
Funding Body: M. de Ciencia e Innovación

Start date: 01/01/2011
End date: 30/06/2014
Funding: 109.505,01 €

Augmenting the CMOS technology with other devices/components will allow the semiconductor industry to progress significantly. In this line, this project focuses the addition of Resonant Tunneling Diodes (RTDs). These devices exhibit interesting characteristics of speed and negative differential resistance (NDR) in their I-V characteristic, have shown their usefulness to reduce circuit complexity and, there are many III-V demonstrators showing area and power reductions and speed advantages. Within the context of previous projects funded by the Spanish Research Program (TEC2004-02948 y TEC2007-67245) we have obtained experience in the design of circuits combining RTDs and transistors. The project aims at achieving progress in two different lines: application of RTDs to high performance digital circuits and application to non-linear circuits.

Concerning digital design, the initial hypothesis is that the easiness with which RTDs implement static holding and the high current they exhibit for low voltages make them excellent candidates to implement dynamic logic-based pipelines, widely used in high speed applications, with competitive performance in terms of frequency and energy efficiency.

With respect to non-linear applications, we have deeply analyzed the dynamics of circuits comprising RTDs and laser diodes with application in optical communication systems and have identified alternative topologies that we think are interesting for exploration.

This project will allow to exploit our previous experience, to converge with very active research lines and to consolidate our position among international groups working in the development and application of this quantum devices.

The precise objectives of the projects are: a) Development and validation of logic architectures competitive in terms of energy and speed in RTD/CMOS technologies and b) Analysis and prototyping of circuits which take advantage of strong non-linearity of RTDs for chaos generation, frequency division and phase locking.

CITIES

Circuitos integrados para transmision de información especialmente segura

PI: Carlos J. Jiménez Fernández
Reference: TEC2010-16870
Funding Body: M. de Ciencia e Innovación

Start date: 01/01/2011
End date: 30/09/2014
Funding: 106.722 €

This project is intended to produce high-performance hardware implementations in nanometric CMOS technologies, providing a solution to the problem of secure transmission and authentication in applications of communication between portable devices.

Within the vast world of cryptography, stream ciphers are used for the secure transmission of information and hash functions as the authentication mechanism, because both offer effective solutions with lower consumption of resources and power. Algorithms better suited to implementation in hardware will be selected and optimized, and architectures optimized both in terms of VLSI design (area, frequency and power consumption) and lateral techniques to prevent attacks will be proposed. Consider these factors in combination will optimize the performance of systems, achieving reductions in any of the parameters without affecting the performance of the circuit.

The three main objectives of the project are:

- Exploration of cryptographic algorithms from the security and hardware implementation points of view, and the attacks they may face.
- Develop efficient architectures for these algorithms, optimized in aspects of VLSI design (resource consumption, operating frequency, power consumption, etc.), and resistant to side attacks.
- Design, manufacture and test in nanometric CMOS technologies a prototype covering all aspects of secure transmission and authentication.

PNEUMA

Plasticity in NEUral Memristive Architectures

PI: Bernabé Linares Barranco
Reference:
Funding Body: Ministerio de Ciencia e Innovación

Start date: 01/09/2011
End date: 01/09/2014
Funding: 89.000 €

This project aspires to develop experimental platforms capable of perceiving, learning and adapting to stimuli by leveraging on the latest developments of five leading European institutions in neuroscience, nanotechnology, modeling and circuit design. The non-linear dynamics as well as the plasticity of the newly discovered memris-

tor are shown to support Spike-based- and Spike-Timing-Dependent-Plasticity (STDP), making this extremely compact device an excellent candidate for realizing large-scale self-adaptive circuits; a step towards 'autonomous cognitive systems'. The intrinsic properties of real neurons and synapses as well as their organization in forming neural circuits will be exploited for optimizing CMOS-based neurons, memristive grids and the integration of the two into real time biophysically realistic neuromorphic systems. Finally, the platforms would be tested with conventional as well as abstract methods to evaluate the technology and its autonomous capacity.

SEIS

Hardware design for embedded systems in intelligent environments

PI: Santiago Sánchez Solano
Reference: TEC2011-24319
Funding Body: Ministerio de Ciencia e Innovación

Start date: 01/01/2012
End date: 31/12/2014
Funding: 134.310 €

This project is aimed at exploring the use of new processing techniques and providing design tools that facilitate the development of embedded systems for intelligent environments. In order to achieve these goals we will, on the one hand, make use of soft-computing techniques to manage the inaccuracy and ambiguity of information supplied by the sensors, implement approximate inference mechanisms that emulate the human reasoning, and facilitate human-machine interaction by means of descriptions in natural language. On the other hand, we will develop new methodologies and design techniques to make it easier to explore the design space of proposed solutions.

DANTE

Adapting Mixed-signal and RF ICs Design and Test to Process and Evironment Variability

PI: Adoración Rueda Rueda
Reference: TEC2011-28302
Funding Body: Ministerio de Ciencia e Innovación

Start date: 01/01/2012
End date: 31/12/2014
Funding: 276.122 €

This project aims to face design and test challenges arisen in nanometer CMOS. It will contribute with new techniques for adapting the design and test of AMS/RF devices to process and environment variations, paving the way to the development of robust complex chips. The project is intended for dealing with three main macro-objectives:

» The development of adaptive design techniques supporting tuning and/or calibration of circuits to face up process and environment variations.

» The search for DfT (Design-for-Test) and BIST (Built-in self-test) solutions, directed towards facilitating component test at different abstraction levels inside a complex integrated system.

» The devising of new experimental paradigms to verify in a lab the different concepts, methods and techniques developed in the first two bullets above. In particular, the development of experimental methodology to evaluate the sensitivity of the proposed test and calibration techniques to Single-Event Effects (SEE).

INNPACTO3 D2

Intelligent Image Sensors in CMOS Technology with 3D Stacked Chips

PI: Ángel Rodríguez Vázquez
Reference: IPT-2011-1625-430000
Funding Body: Ministerio de Ciencia e Innovación

Start date: 01/01/2011
End date: 31/12/2014
Funding: 402.942,50 €

This research deals with the incorporation of 3D visual capabilities, i.e. the generation of a depth map, to the set of functionalities implemented in a smart CMOS image sensor. The techniques explored in this project are based in the estimation of the time-of-flight (ToF), both by properly clocked conventional integrating photodiodes, or by using CMOS-compatible single-photon avalanche diodes. Another objective is the incorporation of intelligent processing at chip level in order to enhance 3D information extraction.

FENIX-SDR

FlExible Nanometer CMOS Analog Integrated Circuits for the NeXt Generation of Software-Defined-Radio Mobile Terminals

PI: José M. de la Rosa Utrera
Reference: TEC2010-14825
Funding Body: Ministerio de Ciencia e Innovación

Start date: 01/01/2011
End date: 31/12/2014
Funding: 236.676 €

The main objective of this project is the systematic design of flexible Radio-Frequency (RF), Analog and Mixed-Signal (AMS) circuits to be incorporated in Software-Defined-Radio (SDR)-based transceivers intended for future Cognitive-Radio (CR) applications. To this purpose, the project will focus on the design, implementation using nanometer CMOS technologies (45nm and beyond) and experimental characterization of flexible digitally-assisted RF/AMS front-ends as well as their supporting design methodologies. This ambitious objective goes beyond state-of-the-art multi-standard ICs-based on in-

cluding adaptability capabilities to RF/AMS circuits.

CISMAE

Mixed-Signal Integrated Circuits for Space Applications

PI: Servando Espejo Meana
Reference: AYA2011-29967-C05-05
Funding Body: Ministerio de Ciencia e Innovación

Start date: 01/01/2012
End date: 31/12/2013
Funding: 242.000 €

IMSE's sub-project within CISMAE focused on finalizing the designs of the two ASICS developed in the MEIGA project, and evaluating their radiation and extreme temperatures robustness. The designs of the analog front-end ASIC for space-use has been improved, and radiation tests on the OWLS and MOURA chips have been performed. A new RHBD digital library has also been developed, improving the performance of that developed in the MEIGA project. Robustness against SEEs has been experimentally measured using the Cyclotron at Université Catholique de Louvain. TID robustness tests are currently underway at the facilities of Centro Nacional de Aceleradores.

POWDERS

Power-Optimized Wireless DEvices for the Remote Sensing of biomedical potentials

PI: Manuel Delgado Restituto
Reference: TEC2009/08447
Funding Body: Ministerio de Ciencia e Innovación

Start date: 01/01/2010
End date: 30/06/2013
Funding: 265.716 €

This project aims to contribute on the implementation of microelectronic circuits for wireless sensing biomedical potentials. More precisely, the main objective is to investigate architectures and circuit techniques for the implementation of low-area, ultra-low power CMOS biomedical sensors able to operate from about 1V voltage supply. The Project will also get on to power management issues and the wireless transmission of clinically relevant information. The monolithic realization of these biosensors implies several challenging design tasks in a wide range of frequencies, from nearly DC up to the GHz band. At low frequencies, in the mHz to kHz range, advances on the design of low-noise (below 2Vrms) low-power (below 1W) amplifiers for biopotential measurements, as well as on the design of variable gain and band-pass filtering stages will be pursued. Together, the design of analog-to-digital (A/D) converters with ultra-low power consumption (in the order of W) and variable data rates (from 1 to 160kbps) will be covered. In order to avoid the inconvenience of internal batteries, short-distance wireless powering techniques based on inductive links will be proposed. At higher frequencies, in the GHZ range, techniques for the wireless transmission of information using low-complexity modulation schemes (FSK-like) will be explored for use in biosensors. In order to limit transmission rates and, thereafter, further decrease power consumption, data reduction techniques to extract patterns of biomedical interest will be implemented on-chip. The design techniques developed in the Project will be demonstrated by two biosensor silicon integrations, together with other testchips for the partial evaluation of relevant circuit components. Both prototypes will preferably use a low-cost 130nm CMOS technology. A first prototype will consist on a biosensor node for the monitoring of ECG waveforms and will use the 2.4GHz ISM band for data transmission. A second prototype will implement a multi-point neural recording system and will use the same inductive link for both powering and communication. For both prototypes, the design of specific lab platforms and testing protocols will be addressed and, only in the case of the ECG sensor node, field measurements using commercial electrodes will be realized.

VULCANO

Ultra-fast frame-less visión by events. Aplication to automotion and anthropomorphic cognitive robotics

PI: Teresa Serrano Gotarredona
Reference: TEC2009-10639-C04-01
Funding Body: M. de Ciencia e Innovación

Start date: 01/01/2010
End date: 31/10/2013
Funding: 148.588,01 €

The VULCANO project aims at exploiting the great potential of the AER (Address Event Representation) technology for very high speed vision sensing and processing as well as for mechanical actuators and motors control in Neuro-robotics. In conventional vision, a video camera captures sequences of still frames or images, each of whichhas to be processed by sophisticated algorithms if automatic recognition tasks are desired (in automotion, robotics, etc).AER is based on a different concept which mimics the structure and information coding of the brain. In AER each sensor pixel sends information events when it detects a given level of a visual property (motion, contrast, luminance, ...). This way, the sensor output is a continuous flow of information (spatial and temporal) which is not restricted to discrete frames. This continuous flow of visual information is sent to a hierarchical structure, which mimics the neurocortex, and extracts relevant information in a continuous and parallel manner event after event, without waiting for frames. The AER philosophy allows to assemble scalable neurocortical systems: for example, to augment the catalog of known objects one only needs to add more AER modules in parallel which does not degrade speed (as happens in the brain).In recent research projects (national and european) the research teams of the VULCANO project have developed several vision sensors, have developed the first sufficiently generic programmable reconfigurable neurocortical processing modules to allow assembly of neurocortical structures for 3D object recognition, and have contributed to the development of motor control

in robotics applications. Very high speed object recognition has been proven, as well as the modularity and scalability properties of AER systems.The objective of the VULCANO project is to perform the necessary steps for developing a set of demonstrators to validate this vision and mechanical actuating sensing and processing technique for applications of interest in industrial sectors.

WIVISNET

Wireless and smart vision sensors for networked surveillance and monitoring

PI: Ricardo Carmona Galán
Reference: TEC2009-11812
Funding Body: Ministerio de Ciencia e Innovación

Start date: 01/01/2010
End date: 31/12/2012
Funding: 81.796 €

The convergence of computer vision, embedded systems, sensor networks and integrated image sensors allows us to think on the physical implementation of decentralized processing systems able to realize real-time distributed vision tasks over image flows coming from different video sources. The fundamental element in these distributed systems is the smart camera. The camera now becomes something beyond an array of photosensors with some signal accommodation. The smart camera is able to locally process the captured images and elaborate abstract representations. The relevant information is shared at a much lower communication cost, because the reduced number of data to be transmitted. This energy savings are partly invested in the in-node realization of the required computing power.

MEIGA-PRECURSOR

Design and Test of ASICs for a Space Mission to Mars

PI: Servando Espejo Meana
Reference: AYA2009-14212-C05-04
Funding Body: M. de Ciencia e Innovación

Start date: 01/01/2010
End date: 31/12/2012
Funding: 955.900 €

IMSE's participation in the MEIGA project had the objective of developing two mixed-signal ASICs for space use. After selecting a specific CMOS technology (AMS 0.35um) for the ASICs, the effects of radiation (single-events effects, SEE, and total ionizing dose, TID) on individual devices and digital blocks was studied using several test chips. Extreme temperatures effects were also observed experimentally. Different radiation hardening by design (RHBD) techniques have been evaluated, and the CAD design kit has been adapted to allow their use. A library of RHBD digital cells has been developed, including every aspect required to allow its use in conventional digital design flows. The mixed-signal ASICs developed are a transceiver for diffuse light intra-satellite communications (OWLS), and an analog front-end for sensor's signal adaptation and conversion aimed to magnetometer and accelerometer applications (MOURA).

DIMISION

Diseño microelectrónico de sistemas de visión para redes de sensores inteligentes

PI: Santiago Sánchez Solano
Reference: TEC2008-04920
Funding Body: Ministerio de Ciencia e Innovación

Start date: 01/01/2009
End date: 30/06/2012
Funding: 149.314 €

This project aims to promote the development of sensor networks with vision capabilities and its application to environmental conservation tasks. To this end, we define three general objectives: 1) application of Soft Computing techniques to improve the efficiency of basic tasks related to image processing, communication protocols and coordination mechanisms for sensor network nodes; 2) to provide electronic components, design methodologies, and platforms for developing systems using the aforementioned techniques; and 3) to implement a prototype of a distributed vision system that illustrates its applicability in the environmental conservation area.

TEST

Técnicas para mejorar la calidad del test y las prestaciones del diseño en tecnologías CMOS submicrónicas

PI: José L. Huertas Díaz
Reference: TEC2007-68072/MIC
Funding Body: Ministerio de Educación y Ciencia

Start date: 01/10/2007
End date: 31/03/2011
Funding: 307.582 €

The basic objective of this project is the exploration and development of new methods, procedures and techniques to address jointly the design and test of analog and mixed-signal integrated circuits in advanced CMOS technologies. The specific objectives are the development of new paradigms to improve mixed-signal circuits performance, generation of new alternative methods to characterize and test mixed-signal ICs, new design-for-test techniques development and BIST application for mixed-signal circuit. All techniques developed were evaluated through the use of practical demonstrators.

SR2

Short Range Radio

PI: Adoración Rueda Rueda
Reference: TSI-020400-2010-55
Funding Body: Ministerio de Industria, Turismo y Comercio

Start date: 01/01/2010
End date: 31/12/2011
Funding: 147.839 €

- Development of constructive blocks, integrated circuits and multi-standard or multi-physical layer platforms for the future devices, which will have to manage this variety of protocols in an acceptable range to ensure their place in the market.
- Investigating and implementing very low consume solutions, and to contribute to the rising WPAN and WBAN standards, paying special attention to the imminent IEEE standard BAN.
- Developing multi-mode Bluetooth chips and reconfigurable chips, capable of operating over several physical layers foreseen in the family of standards IEEE 802.15.
- Reaching interoperability and coexistence of the developed solutions, by means of the development and evaluation of prototypes over multi-standard tests.
- Integration and validation of the specific devices for domestic monitorization.

FORTIN 2011/2012

Fortalecimiento institucional de las actividades de postgrado e investigación en sistemas electrónicos integrados en el Instituto Superior Politécnico José Antonio Echeverría para el avanza en I+D+i en la sociedad cubana

PI: Ángel Barriga Barros
Type: International cooperation project
Reference: A1/039607/11
Funding Body: M. de Asuntos Exteriores

Start date: 13/12/2011
End date: 13/03/2013
Funding: 99.900 €

The basic objective of the project is to contribute to institutional strengthening of the ISPJAE, causing consolidate and reinforce its leadership in Cuba, and spread to the region as a center of reference in graduate and research activities related to electronic systems, enabling the development of collaborative curricular PhD program in electronics between the ISPJAE and the University of Seville, based on the on-line Master in Microelectronics of the University of Seville.

ACATEX

Self-calibration and self-test of analog, mixed-signal and radio frecuency circuits

PI: Adoración Rueda Rueda
Reference: P09-TIC-5386
Funding Body: Junta de Andalucía

Start date: 03/02/2010
End date: 30/06/2014
Funding: 323.939,68 €

The aim of this project is twofold. On one hand, concepts such as robustness against technological and environment variability, digital calibration, self-correction, and self-tuning are developed in the context of advanced systems for wireless communication and space applications. On other hand, activities related to the development of simple and low-cost functional testing techniques and structural design-for-test will be faced in advanced CMOS technologies to develop BIST techniques to reduce test complexity and to manage access to the internal IP blocks in SoCs (Systems on Chip).

CRIPTO-BIO

Diseño microelectrónico para autenticación cripto-biométrica

PI: Iluminada Baturone Castillo
Reference: P08-TIC-03674
Funding Body: Junta de Andalucía

Start date: 13/01/2009
End date: 31/12/2013
Funding: 439.847,36 €

This project addresses the hardware challenges that appear in secure human authentication systems in application domains with restrictive area, power, and speed constraints. Such constraints (which are severe in the case of mobile phones, PDAs, or RFIDs) are even more severe in the case of smart cards, especially contactless ones. Hardware challenges appear at several levels in the system design: from the selection of the processing and communication algorithms and protocols (at the highest level) to the choice of logic families and digital design styles of the circuit implementing them (at the lowest level).

At high level, the cryptographic and biometric algorithms (especially the last ones) can be computationally costly. As a matter of fact, most of current systems implementing biometric techniques separate the recognition process into two parts. Extraction of biometric features, which is computationally costly, is implemented outside the embedded product, and matching, which is simple, is implemented in the embedded product by comparing a stored template with the information provided by the external device. This solution, known as 'match on card', requires the communication of personal data between devices, which may be unsecure. In contrast, a system based on 'authentication on card' is less vulnerable because all recognition process is carried out within the same device. Hence, 'authentication on card' solutions are pursued in this project.

At low level, the hardware can reveal sensitive information when side channel attacks are carried out. Hence, other objectives of the project are to analyze the robustness of the designs against those attacks, in particular to differential power attacks (DPA), as well as to improve such robustness with adequate countermeasures.

MV-NDR

Diseño e implementación de circuitos multivaluados usando dispositivos con características NDR

PI: José M. Quintana Toledo
Reference: P07-TIC-02961
Funding Body: Junta de Andalucía

Start date: 31/01/2008
End date: 31/12/2012
Funding: 70.000 €

This project aims to develop design techniques for integrated circuits that exploit the advantages of speed, power consumption and reduced complexity, demonstrated in III/V technologies, which are offered by RTDs (Resonant Tunneling Diodes). The advantages offered by RTDs circuits when compared to conventional implementations are associated with the presence of an NDR (Negative Differential Resistance) region in their I-V characteristics.

In addition to scaling, the incorporation of new devices generally based on quantum effects is considered a well-established way to extend the CMOS life. In particular, RTDs have been proposed as candidates for short-term incorporation into VLSI technologies. Additionally, multiple peaks devices (and multiple NDR zones) in their I-V characteristics allow in a natural way a multiple-valued operation and, associated with it, redundant number systems in a digit level. Moreover, it is well known that the circuit reliability is an important challenge in the current design. Using emerging devices worse this reliability because the ratio of manufacturing defects is quite high and, additionally, much of the information processing is performed in a multiple-valued or even analog (low accuracy) way. Thus, the reliability becomes a commitment of the highest order.

PLATFORM4G

Desarrollo de una plataforma de diseño de sistemas adaptables para sistemas de telecomunicaciones de cuarta generación

PI: Francisco V. Fernández Fernández
Reference: P07-TIC-02532
Funding Body: Junta de Andalucía

Start date: 31/01/2008
End date: 31/12/2012
Funding: 303.000 €

Future 4G wireless communications devices will have to include in a unique device four different communication services, therefore supporting four different communication standards. Technical and economical viability of these devices will only be possible if they can be fabricated in lower cost technologies, designed in an acceptable time schedule and with an optimized power consumption, so that the battery life can be extended.

Multimode communication requirements together with the need to integrate these devices in hostile technologies for analog and radio frequency circuits, pose new challenges to designers in this field.

The aim of this project is to develop new design platforms for 4th generation reconfigurable communication systems that can support these challenges. These platforms describe the components of these systems at different leves of abstraction, indicating how to compose them and how to transfer information between levels.

As part of the validation process, different reconfigurable subsystems (both mixed-signal and radio frequency circuits) of a 4G communication transceiver will be designed and fabricated in nanometer CMOS technologies.

BIOTAG

Monolithic Implementation of Passive RFID Transponders for Biomedical Applications

PI: Manuel Delgado Restituto
Reference: TIC-02818
Funding Body: Junta de Andalucía

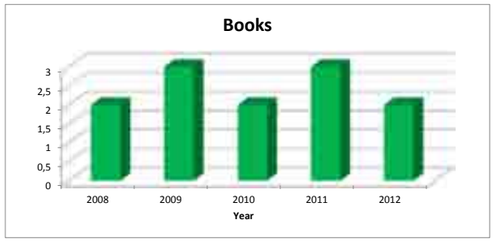
Start date: 31/01/2008
End date: 31/12/2012
Funding: 119.168 €

The ability of sensor-enabled RFID transponders (sensor tags) to monitor, record and even react to ambient conditions is expected to promote a new world of applications far beyond a simple barcode system replacement. In these tags, the information delivered to the reader may not only consist on identification data but also contain environmental readouts (e.g., temperature, pressure, optical or chemical variables) obtained from a companying sensor. In this project, a passive sensor tag targeting the EPC Gen2 protocol is designed and implemented in a 0.35µm CMOS process. The tag, conceived as a wearable device for physiological signal monitoring, can be embedded in a conventional clinical patch and includes two sensors one for measuring body temperature and the other for heart rate monitoring. The design includes a fully EPC-compliant baseband processor, which meets the PER specifications of the standard and is able to tolerate master clock frequency deviations as high as 15% from nominal. Sensor reso lutions are suitable for typical clinical applications.

PUBLICATIONS

BOOKS

Evolution of number of books published by IMSE during the period 2008-2012.



2011

Device-level modeling and synthesis of high-performance pipeline ADCs
J. Ruiz-Amaya, M. Delgado-Restituto and A. Rodríguez-Vázquez
SPRINGER.DOI: 10.1007/978-1-4419-8846-1; ISBN: 978-1-4419-8845-4

This book presents models and procedures to design pipeline analog-to-digital converters, compensating for device inaccuracies, so that high-performance specs can be met within short design cycles. These models are capable of capturing and predicting the behavior of pipeline data converters within less than half-a-bit deviation, versus transistor-level simulations. As a result, far fewer model iterations are required across the design cycle. Models described in this book accurately predict transient behaviors, which are key to the performance of discrete-time systems and hence to the performance of pipeline data converters.

Mining and control of network traffic by computational intelligence
F. Montesino-Pouzols, D.R. López and A. Barriga-Barros
SPRINGER. ISBN: 978-3-642-18083-5

As other complex systems in social and natural sciences as well as in engineering, the Internet is hard to understand from a technical point of view. Packet switched networks defy analytical modeling. The Internet is an outstanding and challenging case because of its fast development, unparalleled heterogeneity and the inherent lack of measurement and monitoring mechanisms in its core conception. This monograph deals with applications of computational intelligence methods, with an emphasis on fuzzy techniques, to a number of current issues in measurement, analysis and control of traffic in the Internet. First, the core building blocks of Internet Science and other related networking aspects are introduced. Then, data mining and control problems are addressed. In the first class two issues are considered: predictive modeling of traffic load as well as summarization of traffic flow measurements. The second class, control, includes active queue management schemes for Internet routers as well as window based end-to-end rate and congestion control. The practical hardware implementation of some of the fuzzy inference systems proposed here is also addressed. While some theoretical developments are described, we favor extensive evaluation of models using real-world data by simulation and experiments.

Nanometer CMOS Sigma-Delta Modulators for Software Defined Radios
A. Morgado, R. del Río and J.M. de la Rosa
SPRINGER. DOI: 10.1007/978-1-4614-0037-0; ISBN: 978-1-4614-0036-3 (Print) 978-1-4614-0037-0

This book presents innovative solutions for the implementation of Sigma-Delta Modulation (SDM) based Analog-to-Digital Conversion (ADC), required for the next generation of wireless hand-held terminals. These devices will be based on the so-called multistandard transceiver chipsets, integrated in nanometer CMOS technologies. One of the most challenging and critical parts in such transceivers is the analog-digital interface, because of the assorted signal bandwidths and dynamic ranges that can be required to handle the A/D conversion for several operation modes. This book describes new adaptive and reconfigurable SDM ADC topologies, circuit strategies and synthesis methods, specially suited for multi-standard wireless telecom systems and future Software-defined-radios (SDRs) integrated in nanoscale CMOS. It is a practical book, going from basic concepts to the frontiers of SDM architectures and circuit implementations, which are explained in a didactical and systematic way. It gives a comprehensive overview of the state-of-the-art performance, challenges and practical solutions, providing the necessary insight to implement successful design, through an efficient design and synthesis methodology. Readers will learn a number of practical skills from system-level design to experimental measurements and testing.

2012

Design of analog circuits through symbolic analysis
M. Fakhfakh,(Ed.), E. Tlelo-Cuautle and F.V. Fernandez-Fernandez (Co-Eds.)
BENTHAM. DOI: 10.2174/ 97816080509561120101; ISBN: 978-1-60805-425-1

This edited book provides an overview of the current state of the art in symbolic analysis. The editors have compiled chapters from the key contributors to the field of symbolic analysis. These chapters neatly describe the latest results in terms of algorithms as well as applications of symbolic analysis techniques for analog circuits. Recent algo-

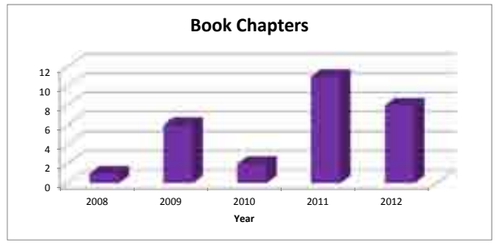
rithmic improvements highlight the potential of today´s symbolic analysis methods, both in terms of circuit complexity and of circuit characteristics that can be analyzed. The second part of the book presents the wide span of applications that utilize symbolic analysis, ranging from behavioral and performance modeling over design centering and fault diagnosis to automated design and system architectural exploration. These chapters clearly demonstrate the potential of symbolic analysis for analog circuits, in complement to or in combination with numerical simulation techniques.

Low-power smart imagers for vision-enabled sensor networks
J. Fernández-Berni, R. Carmona-Galán and A. Rodríguez-Vázquez
SPRINGER. ISBN: 978-1-4614-2391-1

This book presents a comprehensive, systematic approach to the development of vision system architectures that employ sensory-processing concurrency and parallel processing to meet the autonomy challenges posed by a variety of safety and surveillance applications. Coverage includes a thorough analysis of resistive diffusion networks embedded within an image sensor array. This analysis supports a systematic approach to the design of spatial image filters and their implementation as vision chips in CMOS technology. The book also addresses system-level considerations pertaining to the embedding of these vision chips into vision-enabled wireless sensor networks.

BOOK CHAPTERS

Evolution of number of book chapters contributed by IMSE during the period 2008-2012.



2011

A focal plane processor for continuous-time 1-D optical correlation applications
G. Liñán-Cembrano, L. Carranza, B. Alexandre, A. Rodríguez-Vázquez, P. de la Fuente and T. Morlanes
Focal-Plane Sensor-Processor Chips, pp 151-179, 2011
SPRINGER DOI: 10.1007/978-1-4419-6475-5_7 ISBN: 978-1-4419-6474-8

This chapter describes a 1-D Focal Plane Processor, which has been designed to run continuous-time optical correlation applications. The chip contains 200 sensory processing elements, which acquire light patterns through a 2mm×10.9µm photodiode. The photogenerated current is scaled at the pixel level by five independent 3-bit programmable-gain current scaling blocks. The correlation patterns are defined as five sets of two hundred 3-bit numbers (from 0 to 7), which are provided to the chip through a standard I2C interface. Correlation outputs are provided in current form through 8-bit programmable gain amplifiers (PGA), whose configurations are also defined via I2C. The chip contains a mounting alignment help, which consists of three rows of 100 conventional active pixel sensors (APS) inserted at the top, middle and bottom part of the main photodiode array. The chip has been fabricated in a standard 0.35µm CMOS technology and its maximum power consumption is below 30mW. Experimental results demonstrate that the chip is able to process interference patterns moving at an equivalent frequency of 500kHz.

Predictive models of network traffic load
F.M. Pouzols, D.R. López and A. Barriga-Barros
Mining and Control of Network Traffic by Computational Intelligence, Studies in Computational Intelligence, vol. 342, pp 87-145, 2011
SPRINGER DOI: 10.1007/978-3-642-18084-2_3 ISBN: 978-3-642-18083-5 ISSN: 1860-949X

Understanding the dynamics and performance of packet switched networks on the basis of measurements enables practitioners to optimize resources. As network measurement research further advances and new measurement tools and infrastructures are available, the task of network operation becomes more and more complex. In this chapter we apply the methodology developed in the previous chapter to time series concerning network traffic load. An extensive predictability analysis is performed using the same nonparametric residual variance estimation technique that is integrated into the prediction methodology. Based on the predictability results, fuzzy inference based models that are both interpretable and accurate are derived for a wide set of heterogeneous time series for network traffic.

Open FPGA-based development platform for fuzzy inference systems
F.M. Pouzols, D.R. López and A. Barriga-Barros
Mining and Control of Network Traffic by Computational Intelligence, Studies in Computational Intelligence, vol. 342, pp 263-304, 2011
SPRINGER DOI: 10.1007/978-3-642-18084-2_3 ISBN: 978-3-642-18083-5 ISSN: 1860-949X

This chapter looks into the practical implementation of some of the fuzzy inference systems proposed in previous chapters. Both architectural and operational constraints are considered. The focus is on an open FPGA-based hardware platform for the implementation of efficient fuzzy inference systems for solving problems in high-performance packet switched networks. A feasibility study is conducted in order to show that the techniques developed can be deployed in current and future network scenarios with satisfactory performance.

Behavioral Modeling of Mixed-Mode Integrated Circuits
E. Tlelo-Cuautle, E. Martínez-Romero, C. Sánchez-López, F.V. Fernández, Sheldon X.-D. Tan, Peng Li and M. Fakhfakh
Advances in Analog Circuits, Esteban Tlelo-Cuautle (Ed.), pp 85-108, 2011
INTECH DOI: 10.5772/15864 ISBN: 978-953-307-323-1

Improving the accuracy of RF alternate test using multi-VDD conditions: application to envelope-based test of LNAs

M.J. Barragán-Asián, R. Fiorelli-Martegani, G. Leger, A. Rueda and J.L. Huertas-Díaz

20th Anniversary Compendium of Papers from Asian Test Symposium, 2011

This work demonstrates that multi-VDD conditions may be used to improve the accuracy of machine learning models, significantly decreasing the prediction error. The proposed technique has been successfully applied to a previous alternate test strategy for LNAs based on response envelope detection. A prototype has been developed to show its feasibility. The prototype consists of a low-power 2.4GHz LNA and a simple envelope detector, integrated in a 90nm CMOS technology. Postlayout simulation results are provided to verify the functionality of the approach.

Hardware implementation of a real-time image segmentation circuit based on fuzzy logic for edge detection application

A. Barriga-Barros

Image Segmentation, Pei-Gee Ho (Ed.), pp 519-538, 2011

INTECH DOI: 10.5772/15519 ISBN: 978-953-307-228-9

In this chapter there has been described a mechanism for binary image segmentation based on the application of fuzzy logic to calculate the threshold. The described thresholding method allows to adjust the threshold value to the characteristics of the image. The main advantage of this technique is that it allows very efficient hardware implementation in terms of cost and speed. This makes it especially suitable for applications which require real time processing. This technique has been applied for edge detection in images. The designed circuit has been implemented on an FPGA device.

A low-power baseband processor for passive RFID tags employing low-power design techniques

J.A. Rodríguez-Rodríguez and M. Delgado-Restituto

Advances in RFID Tags, 2011

This chapter focuses on the design of the baseband processing section of a passive UHF RFID tag for half-duplex communications in the 860-960 MHz range, which implements the EPCTM Class-1 Generation-2 (Gen2) protocol. Besides serving identification purposes, the tag also includes a 10-bit, 2kS/s generic signal acquisition interface to allow for signal readouts from the environment (e.g., temperature, pressure, optical or chemical variables). This ability to monitor, record and even react to ambient conditions is expected to promote a new world of applications for RFIDs.

Given the complexity of the protocol and the lack of external batteries, as in the case of active transponders, design efforts has been directed towards minimizing the power consumption of the processor. To this end, different power saving techniques has been considered in the implementation. They include the use of clock gating and power down control strategies or the synthesis of dedicated clocks per processor task. Additionally, most of the blocks of the decoding section of the processor are operated by means of simple trigger pulses at a rate defined by the incoming data (much slower than the master clock signal). The combined effect of these techniques is that every element of the processor always operates at the lowest clock frequency possible and it is only active when strictly required. A sophisticated timing unit able to generate the different clock signals, block operation windows and trigger pulses is the responsible for the application of the aforementioned low-power design techniques.

The processor, which implements all the commands/actions defined by the Gen-2 protocol, has been implemented in a 0.35um CMOS technology process using automatic tools for both the logic synthesis and layout. It operates from a 1.2V supply voltage and uses a nominal master clock frequency of 1.92 MHz, enough to comply with the Gen2 requirements. Besides, the processor also includes a simple protocol for handling the signal captured from the sensor interface. This protocol takes advantage of commands already defined in the standard, namely, the Write command for reading and storing the captured data into the nonvolatile memory of the tag, and the Read command, for transferring the sensory information to the interrogator. The signal acquisition interface consists of a rail-to-rail input band-limited programmable gain amplifier followed by a capacitive DAC based Successive Approximation Register (SAR) ADC.

The power consumption of the processor has been measured assuming maximum bitrates for the forward and backward links. During a communication link involving five consecutive commands, the processor consumes less than 2.9uA, assuming worst-case timing conditions. Further, the signal acquisition interface consumes 130nA at 2kS/s and obtains 9.4 bits ENOB (58.4dB SNDR) for a full-scale 300Hz input tone.

ImagCell: A Computer Tool for Cell Culture Image Processing Applications in Bioimpedance Measurements

A. Yúfera, E. Gallego and J. Molina

Software Tools and Algorithms for Biological Systems, Advances in Experimental Medicine and Biology, Hamid R. Arabnia and Quoc-Nam Tran (Eds.), vol. 696, pp 733-740, 2011

SPRINGER DOI: 10.1007/978-1-4419-7046-6_75 ISBN: 978-1-4419-7045-9

This paper presents a computer tool for automatic analysis of cell culture images. The program allows the extraction of relevant information from biological images for pre- and postsystem analysis. In particular, this tool is being used for electrical characterization of electrode-solution-cell systems in which bioimpedance is the main parameter to be known. The correct modeling of this kind of systems enables both electronic system characterization for circuit design specifications and data decoding from measurements. The developed program allows cell culture image processing for geographic information extraction and generates cell count and equivalent circuit descriptions useful for system simulations.

Focal-plane dynamic texture segmentation by programmable binning and scale extraction
J. Fernández-Berni and R. Carmona-Galán
Focal-Plane Sensor-Processor Chips, Ákos Zarándy (Ed.), pp 105-124, 2011
SPRINGER DOI: 10.1007/978-1-4419-6475-5_5 ISBN: 978-1-4419-6474-8

Dynamic textures are spatially repetitive time-varying visual patterns that present, however, some temporal stationarity within their constituting elements. In addition, their spatial and temporal extents are a priori unknown. This kind of pattern is very common in nature; therefore, dynamic texture segmentation is an important task for surveillance and monitoring. Conventional methods employ optic flow computation, though it represents a heavy computational load. Here, we describe texture segmentation based on focal-plane space-scale generation. The programmable size of the subimages to be analysed and the scales to be extracted encode sufficient information from the texture signature to warn its presence. A prototype smart imager has been designed and fabricated in 0.35 µm CMOS, featuring a very low-power scale-space representation of used-defined subimages.

VISCUBE: A multi-layer vision chip
A. Zarándy, C. Rekeczky, P. Földesy, R. Carmona-Galán, G. Liñán-Cembrano, S. Gergely, A. Rodríguez-Vázquez and T. Roska
Focal-Plane Sensor-Processor Chips, pp 181-208, 2011
SPRINGER DOI: 10.1007/978-1-4419-6475-5_8 ISBN: 978-1-4419-6474-8

Vertically integrated focal-plane sensor-processor chip design, combining image sensor with mixed-signal and digital processor arrays on a four layer structure is introduced. The mixed-signal processor array is designed to perform early image processing, while the role of the digital processor array is to accomplish foveal processing. The architecture supports multiscale, multifovea processing. The chip has been designed on a 0.15um feature sized 3DM2 SOI technology provided by MIT Lincoln Laboratory.

Application of fuzzy logic and Lukasiewicz operators for image contrast control
A. Barriga, A and N.M. Hussein-Hassan
New Advances in Intelligent Signal Processing, Studies in Computational Intelligence, Antonio E. Ruano and Annamária R. Várkonyi-Kóczy (Eds.) vol. 372, pp 133-154, 2011
SPRINGER DOI: 10.1007/978-3-642-11739-8_7 ISBN: 978-3-642-11738-1

This chapter reviews image enhancement techniques. In particular the chapter is focused in soft computing technique to improve the contrast of images. There is a wide variety of contrast control techniques. However, most are not suitable for hardware implementation. A technique to control the contrast in images based on the application of Lukasiewicz algebra operators and fuzzy logic is described. In particular, the technique is based on the bounded-sum and the bounded-product . The selection of the control parameters is performed by a fuzzy system. An interesting feature when applying these operators is that it allows low cost hardware realizations (in terms of resources) and high processing speed.

Cell biometrics based on bio-impedance measurements
A. Yúfera, A. Olmo, P. Daza, P and D. Cañete
Advanced Biometric Technologies, Girija Chetty and Jucheng Yang (Eds.), pp 343-366, 2011
INTECH DOI: 10.5772/21742 ISBN: 978-953-307-487-0

Many biological parameters and processes, like cell growth, cell activity, changes in cell composition, shapes or cell location can be sensed and monitored using their impedance as marker, with the advantage that it is a non-invasive and a relative cheap technique. Through this chapter, we will introduce the Electrical Cell-substrate Impedance Spectroscopy (ECIS) technique to determine the biological condition of cells and the strategy adopted to determine a proper relationship between real-word and simulation models. The second section gives a brief overview of electrode solution models useful for cell-electrode characterization. The third section presents a useful method for generating cell-electrode electrical models based on COMSOL multiphysics software. The fourth section describes the finite element simulations performed. Processes for extracting useful models are included in the fifth section, which also illustrates cell size detection simulations on a simplified system. AHDL models are presented in sixth section. The seventh section covers the real time monitoring of the cell under cultivation and the application of the proposed model in dosimetric experiments. Finally, in the eighth section, a two dimensional approach to bioimpedance microscopy is described, based on the models previously developed. Conclusions are given in the ninth section.

Closing the gap between electrical and physical design: the layout-aware solution
R. Castro-López, E. Roca and F.V. Fernández
Analog layout synthesis. A Survey of Topological Approaches, Helmut E. Graeb (Ed.), pp 243-268, 2011
SPRINGER DOI: 10.1007/978-1-4419-6932-3_6 ISBN: 978-1-4419-6931-6

Iterations between separate phases in any procedural design process, usually a by-product of unexpected (or, simply, very complex to consider) adverse effects, clearly play against any time-to-market requirements. In analog integrated circuit (IC) design, going back and forth between electrical and physical synthe- sis to counterbalance layout-induced performance degradations needs to be thus avoided as much as possible. One possible solution involves the integration of the 1 traditionally separated electrical and physical synthesis phases, by including layout- induced effects, in the form of layout parasitics, right into the electrical synthesis phase, in what has been called parasitic-aware synthesis. This solution, as such, is not yet complete since there are geometric requirements (minimization of the occupied area or fulfillment of certain layout aspect ratio, among others), whose effects on the resulting parasitics are not usually considered during electrical synthesis. In this chapter, a layout-aware solution that tackles both geometric and parasitic-aware electrical synthesis is proposed. This technique uses a combination of simulation- based optimization, procedural layout generation, exhaustive geometric evaluation algorithms, and several mechanisms for parasitic estimation. Thanks to the nature of this combination, the solution benefits from, and also fosters, reuse of analog intellectual property (IP) blocks. Several detailed design examples are provided.

Power efficient ADCs for biomedical signal acquisition
A. Rodríguez-Pérez, M. Delgado-Restituto and F. Medeiro
Biomedical Engineering, Trends in Electronics, Communications and Software, pp 171-192, 2011
INTECH ISBN: 978-953-307-475-7

Rapid technological developments in the last century have brought the field of biomedical engineering into a totally new realm. Breakthroughs in materials science, imaging, electronics and, more recently, the information age have improved our understanding of the human body. As a result, the field of biomedical engineering is thriving, with innovations that aim to improve the quality and reduce the cost of medical care. This book is the first in a series of three that will present recent trends in biomedical engineering, with a particular focus on applications in electronics and communications. More specifically: wireless monitoring, sensors, medical imaging and the management of medical information are covered, among other subjects.

Evaluación multiagente en la formación de profesores noveles
J. Benjumea, A. Estrada, E. Ostúa, O. Rivera, J. Ropero, F. Sivianes and M. Valencia
Programa de equipos docentes para la formación de profesores noveles, pp 263-275, 2011
FÉNIX EDITORA ISBN: 978-84-86849-73-3

Six new teachers and a mentor in Electronic Technology present the results of their participation within a training program for novel teachers. Regarding the 4-type observation activities, different evaluation instruments (quantitative/qualitative, closed/open) and different observation agents have been used (the novel himself/herself, his/her students, the mentor and pedagogue specialists). In this work, the main results that all novel teachers have achieved in these evaluations are presented. The results are broadly consistent with the analysis of the different agents. The improvable aspects of the program are also extracted and its main benefit is highlighted: the enhancement of the teaching capacities of the participants.

Experiencias del equipo docente de iniciación en el departamento de tecnología electrónica
G. Miró-Amarante, J. Viejo and M. Valencia
Programa de equipos docentes para la formación de profesores noveles, pp 395-404, 2011
FÉNIX EDITORA ISBN: 978-84-86849-73-3

A new experience with novel lectures has been developed during the academic year 2007-2008 at Electronic Technology Department. The lectures have followed the "Teaching Groups for New Lectures Training Programme" at the University of Seville. The aim of this programme is to provide them with a source of help and advice on learning and teaching covering all aspects of their professional role.

This paper describes the beginning of the Electronic Technology Department teaching group, the face-to-face and online activities developed during the academic year 2007-2008 and the main results. Furthermore, positive and negative points of the Training Programme are listed.

Performance Study of Software AER-Based Convolutions on a Parallel Supercomputer
R.J. Montero-González, A. Morgado-Estévez, A. Linares-Barranco, B. Linares-Barranco, F. Pérez-Peña, J.A. Pérez-Carrasco and A. Jiménez-Fernández
Advances in Computational Intelligence, Lecture Notes in Computer Science, Vol 6691, pp 141-148, 2011
SPRINGER DOI: 10.1007/978-3-642-21501-8_18 ISBN: 978-3-642-21500-1 ISSN: 0302-9743

This chapter is based on the simulation of a convolution model for bio-inspired neuromorphic systems using the Address-Event-Representation (AER) philosophy and implemented in the supercomputer CRS of the University of Cadiz (UCA). In this work we improve the runtime of the simulation, by dividing an image into smaller parts before AER convolution and running each operation in a node of the cluster. This research involves a test cases design in which the optimal parameters are set to run the AER convolution in parallel processors. These cases consist on running the convolution taking an image divided in different number of parts, applying to each part a Sobel filter for edge detection, and based on the AER-TOOL simulator. Execution times are compared for all cases and the optimal configuration of the system is discussed. In general, CRS obtain better performances when the image is divided than for the whole image.

2012

Symbolic Pole/Zero Analysis
F. V. Fernández, C. Sánchez-López, R. Castro-López and E. Roca
Design of Analog Circuits through Symbolic Analysis, pp 287-304, 2012
BENTHAM DOI: 10.2174/978160805095611201010287 ISBN: 978-1-60805-425-1

Extraction of pole/zero expressions as a function of circuit parameters has traditionally been an essential tool for designers. In this Chapter, the main specific techniques for symbolic pole/zero extraction are described and their pros and cons are discussed. The application of the different techniques is illustrated with experimental results on practical circuits.

Symbolic Noise Analysis in Analog Circuits
C. Sanchez-López
Design of Analog Circuits through Symbolic Analysis, pp 265-285, 2012
BENTHAM DOI: 10.2174/978160805095611201010265 ISBN: 978-1-60805-425-1

An approach to the symbolic noise analysis on linear or linearized analog circuits at the transistor level of abstraction is presented. A brief exposition on the signal-path approach into analog circuits working in voltage-mode and current-mode, which are modeled

with nullors, is given. Therefore, symbolic noise parameters, such as: $\overline{V^2_{n,out}}$, $\overline{V^2_{n,in}}$, NF_v, $\overline{I^2_{n,out}}$, $\overline{I^2_{n,in}}$, and NF_i of analog circuits are computed, where all the noise sources associated to MOS transistors and passive elements are assumed to be uncorrelated. Two examples are introduced to illustrate the potentiality of the approach proposed. The first example is a voltage-mode analog circuit, where the signal-path is approached by using the nullator concept and its properties. On the contrary, in the second example, a current-mode analog circuit is considered where the signal-path is approached by using the norator concept along with its properties.

Modeling Active Devices with Nullors for Analog Signal Processing

C. Sanchez-López

Design of Analog Circuits through Symbolic Analysis, pp 61-82, 2012

BENTHAM DOI: 10.2174/978160805095611201010061 ISBN: 978-1-60805-425-1

This chapter describes the modeling of nullor-based active devices from the circuit level of abstraction. After a brief overview on the nullor concept and its properties, the modeling of active devices not only at the voltage-mode but also at the current-mode and the mixed-mode of operation from two-port and four-terminal network point of view is described in some detail. An important view that permeates the chapter is that the nullor-based models are not too complex and they can be introduced in CAD tools. Furthermore, parasitic elements can easily be added in order to predict their impact on the final response of the circuit. Several examples using nullor-based models illustrate its use to calculate fully-symbolic small-signal characteristics of linear or linearized analog circuits.

Approximation Techniques in Symbolic Circuit Analysis

F.V. Fernández, C. Sánchez-López, R. Castro-López and E. Roca

Design of Analog Circuits through Symbolic Analysis, Mourad Fakhfakh (Ed.), pp 173-201, 2012

BENTHAM DOI: 10.2174/978160805095611201010173 ISBN: 978-1-60805-425-1

Symbolic circuit analysis suffers from the exponential growth of expression complexity with circuit size. Therefore, either if the symbolic expressions are used for gaining insight into circuit operation or for repetitive computer-based evaluations, simplification becomes mandatory. This chapter reviews the different existing techniques for symbolic expression simplification, classifying them into three categories according to the step at which the simplification is performed: on the circuit equations, during the solution of the circuit equations or after the circuit equations have been solved. Pros and cons of each approach are discussed.

Applying Image Processing to In-Vitro Human Ovocytes Characterization

J. Aragón, A. González and A. Yúfera

Image Processing: Methods, Applications and Challenges, pp 87-103, 2012

NOVA SCIENCE PUBLISHERS ISBN: 978-1-62081-844-2

This book chapter presents an image processing tool developed to in-vitro human oocytes analysis required in fertilization processes to biological material classification. The application of the proposed tool allows a non-invasive method to define the quality of human oocytes before to be inseminated, enabling the possibility of selection the optimum one.

Specific segmentation algorithms have been developed to specific biomedical images for identifying the cytoplasm area. The oocyte status (normal, medium and highly stressed state) has been defined in terms of a set of parameters extracted from the cytoplasm image. This status quantification allows advising the biomedical staff during oocyte selection, involving by the first time a useful metrics. Experimental results proof that 83% of cases analyzed match with the expert evaluation.

Compact and Power Efficient MOS-NDR Muller C-Elements

J. Núñez-Martínez, M. J. Avedillo and J.M. Quintana-Toledo

Technological Innovation for Value Creation, IFIP Advances in Information and Communication Technology, vol. 372, pp 437-442, 2012

SPRINGER DOI: 10.1007/978-3-642-28255-3_48 ISBN: 978-3-642-28254-6 ISSN: 1868-4238

Recently there is a renewed interest in the development of transistor circuits which emulate the Negative Differential Resistance (NDR) exhibited by different emerging devices like Resonant Tunneling Diodes (RTDs). These MOS-NDR circuits easily allow the prototyping of design concepts and techniques developed for such NDR devices. The importation of those concepts into transistor technologies can result in circuit realizations which are advantageous for some functionalities and application fields. This paper describes a Muller C-element which illustrates this statement which is inspired in an RTD-based topology. The required RTD is implemented by means of the MOS-NDR device. A 4-input Muller C-element has been fabricated and experimentally validated. The proposed circuit compares favorably with respect to a well-known conventional gate realization.

Efficient multirate hybrid continuous-time/discrete-time cascade 2-2 sigma-delta modulators for wideband telecom

J. G. García-Sánchez and J.M. de la Rosa

VLSI-SoC: Advanced Research for Systems on Chip, IFIP Advances in Information and Communication Technology, Salvador Mir, Chi-Ying Tsui, Ricardo Reis and Oliver C. S. Choy (Eds.), vol. 379, pp 124-143, 2012

SPRINGER DOI: 10.1007/978-3-642-32770-4_8 ISBN: 978-3-642-32769-8

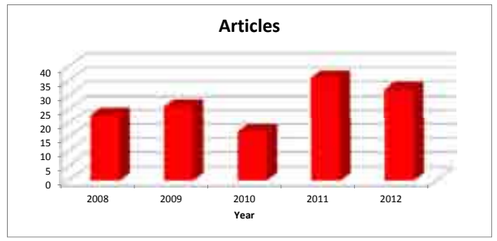
This chapter discusses the use of hybrid continuous-time/discrete-time fourth-order cascade two-stage 2-2 sigma-delta modulators for wideband low-power wireless applications. The modulator architecture under study is based on a new concept of multi-rate operation, in which the front-end stage -implemented using continuous-time (Gm-C) integrators- operates at a higher rate than the back-end (switched-capacitor) sta-

ge. This strategy benefits from the faster operation of continuous-time circuits while keeping power efficiency and high robustness against circuit element tolerances. A comparison with conventional multi-rate and single-rate (continuous-time) sigma-delta modulators is carried out based on the impact of main circuit-level error mechanisms, namely: mismatch, finite OTA dc gain and finite gain-bandwidth product. Closed-form analytical expressions are derived for the nonideal in-band noise power of the different architectures under study, demonstrating a good agreement with simulations and showing the benefits of the presented approach. Simulation results show that the proposed modulator is able to operate with a maximum sampling rate of up to 1GHz, digitizing signals with a 44-to-92dB peak signal-to-(noise+distortion) ratio within a programmable 5-to-60MHz bandwidth.

An all-inversion-region gm/ID based design methodology for radiofrequency blocks in CMOS nanometer technologies
R. Fiorelli, E. Peralías and F. Silveira
Wireless Radio-Frequency Standards and System Design: Advanced Techniques, pp 15-39, 2012
IGI GLOBAL DOI: 10.4018/978-1-4666-0083-6.ch002 ISBN: 9781466600836

This chapter presents a design optimization methodology for analog radiofrequency (RF) blocks based on the gm/ID technique and on the exploration of all-inversion regions (from weak inversion or sub-threshold to strong inversion or above threshold) of the MOS transistor in nanometer technologies. The use of semi-empirical models of MOS transistors and passive components, as inductors or capacitors, assures accurate designs, reducing time and efforts for transferring the initial block specifications to a compliant design. This methodology permits the generation of graphical maps to visualize the evolution of the circuit characteristics when sweeping both the inversion zone and the bias current, allowing reaching very good compromises between performance aspects of the circuit (e.g. noise and power consumption) for a set of initial specifications. In order to demonstrate the effectiveness of this methodology, it is applied in the design of two basic blocks of RF transceivers: low noise amplifiers (LNAs) and voltage controlled oscillators (VCOs), implemented in two different nanometer technologies and specified to be part of a 2.4 GHz transceiver. A possible design flow of each block is provided; resulting designs are implemented and verified both with simulations and measurements.

JOURNAL PAPERS



Evolution of number of journal papers contributed by IMSE during the period 2008-2012.

2011

Characterization and Modelling of Circular Piezoelectric Micro Speakers for Audio Acoustic Actuation
J. Mendoza-López, S. Sánchez-Solano and J.L. Huertas-Díaz
ISRN Mechanical Engineering, vol. 2012

Summarization and analysis of network traffic flow records
F.M. Pouzols, D.R. López and A. Barriga-Barros
Studies in Computational Intelligence, vol. 342, pp 147-190, 2011

Studies in Computational Intelligence: Preface
F.M. Pouzols, D.R. López, DR and A. Barriga Barros
Studies in Computational Intelligence, vol. 342, no. V-VIII, 2011

Neuromorphic silicon neuron circuits
G. Indiveri, B. Linares-Barranco, T.J. Hamilton, A. van Schaik, R. Etienne-Cummings, T. Delbruck, Shih-Chii Liu, P. Dudek, P. Häfliger, S. Renaud, J. Schemmel, G. Cauwenberghs, J. Arthur, K. Hynna11, F. Folowosele, S. Saighi, T. Serrano-Gotarredona, J. Wijekoon, Y. Wang1 and K. Boahen
Frontiers in Neuromorphic Engineering, vol. 5, pp 1-23, 2011

Modeling time series by means of fuzzy inference systems
F.M. Pouzols, D.R. López and A. Barriga
Studies in Computational Intelligence, vol. 342, pp 53-85, 2011

Internet science
F.M. Pouzols, D.R. López and A. Barriga-Barros
Studies in Computational Intelligence, vol. 342, pp 1-51, 2011

Inference systems for network traffic control
F.M. Pouzols, D.R. López and A. Barriga-Barros
Mining and Control of Network Traffic by Computational Intelligence. Studies in Computational Intelligence, vol. 342, pp 191-262, 2011

Diseño de bloques de convolución para procesado de imágenes con FPGA
L.M. Garcés-Socarrás, A.J. Cabrera-Sarmiento, S. Sánchez-Solano and P. Brox
Revista de Ingeniería Electrónica, Automática y Comunicaciones RIELAC, vol. XXXII 3/2011 pp 56-69, 2011

A 1.2V 10-bit 60-MS/s 23 mW CMOS pipeline ADC with 0.67 pJ/conversion-step and on-chip reference voltages generator
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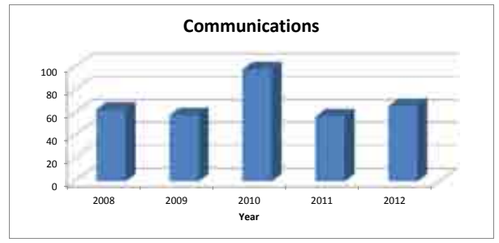

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J. Masuch and M. Delgado-Restituto
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A 55 µW programmable gain amplifier with constant bandwidth for a direct conversion receiver
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SPIE Microtechnologies for the New Millennium 2011

Design of a smart SiPM based on focal-plane processing elements for improved spatial resolution in PET
F. Pozas-Flores, R. Carmona-Galán, J. Fernández-Berni and A. Rodríguez-Vázquez
SPIE Microtechnologies for the New Millennium 2011

Focal-plane generation of multi-resolution and multi-scale image representation for low-power vision applications
J. Fernández-Berni, R. Carmona-Galán, L. Carranza-González, A. Zarandy and A. Rodríguez-Vázquez
SPIE Infrared Technology and Applications XXXVII, 2011

2012

Bifurcation Diagrams in MOS-NDR Frequency Divider Circuits
J. Nuñez-Martínez, M.J. Avedillo and J.M. Quintana-Toledo
19th IEEE International Conference on Electronics, Circuits, and Systems ICECS 2012

Two-phase MOBILE interconnection schemes for ultra-grain pipeline applications
J. Núñez-Martínez, M.J. Avedillo and J.M. Quintana-Toledo
Int. Workshop on Power and Timing Modeling, Optimization and Simulation PATMOS 2012

Systematic Generation of Performance Models of Reconfigurable Analog Circuits
M. Velasco-Jiménez, R. Castro-López, E. Roca and F.V. Fernández
Int. Conf. on Synthesis, Modeling, Analysis and Simulation Methods and Applications to Circuit Design SMACD 2012

Surrogate models of Pareto-optimal planar inductors
M. Kotti, R. González-Echevarría, E. Roca, R. Castro-López, F.V. Fernández, M. Fakhfakh, J. Sieiro and J.M. López-Villegas
Int. Conf. on Synthesis, Modeling, Analysis and Simulation Methods and Applications to Circuit Design SMACD 2012

Semi-empirical model of MOST and passive devices focused on narrowband RF blocks
R. Fiorelli, F. Silveira, A. Rueda and E. Peralías
XXVII Conference on Design of Circuits and Integrated Systems DCIS 2012

Self-Biased Input Common-Mode Generation for Improving Dynamic Range and Yield in Inverter-Based Filters
A.J. Ginés, A. Villegas, A. Rueda and E. Peralías
IEEE International Conference on Electronics, Circuits, and Systems ICECS 2012

Reducing bit flipping problems in SRAM physical unclonable functions for chip identification
S. Eiroa, J. Castro, M.C. Martínez-Rodríguez, E. Tena, P. Brox and I. Baturone
IEEE International Conference on Electronics, Circuits, and Systems ICECS 2012

Real-Time Remote Reporting of Motion Analysis with Wi-Flip
J. Fernández-Berni, R. Carmona-Galán and A. Rodríguez-Vázquez
13th Int. Workshop on Cellular Nanoscale Networks and their Applications CNNA 2012

Real-Time FPGA Connected Component Labeling System
E. Calvo-Gallego, A. Cabrera-Aldaya, P. Brox and S. Sánchez-Solano
IEEE Int. Conf. on Electronics, Circuits, and Systems ICECS 2012

OWLS: A Mixed-Signal Asic for Optical Wire-Less Links in Space Instruments
J. Ramos-Martos, A. Arias-Drake, A. Ragel-Morales, J. Ceballos-Cáceres, J.M. Mora-Gutiérrez, B. Piñero-García, M. Muñoz-Díaz, M.A. Lagos-Florido, S. Sordo-Ibáñez, S. Espejo-Meana, I. Arruego, J. Martínez-Oter and M.T. Álvarez
4th International Workshop on Analogue and Mixed Signal Integrated Circuits For Space Applications AMICSA 2012

New approaches to bridge the design gap of analog and RF circuits
F.V. Fernández, E. Roca and R. Castro-López
Int. Conf. on Analog VLSI Circuits AVIC 2012

Model-based Design for Selecting Fingerprint Recognition Algorithms for Embedded Systems
R. Arjona and I. Baturone
IEEE International Conference on Electronics, Circuits, and Systems ICECS 2012

Low-Power Vision Chips based on Focal-Plane Feature Extraction for Visually-Assisted Autonomous Navigation
R. Carmona-Galán
Workshop on Smart Cameras for robotic applications, IEEE/RSJ Int. Conf. on Intelligent Robots and Systems IROS 2012

Low power implementation of Trivium stream cipher
J.M. Mora-Gutiérrez, C.J. Jiménez-Fernández and Valencia-Barrero
22nd International Workshop PATMOS 2012

Live Demonstration: On the distance estimation of moving targets with a Stereo-Vision AER system
M. Domínguez-Morales, A. Jiménez-Fernández, R. Paz-Vicente, G. Jiménez and A. Linares Barranco
IEEE International Symposium on Circuits and Systems ISCAS 2012

LDS based tools to ease template construction
A. Unutulmaz, G. Dundar and F.V. Fernández-Fernández
Int. Conf. on Synthesis, Modeling, Analysis and Simulation Methods and Applications to Circuit Design SMACD 2012

Implementación sobre FPGA de un algoritmo de etiquetado en tiempo real
E. Calvo-Gallego, P. Brox and S. Sánchez-Solano
Jornadas de Computación Reconfigurable y Aplicaciones JCRA 2012

GMR technology: a real candidate for monolithically integrated off-line IC current sensing
C. Reig, M.D. Cubells, A. Cano, J. Sanchís, D. Gilabert, J. Madrenas, A. Yúfera, E. Figueras, S. Cardoso and P.P. Freitas
International Conference on Analog VLSI Circuits, 2012

Frame-free event-based vision sensors and processors: building smart modular mixed-signal brain-like architectures
T. Serrano-Gotarredona and B. Linares-Barranco
International Conference on Analog VLSI Circuits, 2012

Evaluation of the AMS 0.35µm CMOS Technology for use in Space Applications
J. Ramos-Martos, A. Arias-Drake, A. Ragel-Morales, J. Ceballos-Cáceres, J.M. Mora-Gutiérrez, B. Piñero-García, M. Muñoz-Díaz, M.A. Lagos-Florido, S. Sordo-Ibáñez and S. Espejo-Meana
4th International Workshop on Analogue and Mixed Signal Integrated Circuits For Space Applications AMICSA 2012

Electromechanical performance comparison for different CMUT Element geometries
J. Mendoza-López and C. Sánchez-López
International Conference on Synthesis, Modeling, Analysis and Simulation Methods and Applications to Circuit Design SMACD 2012

Effect of Circuit Errors and Hybrid Continuous-Time/Discrete-Time Sigma-Delta Modulators
J.G. García-Sánchez and J.M. de la Rosa
Design of Circuits and Integrated Circuits and Integrated Systems Conference DCIS 2012

Diseño e implementación de multiplicadores de Montgomery en FPGAs
G. Sassaw-Teshome, C.J. Jiménez-Fernández and M. Valencia-Barrero
Taller sobre Hardware Reconfigurable THR 2012

Design of adaptive nano/CMOS neural architectures
T. Serrano Gotarredona and B. Linares Barranco
19th International conference on electronics, circuits and systems ICECS 2012

CMOS SPADs Selection, Modeling and Characterization Towards Image Sensors Implementation
M. Moreno-García, O. Guerra, R. del Río, B. Pérez-Verdú and A. Rodríguez-Vázquez
19th International Conference on Electronics, Circuits, and Systems ICECS 2012

ASIC-in-the-loop methodology for verification of piecewise affine controllers
M. Martínez-Rodríguez, P. Brox, J. Castro, E. Tena, A. Acosta and I. Baturone
IEEE International Conference on Electronics, Circuits, and Systems ICECS 2012

An Impedance-Based Microscopy for Cell-Culture Imaging Using Microelectrode Sensors
A. Olmo, G. Huertas and A. Yúfera
Conference on Design of Circuits and Integrated Systems DCIS 2012

An Automated Layout-Aware Design Flow
A. Toro-Frías, R. Castro-López, E. Roca and F.V. Fernández
International Conference on Synthesis, Modeling, Analysis and Simulation Methods and Applications to Circuit Design SMACD 2012

An all-inversion-region MOST design methodology applied to a ratioless differential LC-VCO
R. Fiorelli, F. Silveira and E. Peralías
8th Conference on Ph.D. Research in Microelectronics and Electronics PRIME 2012

A Microscopy Technique based on Bio-impedance Sensors
A. Yúfera, G. Huertas and A. Olmo
26th European Conference on Solid-State Transducers EUROSENSOR 2012

A fully automated design flow for planar inductors
R. González-Echevarría, R. Castro-López, E. Roca, F.V. Fernández, J.M. López-Villegas and J. Sieiro
International Conference on Synthesis, Modeling, Analysis and Simulation Methods and Applications to Circuit Design SMACD 2012

A CMOS-3D Reconfigurable Architecture with In-pixel Processing for Feature Detectors
M. Suárez, V.M. Brea, F. Pardo, R. Carmona-Galán and A. Rodríguez-Vázquez
IEEE International 3D System Integration Conference 3DIC 2012

A 0.2-to-2MHz BW, 50-to-86dB SNDR, 16-to-22mW Flexible 4th-Order SD Modulator with DC-to-44MHz Tunable Center Frequency in 1.2-V 90-nm CMOS
S. Asghar, R. del Río and J.M. de la Rosa
20th IFIP/IEEE International Conference on Very Large Scale Integration, 2012

A 0.2pJ/conversion-step 6-bit 200MHz flash ADC with redundancy
H. Darwish, G. Léger and A. Rueda
Conference on Design of Circuits and Integrated Systems DCIS 2012

Control and Acquisition System for a High Dynamic Range CMOS Image Sensor
S. Vargas Sierra, G. Liñán-Cembrano and A. Rodríguez-Vázquez
IEEE International Conference on Electronics, Circuits, and Systems ICECS 2012

High-speed global shutter CMOS machine vision sensor with high dynamic range image acquisition and embedded intelligence
F. Jiménez-Garrido, J. Fernández-Pérez, C. Utrera, J.M. Muñoz, M.D. Pardo, A. Giulietti, R. Domínguez-Castro, F. Medeiro and A. Rodríguez-Vázquez
Sensors, Cameras, and Systems for Industrial and Scientific Applications XIII IMAGING 2012

Design of a smart camera SoC in a 3D-IC technology
R. Carmona-Galán, J. Fernández-Berni, S. Vargas-Sierra, G. Liñán-Cembrano, A. Rodríguez-Vázquez, V. Brea-Sánchez, M. Suárez-Cambre and D. Cabello-Ferrer
Workshop on Architecture of Smart Camera, 2012

Multi-condition alternate test of analog, mixed-signal, and RF systems
M.J. Barragán-Asián, G. Léger and J.L. Huertas-Díaz
13th IEEE Latin American Test Workshop LATW 2012

Un algoritmo en tiempo real para etiquetado de componentes conectados en imágenes
E. Calvo-Gallego, P. Brox and S. Sánchez-Solano
Iberchip XVIII Workshop IWS 2012

Self-adaptive lower confidence bound: A new general and effective prescreening method for Gaussian process surrogate model assisted evolutionary algorithms
B. Liu, Q. Zhang, F.V. Fernández and G. Gielen
IEEE Congress on Evolutionary Computation CEC 2012

A 1.1mW-Rx, 5.9mW-Tx Bluettoth low energy transceiver with -81.4 dBm sensitivity
J. Masuch and M. Delgado-Restituto
International Solid-State Circuits Conference ISSCC 2012

Prácticas de laboratorio de Linux empotrado sobre placas de desarrollo XUPV2P
A. García-Moya and A. Barriga-Barros
X Congreso de Tecnologías Aplicadas a la Enseñanza de la Electrónica TAEE 2012

Implementación sobre FPGA de un sistema de detección de caras basado en LEON3
L. Acasandrei and A. Barriga-Barrios
Iberchip XVIII Workshop IWS 2012

FPGA implementation of an embedded face detection system based on LEON3
L. Acasandrei and A. Barriga-Barrios
International Conference on Image Processing, Computer Vision & Pattern Recognition IPCV 2012

Bifurcation Diagrams in MOS-NDR Frequency Divider Circuits
J. Núñez-Martínez, M.J. Avedillo and J.M. Quintana-Toledo
Iberchip XVIII Workshop IWS 2012

A real-time event-driven neuromorphic system for goal-directed attentional selection
F. Galluppi, K. Brohan, S. Davidson, T. Serrano-Gotarredona, J.A. Pérez-Carrasco, B. Linares-Barranco and S. Furber
19th International Conference on Neural Information Processing ICONIP 2012

XFSML: An XML-based modeling language for fuzzy systems
F.J. Moreno-Velo, A. Barriga, S. Sánchez-Solano and I. Baturone
IEEE International Conference on Fuzzy Systems FUZZ-IEEE 2012

Sistema empotrado de reconocimiento de voz sobre FPGA
J. Balosa, F.J. Crespo and A. Barriga
Iberchip XVIII Workshop IWS 2012

Reflexión sobre los contenidos que cubran la competencia "Conocimientos de los fundamentos de la Electrónica" en los títulos de Grado de Ingeniería Industrial
C.J. Jiménez-Fernández, G. Miró, C. León and A. López
X Congreso de Tecnologías Aplicadas a la Enseñanza de la Electrónica TAEE 2012

Síntesis automática de sistemas difusos mediante xfuzzy
S. Sánchez-Solano and M. Brox
XVI Congreso Español sobre Tecnologías y Lógica Fuzzy ESTYLF 2012

Hybrid continuous-time/discrete-time circuit techniques for the efficient implementation of wideband Sigma-Delta ADCs
J.G. García-Sánchez and J.M. de la Rosa
55th IEEE Midwest Symposium on Circuits and Systems MWSCAS 2012

Analysis of steady-state common-mode response in differential LC-VCOs
R. Doldán, A.J. Ginés, E. Peralías and A. Rueda
IEEE International Symposium on Circuits and Systems ISCAS 2012

An RF-to-DC energy harvester for co-integration in a low-power 2.4 GHz transceiver front-tend
J. Masuch, M. Delgado-Restituto, D. Milosevic and P. Baltus
IEEE International Symposium on Circuits and Systems ISCAS 2012

A power-scalable concurrent cascade 2-2-2 SC Δ modulator for Software Defined Radio
A. Morgado, J.G. García, S. Asghar, L.I. Guerrero, R. del Río and J.M. de la Rosa
IEEE International Symposium on Circuits and Systems ISCAS 2012

A 148dB focal-plane tone-mapping QCIF imager
S. Vargas-Sierra, G. Liñán-Cembrano and A. Rodríguez-Vázquez
IEEE International Symposium on Circuits and Systems ISCAS 2012

A preamplifier for the front-end readout system of particles tracking in secondary electron detectors
A. Garzón-Camacho, B. Fernandez, M.A.G. Alvarez, J. Ceballos and J.M de la Rosa
IEEE International Symposium on Circuits and Systems ISCAS 2012

Behavioral modeling techniques for teaching communication circuits and systems
J.M. de la Rosa
IEEE International Symposium on Circuits and Systems ISCAS 2012

Power-efficient focal-plane image representation for extraction of enriched Viola-Jones features
J. Fernández-Berni, L. Acasandrei, R. Carmona-Galán, A. Barriga-Barrios and A. Rodríguez-Vázquez
IEEE International Symposium on Circuits and Systems ISCAS 2012

In-pixel generation of gaussian pyramid images by block reusing in 3D-CMOS
M. Suárez, V.M. Brea, D. Cabello, R. Carmona-Galán and A. Rodríguez-Vázquez
IEEE International Symposium on Circuits and Systems ISCAS 2012

OBT for settling error test of sampled-data systems using signal-dependent clocking
M.J. Barragán-Asián, G. Léger and J.L. Huertas-Díaz
17th IEEE European Test Symposium ETS 2012

Reflections on content to be included in the "Basic Electronics" proficiency of Industrial Engineering degrees
C.J. Jiménez-Fernández, G. Miró, C. León and A. López
X Congreso de Tecnologías Aplicadas a la Enseñanza de la Electrónica TAEE 2012

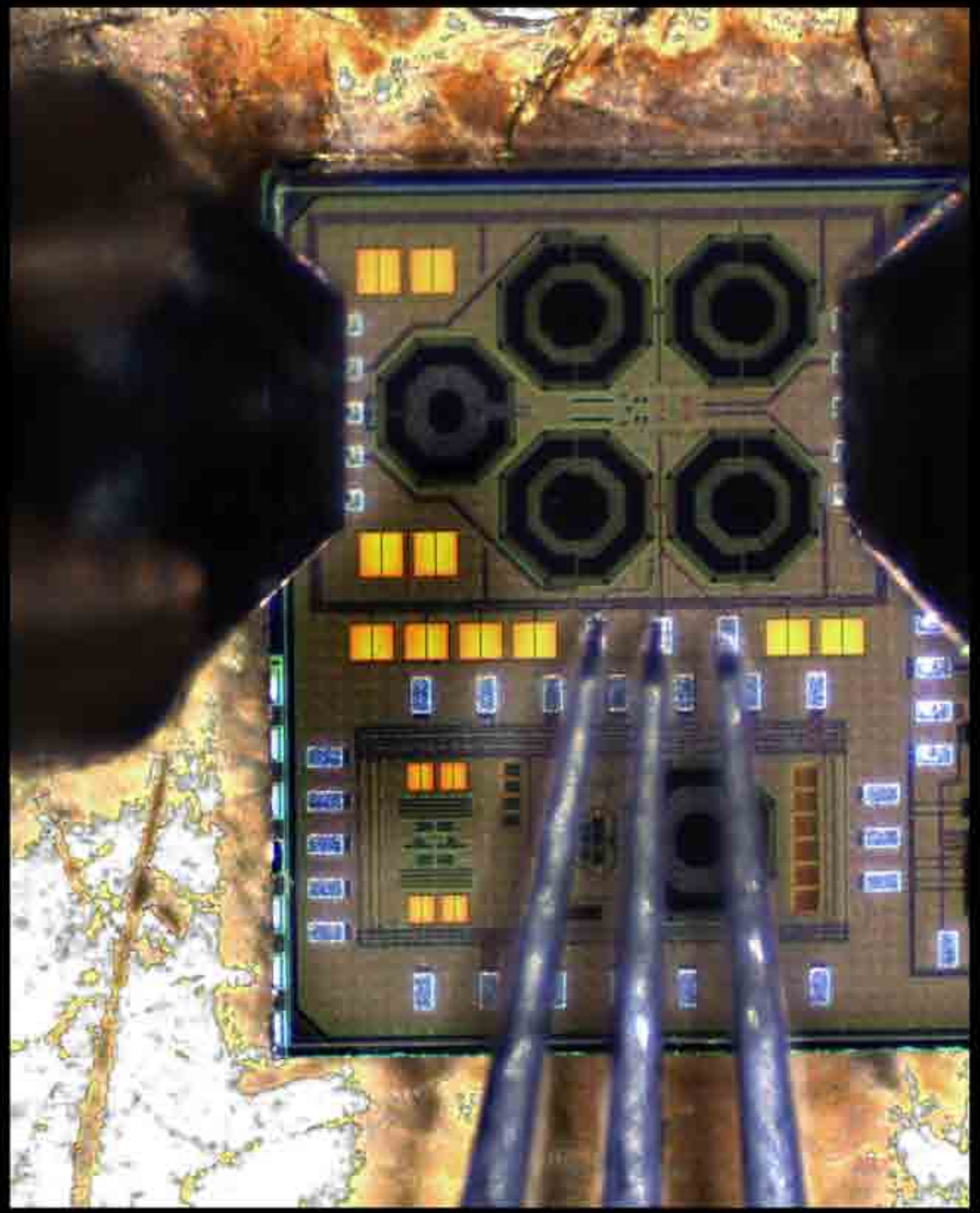
Using behavioral modeling and simulation for learning communication circuits and systems
J.M. de la Rosa
IEEE Global Engineering Education Conference EDUCON 2012

A teamwork-based education strategy for teaching lab of analog integrated circuits design
J.M. de la Rosa
IEEE Global Engineering Education Conference EDUCON 2012

Using nanoHUB.org for teaching and learning nanoelectronic devices in materials engineering
J.M. de la Rosa
IEEE Global Engineering Education Conference EDUCON 2012

Efficient Hybrid Continuous-Time/Discrete-Time Sigma Delta Modulators for Broadband Wireless Telecom Systems
J.G. García-Sánchez and J.M. de la Rosa
3rd Doctoral Conference on Computing, Electrical and Industrial Systems DOCEIS 2012

A 176x144 148dB adaptive tone-mapping imager
S. Vargas-Sierra, G. Liñán-Cembrano and A. Rodríguez-Vázquez
Sensors, Cameras, and Systems for Industrial and Scientific Applications XIII IMAGING 2012



OTHER CONTRIBUTIONS

SPECIAL CONTRIBUTIONS TO SCIENTIFIC JOURNALS

Prof. Ángel Rodríguez-Vazquez was *Guest Editor* of the special issue on the "**36th European Solid-State Circuits Conference**" of the IEEE Journal of Solid-State Circuits, July 2011.

Dr. Manuel Delgado-Restituto is *Deputy-Editor-in-Chief* of the "**IEEE Journal on Emerging and Selected Topics in Circuits and Systems**" since 2011 and associate Editor of the "IEEE Transaction on Circuits and Systems - I: Regular Papers" in 2011.

Dr. José Manuel de la Rosa Utrera was *Guest Editor* of the special issue on the **2012 IEEE International Conference on Electronics, Circuits and Systems** (ICECS 2012) of the Analog Integrated Circuits and Signal Processing Journal.

Prof. Francisco V. Fernández Fernández was *Editor-in-Chief* and *Subject Editor* of Analog and Mixed-Signal of "**Integration, the VLSI Journal**" during 2011-12 and was also *Guest Editor* of the special issue on the **2012 IEEE Int. Conf. on Synthesis, Modeling, Analysis and Simulation Methods and Applications to Circuit Design** (SMACD 2012) of the Analog Integrated Circuits and Signal Processing Journal.

Prof. Bernabé Linares Barranco was *Associated Editor* of "**Frontiers on Neuromorphic Engineering**" during years 2011 and 2012.

Dr. Teresa Serrano-Gotarredona was *Associated Editor* of "**Public Library of Science**" (Plos ONE) and the **IEEE Transactions on Circuits and Systems I** during 2011 and 2012.

PLENARY AND INVITED TALKS

"Implementation of Neuromophic Architectures with Memristors" by *Prof. Bernabé Linares Barranco* at the 2011 CapoCaccia Cognitive Neuromorphic Engineering Workshop, Capo Caccia, Sardinia, Italy, April-May 2011.

"How to Compute with Memristors: Dedicated Bio-Inspired Architectures" by *Prof. Bernabé Linares Barranco* at the 2011 The European Future Technologies Conference and Exhibition (FET 2011). Budapest, Hungary. May 2011

"On Architectures for CMOS Intelligent Imagers and Vision Systems" by *Prof. Ángel Rodríguez-Vázquez* at the 10th International Symposium on Signals, Circuits and Systems (ISSCS 2011), Iasi, Romania, Jun 30 - Jul 1, 2011.

"Low-Power Mixed-Signal Circuits and Architectures for Detection and Preprocessing of 2-D Sensory Signals" by *Prof. Ángel Rodríguez-Vázquez* at the 5th Int. Workshop on Seizure Prediction (IWSP). Dresden, Germany, September 19-23, 2011.

"CMOS Smart Imagers and Vision Systems: Bridging 3-D to Scene" by *Prof. Ángel Rodríguez-Vázquez* at the 2011 Int. Technical Exhibition on Image Technology and Equipment. Yokohama, Japan, December 7-9, 2011.

"Design of a smart camera system on a single chip in a 3D integrated circuit technology" by *Dr. Ricardo Carmona* at the Workshop on Architecture of Smart Camera (WASC 2012), Université Blaise Pascal, Clermont-Ferrand, April 2012.

"Storage and Memory in Neuromorphic Systems: Can Memristors Help?" by *Prof. Bernabé Linares Barranco* at the 2012 Capo-Caccia Cognitive Neuromorphic Engineering Workshop. Capo Caccia, Sardinia, Italy, April-May 2012.

"Smart CMOS Image Sensors for 2-D and 3-D Capture and Processing: Pixels, Circuits, Architectures and Practical Design Guidelines" by *Dr. Ricardo Carmona* (in colaboration with *Prof. Á. Rodríguez-Vázquez*) at the IEEE International Symposium on Circuits and Systems (ISCAS 2012) Tutorials, Seoul, Korea, May 2012.

"Event-driven Dynamic Vision Sensors" by *Prof. Bernabé Linares Barranco* at the 2012 Telluride Neuromorphic Cognition Engineering Workshop, Telluride, Colorado, USA. July 2012

"Progress on CMOS Smart Imagers and Vision Systems" by *Dr. Ricardo Carmona* at the Int. Workshop on Cellular Nanoscale Networks and their Applications (CNNA 2012), Politecnico di Torino, Italy, August 2012.

"Neuromorphic Frame Free Vision. High Speed Sensing and Object Recognition" by *Prof. Bernabé Linares Barranco* at the 2nd FACETS-ITN Student conference: Applications of Neuromorphic Hardware. Barcelona, Spain. September 2012

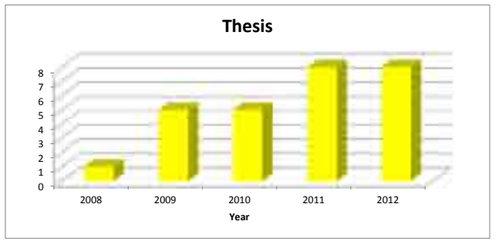
"Low-Power Vision Chips based on Focal-Plane Feature Extraction for Visually-Assisted Autonomous Navigation" by *Dr. Ricardo Carmona* at the Workshop on Smart Cameras for robotic applications, IEEE/RSJ Int. Conf. on Intelligent Robots and Systems (IROS 2012), Vilamoura, Algarve, Portugal, October 2012.

"New approaches to bridge the design gap of analog and RF circuits" by *Prof. Francisco Fernández* at the "International Conferenc. on Analog VLSI Circuits (AVIC)". Valencia, Spain, October 2012.

"Efficient Analog CMOS Circuits for the Next Generation Software-Defined-Radio Mobile Systems: Trends, Challenges and Solutions" by *Dr. José Manuel de la Rosa Utrera* at the 2nd International Symposium on Innovation and Technology", November 2012.

"Learning memristors in event-driven neuromorphic vision systems" by *Prof. Bernabé Linares Barranco* at the MemCo Workshop "Memristors for Computing". Fréjus, France, November 2012

THESIS



Evolution of number of doctoral thesis defended at IMSE during the period 2008-2012.

2011

Diseño lógico de circuitos digitales usando dispositivos con característica NDR
J. Núñez
Date of defense: 04/02/2011
UNIVERSIDAD DE SEVILLA, IMSE-CNM

Reconfigurable sigma-delta modulators for multi-standard wireless communications in nanometer CMOS technologies
A. Morgado
Date of defense: 08/02/2011
UNIVERSIDAD DE SEVILLA, IMSE-CNM

Herramienta de simulación para construir y analizar sistemas complejos y jerárquicamente estructurados basados en AER que implementan procesado de la información visual
J.A Pérez-Carrasco
Date of defense: 11/03/2011
UNIVERSIDAD DE SEVILLA, IMSE-CNM

Power-efficient VLSI implementation of vision hardware on wireless sensor network nodes
J. Fernández-Berni
Date of defense: 20/06/2011
UNIVERSIDAD DE SEVILLA, IMSE-CNM

Desarrollo y aplicaciones de técnicas de control de corriente de alimentación en circuitos integrados digitales CMOS
J. Castro-Ramírez
Date of defense: 13/07/2011
UNIVERSIDAD DE SEVILLA, IMSE-CNM

Diseño de microprocesadores de propósito específico y sistemas de desarrollo y testado para circuitos integrados de visión artificial
L. Carranza-González
Date of defense: 21/10/2011
UNIVERSIDAD DE SEVILLA, IMSE-CNM

Circuitos aritméticos CMOS nanométricos para aplicaciones criptográficas
G. Sassaw
Date of defense: 27/10/2011
UNIVERSIDAD DE SEVILLA, IMSE-CNM

Modular and scalable implementation of AER neuromorphic systems
C. Zamarreño-Ramos
Date of defense: 19/12/2011
UNIVERSIDAD DE SEVILLA, IMSE-CNM

2012

An all-inversion-region gm/ID based design methodology for radiofrequency blocks in CMOS nanometer technologies
R. Fiorelli-Martegani
Date of defense: 27/01/2012
UNIVERSIDAD DE SEVILLA, IMSE-CNM

Estimación de la actividad de conmutación en circuitos digitales CMOS VLSI
M.C. Baena-Oliva
Date of defense: 09/03/2012
UNIVERSIDAD DE SEVILLA, IMSE-CNM

A contribution to the design and implementation of CMOS RF and mixed-signal front-ends for the IEEE 802.15.4 standartd (ZigBee) in the 2.4Gz band
J.A. Villegas-Calvo
Date of defense: 13/04/2012
UNIVERSIDAD DE SEVILLA, IMSE-CNM

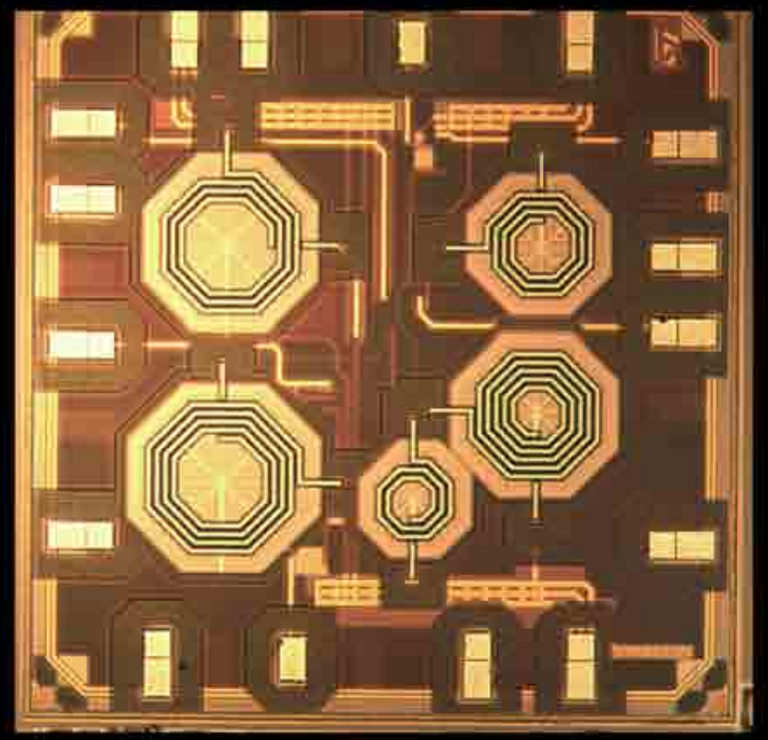
Una contribución al diseño de moduladores sigma-delta en cascada realizados mediante técnicas de circuito en tiempo continuo
R. Tortosa-Navas
Date of defense: 28/06/2012
UNIVERSIDAD DE SEVILLA, IMSE-CNM

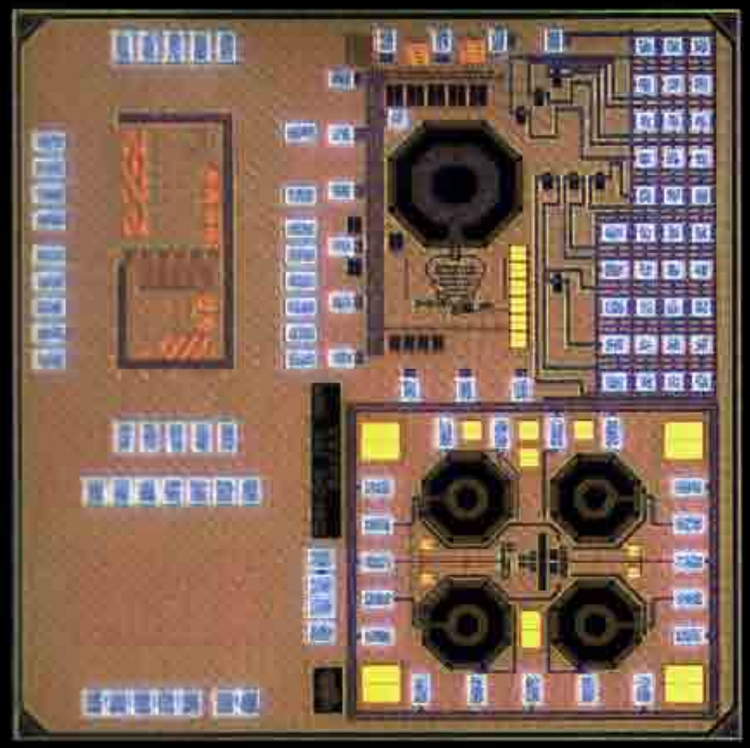
Diseño de un modulador sigma-delta híbrido en configuración cascada con múltiples frecuencias de muestreo para aplicaciones 4G
L.I.V. Guerrero-Linares
Date of defense: 02/08/2012
UNIVERSIDAD DE SEVILLA, IMSE-CNM

Propuesta de arquitectura y circuitos para la mejora del rango dinámico de sistemas de visión en un chip diseñados en tecnologías CMOS profundamente submicrométricas
S. Vargas-Sierra
Date of defense: 11/09/2012
UNIVERSIDAD DE SEVILLA, IMSE-CNM

Ultra low power transceiver for wireless body area networks
J. Masuch
Date of defense: 19/10/2012
UNIVERSIDAD DE SEVILLA, IMSE-CNM

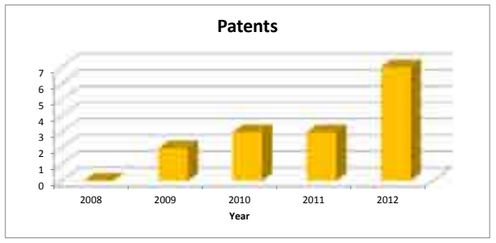
Aceleración del algoritmo de detección de rostros de Viola-Jones mediante su implementación híbrida flexible sobre hardware reconfigurable
E. del Toro-Hernández
Date of defense: 29/11/2012
Instituto Superior Politécnico José Antonio Echeverría (ISPJAE)
La Habana, Cuba.





PATENTS

Specific patent-protected technology produced at the IMSE-CNM during the course of research activities is listed below. Collaboration between IMSE-CNM and interested companies may be established either through development agreements with a licensing options, or through licenses for commercial exploitation.

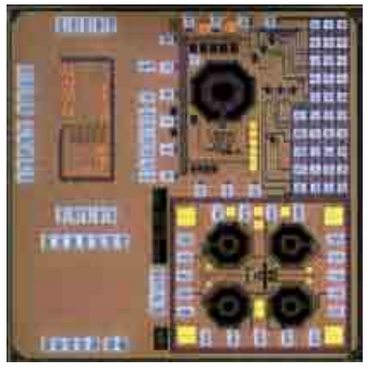


Evolution of number of patents obtained by IMSE during the period 2008-2012.

2011

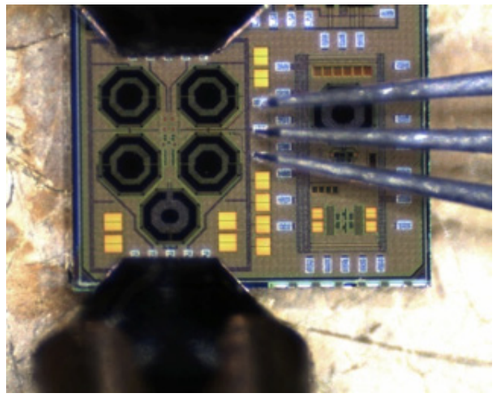
Magneto-electric connection for loopback applications in integrated transceivers
Inventors: Manuel J. Barragán Asián; José L. Huertas Díaz; Eduardo Peralías Macías
Applicants: CSIC, Universidad de Sevilla
Priority number: 201132116
Priority date: 28.12.2011

Improved loopback test method for integrated RF transceivers. The improvement is based on the use of a novel magneto-electric sensor. The sensor is composed of a magneto-electric transducer and a signal conditioning module, and enables a connection between the transmitter and receiver circuits comprising the integrated RF transceiver to test. The presented sensor implements test strategies that require no modifications to the transceiver and can be performed during normal system operation.



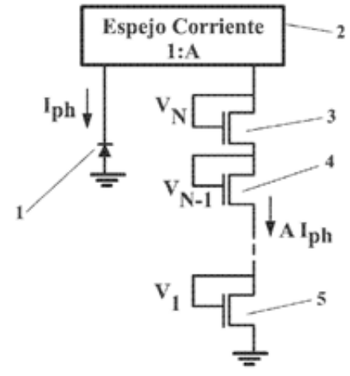
Method and system for testing integrated radio-frequency circuits at the wafer level and the use thereof
Inventors: José L. Huertas Díaz; Manuel J. Barragán Asián
Applicants: CSIC, Universidad de Sevilla
Priority number: 201131109
Priority date: 30.06.2011

The main objective of this invention is to provide a system and a reliable and rapid method for rejecting defective integrated transceivers at the wafer level by establishing wireless links between different circuits in the wafer such that the signals needed to test a particular transceiver are provided or read by another one of the transceivers in the same wafer. For this purpose, the system uses a low-frequency digital test apparatus which at least comprises two test needles for sending, receiving and comparing test data sequences which are interchanged between the test apparatus and the integrated circuits in the wafer.



Low-mismatch and low-consumption transimpedance gain circuit for temporally differentiating photo-sensing systems in dynamic vision sensors
Inventors: Teresa Serrano Gotarredona; Bernabé Linares Barranco
Applicants: CSIC
Priority number: 201130862
Priority date: 26.05.2011

The invention relates to a low-mismatch and low-consumption transimpedance gain circuit for temporally differentiating photo-sensing systems in dynamic vision sensors, which uses at least one photodiode and at least two in-series transistors, each of the transistors being connected in diode configuration and being positioned at the output of the photodiode. The output current from the photodiode flows through the drain-source channels of the transistors and the source of the last transistor in series is connected to a voltage selected from earth voltage, a constant voltage or a controlled voltage.



Improved dynamic vision sensor (DVS) device
Inventors: Teresa Serrano Gotarredona; Bernabé Linares Barranco
Applicants: CSIC
Priority number: 201231921
Priority date: 11.12.2012

DVS device with greater contrast sensitivity, lower production cost, lower power consumption requirements, and, in general, better performance than current DVS ones. System improvement is due to the incorporation of a transimpedance circuit for low power and low mismatch which provides amplification of the voltage coming from the photo current conversion. Best performance of the device makes it especially useful in applications which require low power, high speed, and complex information processing such as robotics, automated driving of vehicles, aircraft and surveillance among others.

Image processor for key points detection at the focal plane
Inventors: Ricardo Carmona Galán; Jorge Fernández Berni; Ángel Rodríguez Vázquez
Applicants: CSIC, Universidad de Sevilla
Priority number: 201201011
Priority date: 08.10.2012

Hardware device for detecting local extrema of an image. Processing is done at the focal plane by using mixed-signal circuitry (analog and digital). To this end, and by comparison of the neighboring pixel voltages representing the value of each pixel, the device determines the existence of local maxima and minima prior to downloading the image from the sensor. The resulting time and energy savings enables develop autonomous vision devices with low power consumption.

Wireless battery-free biomedical signal monitoring patch
Inventors: Jens Masuch; Alberto Rodríguez Pérez; Jesús Ruiz Amaya; Manuel Delgado Restituto; José A. Rodríguez Rodríguez
Applicants: CSIC
Priority number: 201231201
Priority date: 26.07.2012

System for the remote monitoring of physiological patterns, such as temperature and heart rate, without decreasing the mobility or comfort of the patient. The system comprises a reader instrument, for enabling the measure procedure and processing the received information; and patch transponders, singled out with individual identifiers, for capturing and wirelessly transmitting sensory data. The system, based on passive RFID technology combined with transmitted time reference strategies, does not require tags to be supplied from primary batteries, exhibits a wireless coverage in the order of meters and offers the ability to measure different physical quantities simultaneously.

Universal controller and virtual sensor
Inventors: Antonio Acosta; Iluminada Baturone; Javier Castro; Carlos Jesús Jiménez; Piedad Brox; Macarena C. Martínez Rodríguez.
Applicants: CSIC, Universidad de Sevilla
Priority number: 201200608
Priority date: 04.06.2012

A method to provide the generation of digital circuits that implement multivariable Piece-Wise Affine (PWA) functions without approximations. These circuits offer a high performance in terms of area, speed, and power. The method presents two additional features: programmability and re-configurability. Both characteristics allow the implementation of several functions in the same integrated circuit, generating devices that could integrate the requirements of any controller or virtual sensor easily.

Instantaneous synapses to pulse-based neural network dynamic conversor
Inventors: Teresa Serrano Gotarredona; Bernabé Linares Barranco
Applicants: CSIC
Priority number: 201230702
Priority date: 10.05.2012

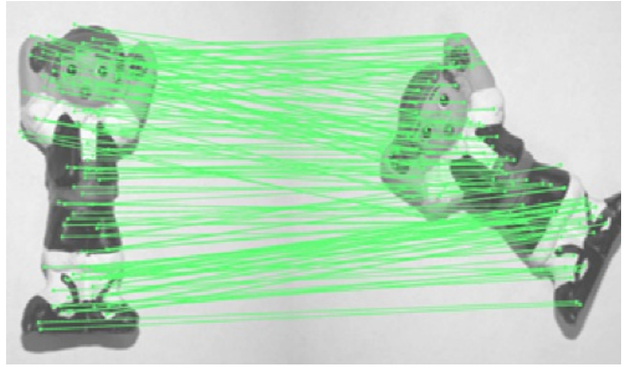
The proposed system allows the pulse-based processing with dynamic integration synapses using simple neural integrated circuits as the instantaneous integration ones. The system is based on the introduction of an event planner block that separates the pulses received by the neurons. That way, the pulse contribution is not instantaneous, avoiding neurons from taking wrong early activation decisions.

Image enhancement processor based on edge detection and anisotropic diffusion
Inventors: Ricardo Carmona Galán; Jorge Fernández Berni; Ángel Rodríguez Vázquez
Applicants: CSIC, Universidad de Sevilla
Priority number: 201200474
Priority date: 03.05.2012

Hardware device that enables, using mixed-signal circuitry, image improvement by means of edge detection and smoothing of homogeneous areas. In order to do this, each pixel is represented by a voltage value proportional to the light intensity at that point and subsequently compared with the voltage values of neighboring pixels. The elementary in-pixel circuits have low power consumption. This enables developing power-efficient artificial vision systems with applications in robotics, surveillance and navigation aids among others.

3D-Image processor for feature detection
Inventors: Ricardo Carmona Galán; Jorge Fernández Berni; Ángel Rodríguez Vázquez
Applicants: CSIC, Universidad de Sevilla, Universidad de Santiago de Compostela
Priority number: 201200090
Priority date: 01.02.2012

Hardware device that enables integration of all the elements of an artificial vision system into a single chip. The implementation of the chip into a vertical integration processing architecture, also known as 3D CMOS, enables in real time processing while maintaining a practical image size. This system represents an alternative to the high computational cost of already known image processing techniques. Autonomous systems based on this chip are useful in robotics, medical and aeronautics applications among others.



CONFERENCE ORGANIZATION

SMACD 2012

International Conference on Synthesis, Modeling, Analysis and Simulation Methods and Applications to Circuit Design

http://www2.imse-cnm.csic.es/~smacd2012/SMACD_2012/HOME.html

The "International Conference on Synthesis, Modeling, Analysis and Simulation Methods and Applications to Circuit Design (SMACD2012)" was held on 19-21 September 2012 in Seville, as a forum dedicated to Design Methods and Tools for Analog, Mixed-signal, RF (AMS/RF) and multi-domain (MEMs, nanoelectronic, optoelectronic, biological, etc.) integrated circuits and systems.

SMACD2012 was organized by the Instituto de Microelectrónica de Sevilla (IMSE-CNM) and the Universidad de Sevilla. The General Chair of this conference was Prof. Francisco V. Fernández. Dr. Elisenda Roca Moreno and Dr. Rafael Castro López were the Technical Programme Chairs. The local organizing committee also included Prof. Alberto Yúfera and Dr. Jorge Mendoza as Local Arrangement Chairs and Dr. Piedad Brox and Dr. Rafael Castro López as Publications Chairs.

The main objective of SMACD2012 was to consolidate the conference, which is held biannually, as a reference forum for researchers and industries in the area. The large amount of submitted works and the high scientific quality of the final technical programme are clear indicators of the success in achieving this goal. The conference was also been sponsored by two of the most important companies in the area, Agilent Technologies and CADENCE, and had the technical co-sponsorship of the IEEE Council on Electronic Design Automation (CEDA), and the IEEE Systems and Circuits Society (CAS).

The conference was attended by about 100 scientist and professionals, mainly from Europe and northern Africa, although attendees were coming from four different continents.

The technical programme included a total of 52 papers for oral presentation and 12 papers for poster presentation, plus two special sessions, one on Design Tecniques from RF/Microwave circuits and a second one on MEMs and Heterogeneous Systems. Three plenary talks were programmed by well-known researchers in the field of the conference: "From circuits to cancer", by Dr. Sani Nassif, from IBM Austin Research Laboratory (USA) and IEEE CEDA president; "Analog Synthesis (and Verification) Revisited: What's Missing?", by Dr. Rob A. Rutenbar, from University of Illinois at Urbana Champaign (USA); and "Worst-case – what you always wanted to know about it and never dared to ask", by Prof. Helmut Graeb, from the Technical University of Munich (Germany). A keynote presentation was given by Alexander Perez, Support engineer and Consultant from Agilent Technologies in the field of RF circuit design entitled "Trends in Circuit/EM Cosimulation". A pannel session on "Challenges and solutions for electronic circuit design in nanometer CMOS" was organized by Prof. Georges Gielen, from KU Leuven (Belgium).

For the first time, SMACD2012 held an event where PhD and MSc students could compete with their best ideas, methodologies, flows and tools with one unique but challenging goal: improve design automation for analog, mixed-signal, RF, and multi-domain (MEMs, nanoelectronic, optoelectronic, biological, etc.) integrated circuits and systems. The competition was a great success, both in participation (with a large number of submitted works), and in attendance during the conference. The winer of the competition, which was elected by a jury formed by members of industry and academia, was awarded with a 1.000$ price sponsorized by CEDA.

ICECS 2012

19th IEEE International Conference on Electronics, Circuits and Systems

http://www.ieee-icecs2012.org/

From 9th to 11st December 2012, was held in the Barceló Hotel Renacimiento (Seville) the 19th IEEE International Conference on Electronics, Circuits and Systems (ICECS 2012). This conference sponsored by the Institute of Electrical and Electronics Engineers, is the flagship conference of the IEEE Circuits and Systems Society in Region 8 of IEEE (Europe, Middle East, and Africa).

The ICECS series of conferences have evolved during nearly two decades to become a major networking event for those working on Circuit and Systems topics, from analog and RF circuits to VLSI signal processing, including biomedical, emerging technologies, CAD, nonlinear and neural networks, etc, offering to attendees the opportunity to learn of the latest advances in these fields, and to meet those who have dared, pioneered, and succeeded.

ICECS 2012 were organized by members of the Institute of Microelectronics of Seville (IMSE- CNM), the Spanish Council of Research (CSIC) and the University of Seville. General Chairs of the Conference were Prof. Angel Rodríguez Vázquez, Dr Manuel Delgado-Restituto and Prof. Magdy Bayoumi and Technical Program Chairs were José M. de la Rosa and Gianluca Setti.The local organizing comitee also included Rocío del Río, Piedad Brox-Jiménez, Gustavo Liñán-Cembrano , Ricardo Carmona-Galán and Oscar Guerra-Vinuesa.

In this edition, a total of 380 submissions from 51 different countries were received including 222 papers from Europe, 61 from Asia-Pacific, 28 from North America, 26 from Latin America and 43 from the Middle East and Africa, proofing of the truly international nature of this event.

In addition to contributed papers, the event included three plenary lectures presented by world- wide recognized experts which covered hot topics in the circuits and systems field. They were: "Ultra-low-power circuit techniques for implanted/medical applications" by Prof. Yusuf Leblebici Director of the Microelectronic Systems Laboratory at the Ecole polytechnique fédérale de Lausanne (EPFL); "From data to insight" by Dr Ellen J. Yoffa. Director of the IBM Corp. T. J. Watson Research Center at Hawthorne (NY); "Compressive sampling analog to digital conversion" by Prof. Michael Flynn Dept. of Electrical Engineering & Computer Science (EECS) at the University of Michigan.

As a novelty this year, eight Tutorials covering a variety of topics were scheduled on Sunday 9 and offered for free to all attendees. The eight tutorials were: "Advances in time-encoded analog signal processing and data conversion" by Luis Hernandez, Susana Paton, Enrique Prefasi,from the Electronics Department of Carlos III University, Spain, and by Pieter Rombouts, from the Electronics and Information Systems Department of Gent University, Belgium; "Siliconized photonics-electronics as an emerging technology" by Henry H. Radamson and Lars Thylén from the KTH Royal Institute of Technology, Sweden; "RF CMOS Wireless Receivers for 402MHz Medical Implantable Communication Systems" by Sherif Mohamed and Yiannos Manoli from the Fritz Huettinger Chair of Microelectronics, IMTEK. Albert-Ludwig-University Freiburg, Germany; "Digital Delta-Sigma Modulators for DAC and Fractional-N Frequency Synthesis Applications" by Michael Peter Kennedy, from the Department of Electrical & Electronic Engineering and Tyndall National Institute, University College Cork, Ireland; "Using Logical Effort for Designing Carbon Nanotube FET (CNFET)- based Digital Circuits" by Malgorzata Chrzanowska-Jeske, from, Portland State University, USA; "Memristor Technology in Neuromorphic Circuits" by Fernando Corinto from the Department of Electronics and Telecommunications at Politecnico di Torino, Italy;" Low power design methodology and techniques – industrial perspective" by Kaijian Shi, from Cadence Design Systems, USA.

EXTERNAL LIAISON

COMMITTIES & SOCIETIES

Institute of Electrical and Electronics Engineers (IEEE)

Soft Computing in Image Processing (SCIP)

COMPANIES & ORGANIZATIONS

Ford (Research and Advanced Engineering Center in Aachen, Germany)

Philips (Philips Research Eindhoven, the Netherlands)

Technische Universiteit Eindhoven (the Netherlands)

Instituto Superior Politécnico José Antonio Echeverría (CUJAE)

CIMA Nuevas Tecnologías Informáticas S.L.

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Euskal Herriko Unibertsitatea

Universidad Politécnica de Cataluña

Vniversitat de València

Instituto Nacional de Técnica Aeroespacial

University of Southampton

institute of neuroinformatics
University of Zurich

Universitat Rovira i Virgili

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CiTIUS Centro Singular de Investigación en Tecnoloxías da Información

Centro Universitario de la Defensa de San Javier

Universidad Politécnica de Cartagena

AWARDS & RECOGNITIONS

During years 2011-2012 IMSE members have received the awards and distinctions listed below.

The *doctoral program in Microelectronics* which is coordinated by Prof. Ángel Rodríguez Vázquez and imparted by Doctors of the Department of Electronics and Electromagnetism (University of Seville), of the Department of Electronics Technology (Universidad de Sevilla) and of the Microelectronics Institute of Seville (IMSE-CNM) received the ***Mention of Excellence*** by Resolution of October 6, 2011 of the General Secretariat of Universities (BOE no. 253, October 20, 2011).

In November 2012, the *Instituto de Microelectrónica de Sevilla* and four of their members: *Prof. José Luis Huertas Díaz*, *Prof. Manuel Valencia Barrero*, *Prof. Ángel Barriga Barros* and *Dr. Santiago Sánchez Solano* were awarded by the ***CUJAE Seal***. This distinction, given by the Instituto Superior Politécnico José Antonio Echeverría from La Habana (Cuba), is an acknowledgment to prominent university professors and researchers who maintain a close collaboration with this institution. The prizes were given during the Gala Dinner of the "XVI Convención Científica de Ingeniería y Arquitectura" in La Habana.

"***Best Paper Award (First Runner-Up)***", to *Dr. José Manuel de la Rosa Utrera* for the paper entitled "Multirate Hybrid Continuous-Time/Discrete-Time Cascade 2-2 Sigma-Delta Modulator for Wideband Telecom", which was presented at the IFIP/IEEE Int. Conference on Very Large Scale Integration, 3rd-5th October 2011.

"***Best Paper Award***" for the paper "High-Level Design of a hibrid Sigma-Delta Modulator for UMTS/GSM/Bluetooth/WLAN Applications", authored by *Dr. José Manuel de la Rosa Utrera* presented at the 1st Workshop on Analog and Digital Electronic Design, October 2011 at Guadalajara, Mexico.

"***Best Contributions Award***" in the Laboratory Section of the del X Congreso de Tecnologías Aplicadas a la Enseñanza de la Electrónica (TAEE'2012), to the work "Prácticas de Laboratorio de Linux Empotrado sobre Placas de Desarrollo XUPV2P" co-authored by *Prof. Ángel Barriga Barros*. Vigo, June 2012.

At the International Conference on Synthesis, Modeling, Analysis and Simulation Methods and Applications to Circuit Design (SMACD) 2012 Competition, *Manuel Velasco Sánchez* obtained the ***Silver Competition Award*** with the work "Systematic Generation of Performance Models of Reconfigurable Analog Circuits". At the same competition the paper entitled "An Automated Layout-Aware Design Flow" presented by *Antonio Toro-Frías* was granted with the ***Bronze Competition Award*** (Ex Aequo).

In December 2012, at the IEEE International Conference on Electronics, Circuits, and Systems (ICECS), *Sonia Vargas* obtained one of the three first prizes of the ***ICECS 2012 PhD Student Competition*** with the work entitled "Control and Acquisition System for a High Dynamic Range CMOS Image Sensor".

OUTREACH

According to the report "Comprehension of Science" published by BBVA Foundation, nexus of the Spanish population and the scientist career is not as strong as we would desire and is below the European average, only 22% of people met a scientist and solely 16% of population has taken in consideration the possibility of taking such professional career. This situation is extremely paradoxical in a society which has experimented a revolution in the ways through we communicate, we interact or, in general, in how we live as a result of scientist advances. Microelectronics and more recently, nanoelectronics are in center of this revolution and, however, knowledge about these sciences and people involved in them is very poor, very confusing and sometimes more related to science-fiction than a rigorous science.

GUIDED TOURS

In an effort to reduce the gap between Science and Society, IMSE-CNM opens its doors to students and general public, offering guided tours through its facilities.

At the beginning of the tours, visitors can get to know the fundamentals of microelectronics and its applications watching some illustrative videos. Later on, IMSE-CNM´s scientists present their specific areas of research and their daily activity. Tours conclude de visiting the test facilities.

The participation of high school and undergraduate students in these activities has been very remarkable. Accompanied by their teachers, they have visited IMSE-CNM facilities on numerous occasions.

In this sense, we hope this initiative will serve as a mean of promotion for new scientist vocations.

CAFÉ CONCIENCIA

During this time, IMSE has integrated into the CSIC Outreach Network, participating in some events and activities like "Café Conciencia" where Manuel Barragán and Javier Castro, youngs researchers from IMSE, took part with the lecture "Why battery life in your Smart Phone is only one day" which was followed with great expectancy by the audience.


20

PISTAS PARA HOY

1 Presentación de la **novela** 'Democracia'

2 **Conferencia** del arzobispo Juan José Asenjo

3 Celebración de una **jornada** sobre Smart City

Vivir en Sevilla

Un capuchino de energías renovables

120 estudiantes de secundaria y una docena de investigadores participaron ayer en la actividad 'Café con Ciencia', que se celebró por segundo año, de forma didendida, en el Pabellón de Perú

El Museo de la Autonomía también apoya a la ciencia

Técnicos del IAPH hablan de la ciencia aplicada al arte

SOCIAL MEDIA

Traditionally, the gap between Science and Society has been wide and deep. For a long time, most scientists in the public research system regard their job as finished when they report their results in a specialized research journal. Today, this awareness has changed and the scientific community is trying to show citizens, using a language easily understandable, how Science has improved all aspects of their lives. Social Media are very important tools to gain access to people and, during the biennium 2011-2012, personnel of IMSE-CNM put a lot of effort in increasing their expertise in media and communication as a way to bridge science and society. As a result of this strategy, public visibility of IMSE-CNM has been substantially increased. Some examples of news items published by local and regional newspapers are shown in these pages. Other communications in video format can be found at *https://www.imse-cnm.csic.es/es/medios.php*.


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Contracorriente

Un invento contra el fuego

Jorge Fernández Berni diseña un novedoso sistema de visión artificial

RAFAEL CASTRO ÁVILA

El doctor ingeniero de Telecomunicación Jorge Fernández Berni ha diseñado un novedoso sistema de visión artificial que permite analizar una escena en tiempo real, extraer conclusiones sobre la misma y enviar los resultados a otros sistemas similares cercanos con los que conforme una red inalámbrica. La investigación se enmarca dentro de dos proyectos dirigidos por Ricardo Carmona Galán, científico titular del CSIC, y financiados por la Junta de Andalucía y el Ministerio de Ciencia e Innova-

Jorge Fernández (i) y Ricardo Carmona muestran este revolucionario invento.


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Las redes inalámbricas Wi-Fi o el Bluetooth, así como los teléfonos inteligentes o los ordenadores, utilizan sistemas de autenticación de sus usuarios para comprobar que quien accede al sistema es la persona autorizada. Un equipo multidisciplinar formado


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Andalucía

Sevilla

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