PhD Forum: A survey on FPGA-based high-resolution TDCs

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ABSTRACT

Time-to-digital converters based on Nutt method are especially suitable for FPGA implementation. They are able to provide high resolution, range and linearity with low resources usage. The core of this architecture consist in a coarse counter for long range, a fine time interpolator for high resolution and real-time calibration for high linearity. This paper reviews different time interpolation and real-time calibration techniques. Moreover, a comparison of state-of-the-art FPGA-based TDCs is presented as well.

CCS CONCEPTS

CCS → Hardware → Integrated circuits → Reconfigurable logic and FPGAs → High-speed input/output

KEYWORDS

Field-programmable gate array (FPGA), time-to-digital converter (TDC), fine time interpolation, real-time calibration.

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1 Introduction

TDCs are a central component in systems based on time-delay assessment. Resolution is a critical specification of TDCs in many applications, especially those based on time-of-flight (ToF) estimation, from 3D imaging to nuclear medicine detectors. Therefore, high resolution TDCs are in high demand. Other principal characteristics to be sought for in a TDC design are time range, linearity, and resource usage.

Nutt method, which combines a coarse counter with a fine time interpolator is the most extended method to cover a long time interval while preserving a high time resolution. The coarse counter scores the number of reference clock periods between the start and stop signals and the fine time interpolator measures the time intervals between each of these signals and rising edge of the reference clocks next to them.

FPGAs represent an interesting option to explore fully-digital TDC architectures, because of their flexibility, shorter development time and lower prototyping cost than ASICs. They are reconfigurable and usually built on the finest silicon technologies. Also, by exploiting fast carry chains of FPGAs, sub-hundred-picosecond resolution can be achieved [1] In order to minimize the influence of voltage and temperature changes and nonlinearity, real-time calibration is needed. Multiple measurements for each time interval can be employed to reduce nonlinearity.

In this paper, fine time interpolation methods and accuracy improvement techniques have been investigated and a comparison between the state-of-the-art FPGA-based TDCs has been provided.

2 Fine Time-interpolation Methods

Several techniques have been used to implement the interpolator. The first method, based on tapped delay lines (TDLs) [2] , consist of a number of consecutive delay elements with equal theoretical propagation delay. The fine time measurement is achieved by sampling the state of the delay line when START and STOP signals are detected. For high resolution, carry elements can be employed as delay cells. A carry element is a FPGA component for fast arithmetic calculation. Its propagation delay is short. Carry chains have been extensively used as delay lines in FPGA-based TDCs.

The second method is using multiple clock phases linked to the reference clock to achieve sub-clock resolution [3] The number of phases is limited and thus the best achievable resolution.

The third method is delay-line loop-shrinking [4] It is based on two delay-line loops. The resolution is equal to the difference between their delay times. The loops have similar architecture, the same number of delay cells, but differ in their routing and placement. This method has a long dead time, more than one microsecond. Therefore, it is not suitable for high sampling rate TDCs.

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The fourth method is using a matrix of counters [5] . Now, routing resources are used as delay elements. They are metal tracks and they are not sensitive to voltage and temperature drifts. No special circuitry for PVT compensation is needed.

These methods are compared in Table 1. For applications requiring a-few-hundred-picosecond resolution, a multiphase clock interpolator is the best. For sub-hundred-picosecond resolution applications, it is TDL. If resource usage and dead time are not that important, a matrix of counters provides the highest resolution.

Table 1: Fine time interpolation methods comparison

Method	TDL	Multiphase Clock	Shrinking Method	Matrix of Counters
Resolution (ps)	10	160	60	7.4
Dead time (ns)	1.5	8	1410	80
INL (LSB)	0.7	0.05	0.7	1.57
Meas. Range	High	High	Limited	High
Resources Usage	Medium	Low	Medium	High
PVT compensation	Yes	No	Yes	No

3 Accuracy Improvements

Ambient conditions may change while measuring time intervals. These changes can increase the nonlinearity and change the bin width. In order to prevent TDC performance degradation, real-time calibration is essential. Several calibration techniques have been introduced in literature. Most of them calibrate the bin width at the cost of dead time and resources usage, except the on-the-fly calibrator implemented at [6] The main advantage of this method is that it uses the measured data to renew the calibration table without any additional dead time.

In order to improve the precision, multi-measurement TDCs can be employed. They can be based on either multi-TDLs or multiple measurements with the same TDL. The former improves resolution at the cost of resource usage. But, the latter technique uses the same TDL for multi-measurement and leads to additional dead time

Besides, it does not guarantee better precision all the time. For instance, if the time interpolator is based on a free-run ring oscillator [7] there is an optimal number of measurements for the best precision. Beyond that, precision degrades due to the accumulated jitter at the ring oscillator.

4 Comparison and discussion

In order to provide a comparison between state-of-the-art FPGA-based TDCs reported in [1-2], [5], and [8-11], we have computed this figure of merit (FoM).

$$\mathrm{FoM} = \frac{1}{F_S \times 2^{N-log_2(\mathrm{INL}+1)}} \qquad (1)$$

where F_S is the sampling frequency, N is the number of bits and INL is the corresponding integral nonlinearity. Very few references report their power consumption. Probably because power consumption was not a main issue for them. Therefore, it not been included in the FoM. The figure of merit vs. time resolution is plotted in Figure 1. Each point is labeled with the name of the first author, publication year, and FPGA technology in nm. Obviously, TDC performance depends on FPGA technology and newer technologies lead to better performance. As can be seen in Figure 1, the design reported in [11] and labeled with [Won'16 , 40] has obtained the best FoM. They have improved INL and measurement uncertainty by changing the sampling pattern of the carry chain without additional dead time.

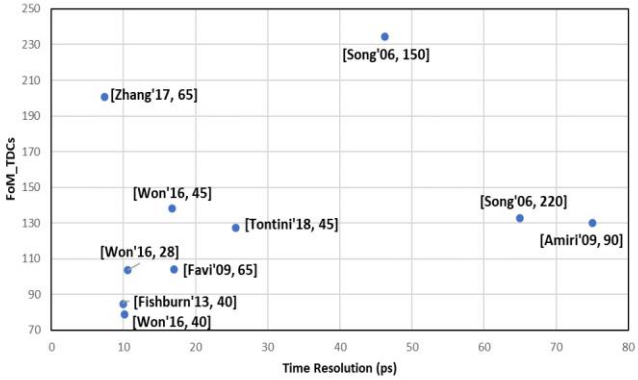

Figure 1: FoM vs. time resolution

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