A thermal study of multilayer RRAMs based on HfO₂ and Al₂O₃ oxides

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An in-depth analysis including both simulation and experimental characterization of Resistive RAMs (RRAMs) with dielectric stacks composed of two layers of HfO₂ and Al₂O₃ stacked in different order is presented. The simulator, that includes the electrodes in the simulation domain, solves the 3D heat equation and calculates the device current. The results are employed to analyze thermal effects in bilayer HfO₂ and Al₂O₃-based RRAMs with electrodes of Ni and Si-n+ during resistive switching (RS) operation. According to our simulations and the experimental data, the narrow part of the conductive filaments (CF) is formed in the HfO₂ layer in all the cases and, therefore, no important differences are found in terms of reset voltage if the oxide stack order is changed with respect to the electrodes. This result is attributed to the fact that the heat flux in the Al₂O₃ is higher than

in the HfO_2 layer and this determines the thermal behavior and RS operation. The heat transfer rate from the conductive filament to the electrodes and surrounding oxide has been analysed. The lateral heat flux component from the CF to the oxide is shown to be important with respect to the vertical component (from the CF to the electrodes).

I. INTRODUCTION

RRAMs will be a key technology for future non-volatile memory circuits¹⁻⁷. Applications of RS devices can also be found in the neuromorphic and hardware security circuit realms^{5, 8, 9}. A continuous growth of the publications linked to resistive memories in all the research facets has been driven by both industry and academia in the last few years due to the outstanding features of these devices in connection to their fast read/writing speed, low power consumption, good retention and endurance characteristics, and their CMOS technology compatibility^{5, 6, 7, 10, 11}.

A resistive memory consists of two electrodes composed of metallic materials that are separated by a dielectric that is usually fabricated using one or several oxide layers. RRAM research on these devices has dealt with dozens of devices with different combinations of electrodes and dielectrics, including a great variety of materials, even 2D structures⁴. Filamentary conduction through CFs is the most common operation mechanism: it is based on the stochastic formation and destruction processes of ohmic conductive filaments that shunt the electrodes^{1, 2, 5, 6, 7, 11, 12, 13, 14, 15}. These processes are linked to localized high temperature regions (generated by Joule heating) in which thermally based mechanisms are triggered^{11, 16, 17}. Consequently, in order to obtain a deeper understanding of the main parameters influencing the RS phenomenon in different stacks a detailed device thermal description is required. In this way, we can detect the regions that reach high temperatures and the heat flux nature inside the device. In this work, we deal with these issues to analyze RS in RRAMs with dielectrics composed of different materials: HfO_2 and Al_2O_3 . In addition to simulations, we have employed a wide set of experimental data obtained from devices previously fabricated^{18, 19}. In this respect, long series of experimental RS cycles are analyzed in four different device

structures (see Figure 1). These results are interpreted by using the temperature distributions obtained by solving the 3D heat equation considering truncated-cone shaped conductive filaments and including the electrodes as a part of the simulation domain (SD). The analysis of the heat flux from CF to the dielectric and the electrodes allows further understanding of the phenomenology behind the RS phenomenon. The study performed describes the role played by the different materials employed in the device fabrication and explains the obtained experimental reset voltage distributions.

The paper is organized as follows: in Section II, we give details of the fabricated devices and measurement set-up. The main features of the numerical simulator are explained in Section III. In Section IV we present the main results and the corresponding discussions. The final conclusions are drawn in Sec. V.

II. DEVICE FABRICATION AND MEASUREMENT

The Ni/insulator/Si- n^+ devices are field-oxide isolated square structures fabricated on (100) highly doped n-type CZ silicon wafers with a resistivity of $(7\text{--}13) \text{ m}\Omega\cdot\text{cm}$ ^{18, 19}. The HfO₂ and Al₂O₃ layers were grown at 225°C by atomic layer deposition in a Cambridge NanoTech Savannah 200 system equipped with trimethylaluminum (TMA), tetrakis(dimethylamido)-hafnium (TDMAH), and H₂O as precursors, and N₂ as carrier and purge gas. A schematic cross-section of the fabricated bilayer and single layer resistive RS devices is shown in Figure 1. The I-V curves were measured using a HP-4155B semiconductor parameter analyzer. The voltage was applied to the top Ni electrode, while the Si substrate was grounded. Long RS cycle series were measured in an automatic

procedure controlled using MATLAB and a GPIB (General Purpose Instrumentation Bus) connection for the whole set-up.

FIG. 1. Set of devices used in this work. α and β stacks are made out of HfO_2 and Al_2O_3 layers changing their position with respect to the electrodes. In the γ and δ cases the dielectric consist of a single oxide material.

Figure 2a shows typical I-V curves for the devices under consideration. The reset and set voltages and the corresponding currents have been extracted for the series of cycles analyzed and the results are plotted in Figures 2b and 2c. The reset voltage Cumulative Distribution Functions (CDF) are shown in Figure 2d for the four different RRAMs. The reset voltage CDFs for the α , β and δ cases have a similar behavior in terms of the reset voltage values; nevertheless, for the device corresponding to the γ dielectric stacking, the only one without HfO_2 in the dielectric, the reset voltages are higher (see the green curve in Figure 2d and the green point cloud in Figure 2b).

FIG. 2. a) Representative set and reset I-V curves for the devices with the α , β , γ and δ dielectric stacking described in Figure 1. The reset (set) curves are shown in solid (dashed) lines. b) Reset current (I_{Reset}) versus the corresponding reset voltage (V_{Reset}), c) Set current (I_{Set}) versus the corresponding set voltage (V_{Set}), d) Cumulative distribution functions for V_{Reset} for the devices under consideration.

As reported previously, the reset process is characterized in these devices by a sudden temperature rise in the conductive filament and the surrounding regions^{12, 20, 21, 22}. Therefore, the differences observed experimentally in the reset voltage for the δ devices could be linked to the thermal response of this particular structure. In order to check that issue, a 3D RRAM simulator has been implemented where a detailed solution of the heat equation is performed. Consequently, the temperature distributions and heat flux in the different device regions can be obtained.

III. SIMULATOR DESCRIPTION

Our simulation tool solves the heat equation in a 3D simulation domain (SD) that includes all the active parts of the RRAMs under study. The equation is solved making use of the fully explicit finite difference method²³. The device electrodes (the electrode region closer to the dielectric) have been included in the simulation domain to account for the important heat flux at the dielectric-electrode interface. The SD is shown in Figure 3: it consists of a matrix of 161x161x321 nodes with a uniform mesh (161 nodes in the X, Y directions and 321 in the Z direction). We have assumed a grid mesh distance of 0.125 nm, corresponding approximately to the Ni atom radius, in line with previous tools based on different simulation approaches²⁴. The layer of the electrode materials included in the SD is 10nm thick. At these outer electrode layer surfaces Dirichlet boundary conditions are included (assuming the constant temperature located outside the device, room temperature in our case). This is a reasonable assumption since the electrode thermal conductivities are high and consequently, a high heat conduction (Fourier's law) would keep the temperature distribution uniform in the electrodes. In the SD lateral faces, perfectly matched layers (PML)²⁵ are employed. PMLs are an interesting numerical tool of common use in parabolic partial differential equation (as heat equation), hyperbolic partial differential equation (wave equation) and even in elliptic partial differential equation (e.g. Poisson's equation as shown in Ref. 26). PML allows one dealing with open boundary problems, such as the boundary conditions we have in the lateral faces of the simulation domain here.

Joule heating occurs in the metallic-like conductive filament, which is formed by an atom cluster that it is modeled as a truncated-cone (see Figure 3)^{1, 20, 24, 27}. The CF

electric conductivity was in line with the one reported in Ref. 20 and after an extensive process of experimental data fitting. In our modeling approach the current flows through a fully formed conductive filament; therefore, the device is in the low resistance state (LRS). Series and Maxwell resistances are also taken into account for the current calculation. After the current determination, the heat generation rate ($\dot{q}$) is obtained and introduced in the corresponding term following references^{5, 20, 28} (see Equation 1).

$$\dot{q} = -\nabla[k_{th}(x, y, z)\nabla T(x, y, z)] \quad (1)$$

As described in Equation 1, the different thermal conductivities have to be incorporated in a 3D matrix in the SD. For the wider layers (the electrodes, although only a 10 nm layer is included in the SD) 3D thermal conductivity values are used ($k_{th}(\text{silicon})=148 \text{ W/m K}$, $k_{th}(\text{Ni})=90 \text{ W/m K}$).

FIG. 3. Simulation domain for the RRAMs under study. The yellow and red layers correspond to the electrode regions (Si-n+ and Ni, respectively). In between the electrodes, we find the dielectric where the CF is formed (represented by a cluster of atoms). The dielectric is composed of two layers (the α case is represented here, the β case is obtained by changing the oxide layers order), or the dielectric consists in a single oxide layer (corresponding to γ and δ structures).

The CF thermal conductivity was $k_{th}(CF) = 19 \text{ W/m K}$, a value in line with data previously reported^{24, 28}. For the dielectric layer thicknesses employed here a general rule described in Ref. 29 can be applied. Roughly one-tenth of the bulk value for the thermal conductivity can be considered for dielectric layers few nanometers thick. In our case, the following values were used: $k_{th}(Al_2O_3) = 2.86 \text{ W/m K}$ and $k_{th}(HfO_2) = 1.0 \text{ W/m K}$; in choosing these values we have taken into consideration other Refs. 29, 30, 31, 32 for the coherence of the thermal conductivity values.

The 3D heat equation has been solved by means of the fully explicit finite differences numerical method. However, for the sake of comparison, the fully implicit weighed residuals method has been also used in some simulations. The results are the same. Nevertheless, we chose the explicit method because it is faster achieving the same degree of accuracy.

IV. RESULTS AND DISCUSSION

Using our self-developed RRAM simulation tool, we were able to study the temperature distributions of devices working in the LRS. We did so for all the structures considered in Figure 1 assuming the same oxide layer thicknesses. A truncated-cone shaped

CF has been supposed, with the same orientation in all the cases (from top to bottom, the widest radii on the dielectric-Ni interface, see Figure 3).

FIG. 4. Temperature distribution cross-sections for the device structures α (first row) and β (second row) in the X-Y plane that corresponds to the different materials (electrodes and oxide layers) of the RRAMs analyzed. The simulations have been performed assuming a device current of 0.4 mA in all cases. The first graph on the left corresponds to a cross-section in the silicon electrode, 0.125nm below the interface Si/oxide, the second corresponds to a cross-section at 1.5nm above the silicon-oxide interface (the maximum temperature in all the SD; the narrowest part of the CF is close to this position in all the considered device structures), the third is placed 0.125nm above the two oxide layers interface, and the graph on the right is a cross-section in the Ni electrode, 0.125nm below the oxide/Ni interface.

We have calculated the device current for different voltages. In all the cases considered here, the CF narrowest part is placed in the dielectric layer closer to the Si electrode. As can be seen in Figure 4, the temperature achieved in the lower oxide layer (where the CF narrow section is placed) is higher for the β device in comparison to the α

device; i.e., for the case where the HfO_2 layer is closer to the Si electrode. This result is coherent with the lower thermal conductivity of this material with respect to Al_2O_3 . In both cases (α and β) the higher temperatures are achieved in the oxide layer closer to the Si electrode (1.5nm from the interface); this result makes sense since the concentration of current lines in the CF narrowest part produces the higher Joule heating dissipation effects in this region. In order to highlight the differences between the highest temperature distributions in these devices, a direct comparison is shown in Fig. 5.

FIG. 5. (a) 3D Temperature distributions for the device structures α and β in the X-Y plane for the cross-section at 1.5nm above the silicon-oxide interface. (b) Temperature difference $[T(\beta \text{ device}) - T(\alpha \text{ device})]$ in the X-Y plane for the cross-section 1.5nm above the silicon-oxide interface. The same bias employed in Figure 4 was used here.

The higher temperatures correspond to the β device structure, as shown in Figure 5. It is known that the reset process in unipolar devices (like the ones under study here) is temperature dependent^{5, 21}; therefore, the thermally assisted mechanisms that lead to the CF rupture would be triggered in the region where the temperature is higher, that is in the oxide layer closer to the Si electrode in the simulated devices. In this respect, the temperature difference plotted in Figure 5 would lead to reset voltages of different value for the device structures α and β ; however, this is not the case, as can be seen in Figure 2.

This result would suggest that the CF narrow section is placed in the HfO_2 layer independently on the stack order employed in the device fabrication.

In order to deepen on this issue, two more device structures were analyzed and employed as a reference for our reasoning (γ , with a single layer of Al_2O_3 in between the electrodes and δ , with a single HfO_2 layer, see Figure 1). We call the reader's attention to the fact that the simulations in these two structures lead to the expected results in terms of the temperature distributions (Figure 6).

FIG. 6. Temperature distribution cross-sections for the device structures γ (first row) and δ (second row) in the X-Y plane that corresponds to the different materials (electrodes and oxide layer) of the RRAMs analyzed, see Figure 1. The simulations have been performed assuming a device current of 0.4 mA in all cases. The first graph on the left corresponds to a cross-section in the silicon electrode, 0.125nm below the interface with the oxide, the second corresponds to a cross-section at 1.5nm above the silicon-oxide interface, the graph on the right is a cross-section in the Ni electrode, 0.125nm below the Ni-oxide electrode.

The simulation results show that the temperature is higher in the device with the HfO₂ dielectric since the thermal conductivity is lower, and therefore, the heat flux from the CF to the surrounding dielectric is lower. A direct comparison of the temperature distributions shown previously is plotted in Figure 7. A higher temperature is clearly observed in the δ device.

FIG. 7. (a) 3D Temperature distributions for the device structures γ and δ in the X-Y plane for the cross-section at 1nm above the silicon-oxide interface. (b) Temperature difference $[T(\delta \text{ device}) - T(\gamma \text{ device})]$ in the X-Y plane for the cross-section at 1nm above the silicon-oxide interface. The same bias employed in Figure 6 was used here.

The comparison of the experimental reset voltages for these two device types is shown in Figure 2. If the CF narrow part were placed in the Al₂O₃ layer for the α , β structures, the reset voltages measured in these two structures would be similar to the ones found in the γ structure, which is not the case. Nevertheless, the reset voltage CDFs for the structures α , β and δ are the same. In this regards the assumption raised previously (the narrowest portion of the CF is located at the HfO₂ layer, independently on the stack order) is coherent with the experimental data and the simulations performed. Finally, it is

important to highlight that the experimental reset voltages for the γ structure (a single layer of Al_2O_3) show values higher than those found in the other structures. In this case, the whole CF is formed in the Al_2O_3 layer and therefore the heat transfer rate is higher than in the three other cases; as a consequence, higher voltages are needed to heat the CF up to the temperature regime where the physical mechanisms behind the reset process are triggered. These higher reset voltages are shown in green dots in Figure 2c and in green lines in Figure 2d.

For the sake of completeness, we have also calculated the heat transfer rate in the devices under consideration following the sketch is shown in Figure 8.

FIG. 8. Thermal energy flux for the RRAMs under study. The heat flux has two main directions: from the CF to the surrounding dielectric (lateral heat conduction) and from the CF to the top and bottom electrodes (vertical heat conduction). The heat loss in these two different directions (and their relative value with respect to the total heat loss) and heat loss in each oxide layer can greatly affect the RRAM resistive switching operation.

The calculation of the heat transfer rate (HTR) has been performed solving numerically the corresponding surface integrals for the heat flux density obtained by means

of Fourier's law. In order to study the amount of energy that flows in each part of the RRAM, we computed the total energy flux that escapes from the CF to each material (see FIG. 8.), making use of an imaginary surface around the CF. If we observe the amount of energy lost in each one of the oxides (FIG. 9) we can see that in the α case, the heat transfer rate is much bigger in Al_2O_3 than in HfO_2 as expected. It is also important to highlight that the heat transfer rate in the lateral direction is important (more than a 20% of the total HTR) in comparison with the vertical direction. This means that thermal models within complete RRAM electrical compact models have to account for the heat losses in the lateral direction and consider this energy flux in the corresponding thermal resistances.

FIG. 9. Heat transfer rate versus applied voltage for the α RRAM structure. The heat transfer rate is represented for both electrodes (total vertical HTR) and for the two oxide layers of the device (lateral HTR), the total rate through the dielectric stack is also plotted for reference.

V. CONCLUSIONS

An in-depth study of thermal effects in HfO_2 and Al_2O_3 based RRAMs composed of single oxide layers or bilayers stacks, and with Ni and Si-n^+ as top and bottom electrodes, respectively, has been presented. The devices have been fabricated making use of ALD grown HfO_2 and Al_2O_3 oxides, with the two materials interchanged in different dielectric stacks. The reset voltages are characterized for these devices and others with single layer dielectrics. The experimental results have been complemented with simulations obtained with an ad-hoc RRAM simulation tool developed where the 3D heat equation is solved including the electrodes. By means of comparison of experimental reset voltage distributions and thermal simulations, it has been found that the hottest portion of the filament (and therefore, the narrowest section of the CF where the disruption takes place) is always located at the HfO_2 layer (if present), independently on the stack order. It has been found that the heat transfer in HfO_2 layers is lower than in Al_2O_3 and therefore the devices reach higher temperatures in the regions where the narrow CF section is found. This higher temperature affects the reset voltage, which is lower due to the poorer HfO_2 thermal conduction. For the device with Al_2O_3 as the only dielectric, the thermal conduction is better and, therefore, the reset voltage higher. The results show that thermal effects are essential to correctly describe resistive switching in RRAMs along with the thermal properties of the materials employed in their fabrication. The heat transfer rate from the conductive filament to the electrodes and the surrounding oxide has been analysed. The importance of lateral heat flux from the CF to the oxide suggests that thermal resistances within compact models should account for these lateral components.

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