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Grid voltage regulation using a reset PI+CI controller for Energy storage systems

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Abstract: Hybrid controllers are capable of improved performance over their linear counterparts. In particular, reset controllers like the PI+CI are capable of fast flat response for lag dominant plants. Grid connected power converters especially interfacing energy storage systems to grids are required to have fast response to varying load demands to ensure minimum variation in grid parameters. Application of PI+CI controllers in such systems can improve their performance. In this work the improvement brought about by use of PI+CI controller employed for energy storage system power converters is highlighted by comparing it with PI controller based system under load variations. A DC microgrid with Fuel cell-supercapacitor based storage elements are considered here. The design criteria and simulation results are presented here.

Keywords: Hybrid systems, non-linear systems, power system, voltage control, disturbance rejection.

1. INTRODUCTION

Reset controllers belong to the group of hybrid controllers. Since the introduction of reset controllers through the Clegg Integrator (CI) in, Clegg (1958) many works have been done in this field. The CI is an integrator which resets to zero when input is zero. These reset actions improve closed-loop performance, by eliminating or significantly reducing output overshoot while reference tracking. Different type of reset controllers like First order reset element (FORE) was studied extensively in the works of Krishnan and Horowitz (1974); Horowitz and Rosenbaum (1975); Zaccarian et al. (2005); Nesic et al. (2011) and PI+CI controllers in Baños and Barreiro (2009); Baños and Vidal (2012); Baños and Davó (2014). Reset controllers provide the advantage that they are capable of performance levels which are impossible to obtain by linear control, and this is achieved simply by introducing reset actions at some specific instants (typically when the error signal is zero, but there are other possibilities), Baños and Vidal (2012).

The PI+CI controller is a modification of the classic PI (proportional integral) controller employing a CI in parallel. This allows for zero steady state error for step-like reference/disturbances ensured by the PI and reduced controller overshoot by the CI. The PI+CI controller is capable of a fast flat response in reference tracking problems and improved disturbance rejection as shown in Baños and Davó (2014). This makes PI+CI controller an interesting choice for a variety of applications as explored in Villaverde et al. (2011), Vidal et al. (2008), Heertjes et al. (2016), Baños and Davó (2014).

The ability of the PI+CI systems to generate a fast flat response, for lag dominant plants and ideally for first order plants, is an interesting property which can be exploited in grid connected systems. Nowadays, with increased penetration of Renewable energy sources (RES) there are increasing changes in modern grids in the way power is being delivered. There is an increased deployment of power electronic converter in modern grids since it is necessary to employ these converters as interfacing systems for the grid connection of RES, Bory Prevez et al. (2018). In order to combat the non dispatchable nature of RES there is also an increased deployment of Energy Storage Systems (ESS) in present grids. These ESS stores surplus energy from RES and gives it back to the grid when there is deficiency in energy generation, Denholm et al. (2010). This ensures the stability of the grid and improves the penetration of RES. The grid connection of ESS also requires interfacing power converters. These converters provide controllability of the power flow between these sources and grid. These grid connected systems are required to respond fast to load changes in order to ensure that the grid parameters like voltage, frequency (AC grid) remain within the prescribed limits. This requires that the converters interfacing these sources have controllers capable of fast response.

Currently most of these converters employ PI control tuned such that they meet grid codes. A fast response with PI control will necessarily result in overshoot which can be observed in the grid voltage, frequency profiles. Therefore these controllers can be further improved by ensuring a flat response so that the voltage profiles in the grid has minimal effect. Flat response from converters have been achieved with higher order

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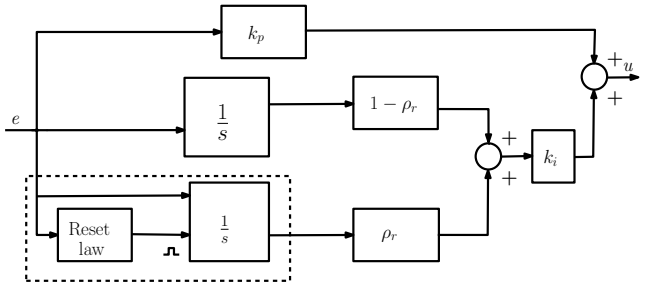

Fig. 1. Schematic of a PI+CI reset controller

sliding mode controller as shown in Ashok et al. (2014); Ramanarayanan (1986) and with differential flatness theory based controllers as mentioned in Thounthong et al. (2014). Although these controllers can result in flat response they tend to be complex. The PI+CI controller may be a sound alternative since it can ensure flat response while keeping the controller design easier through simple analytical equation and easy implementation.

In this work the application of a PI+CI controller in power converter connecting ESS to DC microgrid is considered for an interconnected system formed by a hybrid ESS system comprised of Fuel cell(FC) and Supercapacitor(SC). The main objective is to identify the improvement in grid voltage profile under varying load condition that can be brought about by this controller. To this extent two systems, one designed with PI controller and another with PI+CI controller will be simulated and their results will be compared. The modelling of the RES, ESS is not considered in detail as it is not the main focus of this work. This work emphasizes the application part in grid connected systems of simple reset controllers. A detailed and more theoretical analysis of stability and robustness, based on Baños et al. (2016); Baños and Davó (2014) will be performed elsewhere.

The rest of the paper is structured as follows. Section 2 presents preliminaries where the PI+CI controller model and system equations are presented. Section 3 presents the control architecture employed for the system. The converter models and controller design procedure for the same is also explained here. Finally simulation results and conclusions are provided in Section 4 and 5 respectively.

2. PRELIMINARIES

2.1 PI+CI reset control system

The schematic representation of a PI+CI reset controller is shown in Fig.1. k_p and k_i represents the gains of PI controller to which CI is connected in parallel. The highlighted region is the CI part. The reset law indicates the condition at which the CI resets its output. The term ρ_r is the reset ratio which indicates the percentage of the integral action that gets reset. The PI+CI controller is represented mathematically using the impulsive dynamic equations, Baños and Vidal (2012). The reset controller can be classified into two depending on the nature of ρ_r, as a constant or variable reset ratio controllers. The variable reset ratio controllers are capable of a flat response on fist order system compared to a constant reset ratio controller and is considered in this work, Baños and Davó (2014). The variable reset ratio controller is expressed in the impulsive differential form as

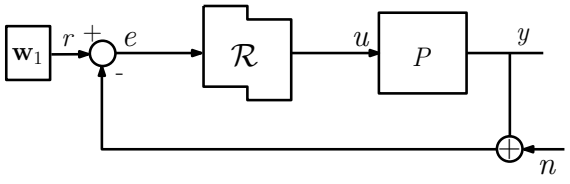

Fig. 2. Reset control system

$$\begin{cases} \dot{\rho}_r(t) = 0, \dot{\mathbf{x}}_r(t) = \mathbf{A}_r\mathbf{x}_r(t) + \mathbf{B}_r e(t), & e(t) \neq 0 \\ \rho_r(t^+) = \mathcal{P}(\mathbf{x}_r(t), e(t)), \mathbf{x}_r(t^+) = \mathbf{A}_\rho \mathbf{x}_r(t), & e(t) = 0 \\ u(t) = \mathbf{C}_r(\rho_r(t))\mathbf{x}_r(t) + \mathbf{D}_r e(t) \end{cases} \tag{1}$$

The matrices $\mathbf{A}_r, \mathbf{B}_r, \mathbf{C}_r, \mathbf{D}_r$ and $\mathbf{A}_\rho$ are

$$\mathbf{A}_r \triangleq \begin{bmatrix} 0 & 0 \\ 0 & 0 \end{bmatrix}, \quad \mathbf{B}_r \triangleq \begin{bmatrix} 1 \\ 1 \end{bmatrix}, \quad \mathbf{C}_r \triangleq k_i \begin{bmatrix} 1-\rho_r & \rho_r \end{bmatrix}$$

$$\mathbf{D}_r \triangleq k_p, \quad \mathbf{A}_\rho \triangleq \begin{bmatrix} 1 & 0 \\ 0 & 0 \end{bmatrix}$$

where $\mathbf{x}_r = [x_i \ x_{ci}]^T$ are the states of the controller, $\mathbf{x}_r(t^+) = \mathbf{x}_r(t+\varepsilon)$ with $\varepsilon \longrightarrow 0^+$, $e(t)$ is the error of the system and $\mathcal{P}(\mathbf{x}_r(t), e(t))$ is the variable reset ratio function defined as $\mathcal{P} : \mathbb{R}^2 \text{ x } \mathbb{R} \rightarrow \mathbb{R}$ and $\mathbf{C}_r(\rho_r(t)) = k_i[1-\rho_r(t) \ \rho_r(t)]$. The reset law in the above case is the zero error instance which will reset the CI output.

The Fig.2 shows a plant controlled by the reset controller $\mathcal{R}$. In the case of plant P defined by a first order system

$$P(s) = \frac{b_0}{s + a_0}, \tag{2}$$

subjected to an exogenous input $\mathbf{w_1}$ represented by a step signal of initial value w_{10} the variable reset ratio to ensure a fast flat response is given according to, Baños and Davó (2014) as

$$\rho_r(t_k) = \begin{cases} 0 & k = 0 \\ 1 - \dfrac{a_0 w_{10}}{b_0 k_i x_i(t_k)} & k > 0 \end{cases} \tag{3}$$

where $x_i(t_k)$ is the integrator value at the instant of reset. The value of ρ_r in (3) though appears varying, in the actual implementation takes a constant form. This is because after the first reset instant the system reaches the steady state and the value of $x_i(t_k) = x_i(t_{k+1})$ making ρ_r a constant.

2.2 Energy storage systems

Energy storage systems (ESS) are becoming an integral part of modern grids with increased penetration of renewable energy sources (RES) mainly to combat the stochastic and pulsating nature of the output power form these sources. The ESS ensure energy balance by acting as a spinning reserve, provides smoothing function at the output of RES and ensures that the grid parameters remain within the prescribed limits, Denholm et al. (2010), Ma and Cheung (2016). In the grid connected scenario the ESS need to cater sudden changes in load demand and prolonged period of energy imbalance. This requires that the ESS should meet both fast dynamics and slow variations. As no single ESS can cater to such demands without being oversized hybrid storages systems comprising of different ESS is considered as solution for grid connected applications, Schaltz et al. (2009). The selection of ESS in grid connected application is based on the power and energy density characteristics of the same. The ESS with high power density capability, i.e

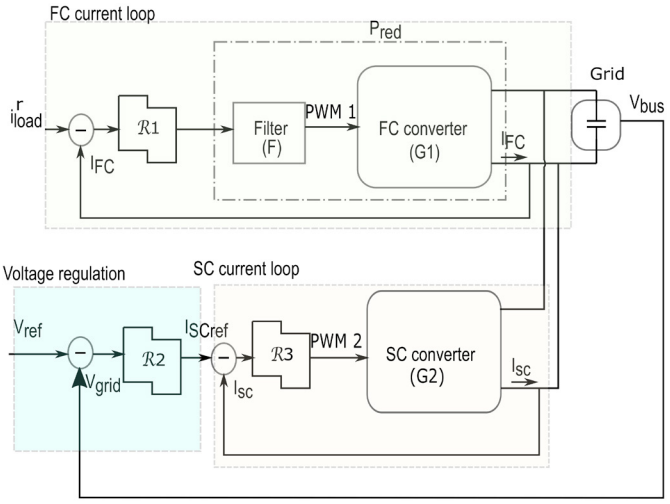

Fig. 3. Control architecture for the proposed system

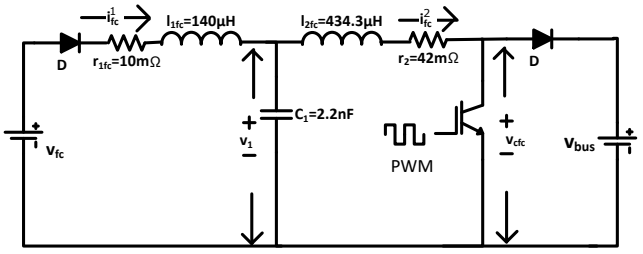

Fig. 4. Schematic of FC converter

capable of supplying large power for short duration are usually supercapacitors, flywheels, super conducting magnetic storage etc. These cannot meet the energy demand for a longer time. The ESS with high energy density, i.e capable of supplying energy for a longer time period, are pumped hydro storage, compressed air storage, fuel cells, batteries etc. These ESS when subjected to sudden power changes can be degraded affecting the life-time of the same, Chen et al. (2009). Therefore in grid connected applications it is essential to have a hybrid ESS comprising of elements from both the above mentioned groups to meet the different load scenarios in the grid. In this example a hybrid ESS system formed by FC and SC connected to a DC- microgrid is considered.

3. CONTROL ARCHITECTURE AND CONTROLLER DESIGN FOR AN ESS BASED DC-MICROGRID

The schematic of the ESS connection to DC microgrid is as shown in Fig.3. As discussed before the objective here is to analyse the performance of the interconnected system when the PI controller is replaced with the PI+CI controller. A simple rule for the power splitting is considered here under the assumption that load profile is known a priori. The FC converter will be provided with the load profile in the form of current reference (i^r_{load}) as shown in Fig.3. The FC controller is designed slower than that of the SC controller so that the FC does not meet the sudden load changes instantaneously but slowly ramp up and meet the reference value. The SC controller is designed using a multi-loop architecture. The outer loop is a voltage control loop which is tasked with maintaining the grid voltage (V_{bus}) at the nominal value thus regulating the DC bus voltage. The inner loop is the current loop which works on the reference from outer loop such that sufficient current is injected into the grid to ensure the grid voltage remain within prescribed range. Employing such a control architecture for the SC ensures that when the demanded load level changes the voltage difference created by the load imbalance as the FC ramps up in power will activate the SC outer loop causing the SC to supply the deficient power. Through this, sudden changes in load requirement will be met by the SC and larger imbalances by FC.

3.1 FC converter modelling and controller design

The FC converter as shown in Fig.4 is a DC-DC boost converter. Since the main objective here is to highlight the proposed improvement in performance achieved by the reset controllers a detailed modelling of the FC is not done and is simply realised as a voltage source v_{fc}. The system modelling is done considering the average voltage across the power electronic switch (IGBT in this case) $v_{cfc} = d'_1 v_{bus}$ where $d'_1 = 1 - d_1$ with d_1, the duty ratio of the gate signals for the FC side. This ensures that the high frequency switching ripples are neglected in the modelling. The FC converter model is derived using the framework employed in Erickson (2002) and is obtained as (4)

A variable change is proposed for (4) as shown below

$$V_{mfc}(s) = \frac{V_{fc}(s)}{l_{1fc}c_{1fc}s^2 + r_{1fc}c_{1fc}s + 1} - V_{cfc}(s) \quad (6)$$

This variable change ensures limiting of inrush currents at the start of converter. The resulting model is given by (5).

The converter model presented by (5) is a third order system. In order to ensure the flat response PI+CI controller requires a first order system of the form (2). Therefore a reduction of this third order system is proposed so that the effective system seen by the controller is first order. This done by introducing a filter (F) as shown in Fig.3 in FC current loop. The converter transfer function for the component values shown in Fig.4 is given by

$$G1(s) = \frac{I_2(s)}{V_{m2}(s)} = \frac{s + 35.70 \pm 1800i}{(s + 87.1)(s + 38.20 \pm 2070i)}. \quad (7)$$

A filter F(s) is then designed to cancel the complex conjugate zeros and poles of *G1(s)* as shown by

$$F(s) = \frac{s + 38.20 \pm 2070i}{s + 35.70 \pm 1800i} \quad (8)$$

such that the controller sees a effective first order system P_{red} given by

$$P_{red}(s) = G1(s) \cdot F(s) = \frac{1742}{s + 87.1}. \quad (9)$$

$$I^2_{fc} = \frac{V_{fc}(s) - (l_{1fc}c_{1fc}s^2 + c_{1fc}r_{1fc}s + 1)V_{cfc}(s)}{l_{1fc}l_{2fc}c_{1fc}s^3 + c_{1fc}(l_{1fc}r_{2fc} + l_{2fc}r_{1fc})s^2 + (c_{1fc}r_{1fc}r_{2fc} + l_{1fc} + l_{2fc})s + (r_{1fc} + r_{2fc})} \quad (4)$$

$$G1(s) = \frac{I^2_{fc}}{V_{mfc}(s)} = \frac{c_{1fc}l_{1fc}s^2 + c_{1fc}r_{1fc}s + 1}{l_{1fc}l_2c_{1fc}s^3 + c_{1fc}(l_{1fc}r_{2fc} + l_2r_{1fc})s^2 + (c_{1fc}r_1r_{2fc} + l_{1fc} + l_{2fc})s + (r_{1fc} + r_{2fc})} \quad (5)$$

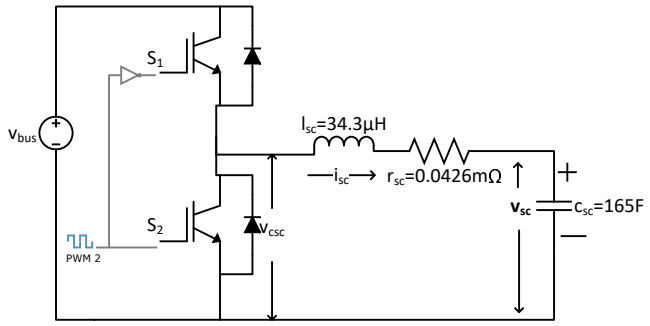

Fig. 5. Schematic of SC DC-DC converter

The controller will therefore be designed using system model given by(9). First the values k_p^{fc} and k_i^{fc} (k_p and k_i gains for the PI+CI controller in FC current loop shown in Fig.1) are calculated by considering the controller as standard PI without reset. Based on this the k_p^{fc} and k_i^{fc} are calculated to be 0.03316 and 19.39 respectively for a settling time of 0.055s and overshoot of 28% which will be flattened out by the reset control. The value of ρ_r is then calculated using (3) and obtained as 0.4889.

3.2 SC converter modelling and controller design

The Fig.5 shows the bi-directional DC-DC converter for interfacing SC to DC grid. The gate signals for IGBTs S_1 and S_2 are always complementary to ensure that the output voltage is not shorted by the converter leg. The modelling of SC converter is done considering the average voltage across S_2 as V_{csc} and neglecting the higher order switching ripples just like the FC converter. The resulting model is given by

$$G2(s) = I_{sc}(s) = \frac{V_{csc}(s) - V_{sc}(s)}{sl_{sc} + r_{sc}} \tag{10}$$

As is the case with FC converter a variable change is proposed as given by

$$V_{msc}(s) = V_{csc}(s) - V_{sc}(s). \tag{11}$$

The resulting model of the SC converter is therefore,

$$G2(s) = \frac{I_{sc}(s)}{V_{msc}(s)} = \frac{1}{sl_{sc} + r_{sc}}. \tag{12}$$

The SC converter presents a first order system and as such the controller design is straightforward. The k_p^{sc} and k_i^{sc} are calculated by considering the controller as standard PI without reset. The SC current loop was designed faster than the FC loop for a settling time of 0.003s with resulting k_p^{sc} and k_i^{sc} values to be 0.4825 and 216.2 respectively. The resulting overshoot was 17%. The ρ_r calculated using (3) was obtained to be 0.4.

3.3 Voltage regulation loop design

The voltage regulating loop forms the outer loop in the SC control as mentioned before. This loop will be designed with slower dynamics compared to the inner SC current loop. The voltage regulating loop is tasked with maintaining the bus voltage (v_{bus}) at nominal value (80 V in this case) under load variations. Therefore the controller for this loop is mainly meant to function as a disturbance rejecting controller. The voltage control loop is shown in Fig.3. The inner SC current loop is designed to be very fast compared to voltage loop

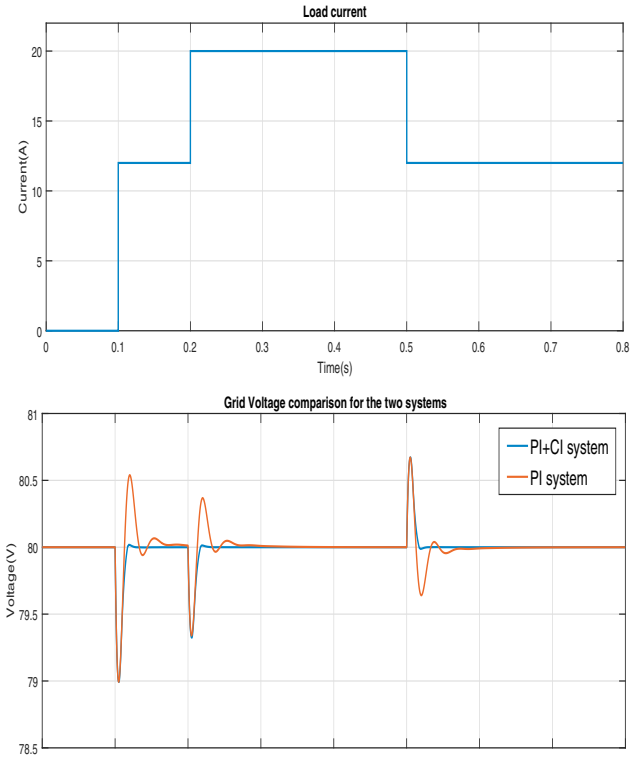

Fig. 6. The load profile introduced to DC grid (top) and comparison of grid voltages for PI+CI and PI based system under load variation (bottom).

making resulting output current from SC converter as steady state values seen by voltage loop. This results in the voltage loop seeing only the capacitance shown as *Grid* in Fig.3. Therefore, the plant for this loop is effectively an integrator. The design procedure for the PI+CI reset control for this voltage loop is done differently compared to the current loops since the major function here is disturbance rejection. As with the case of step tracking the disturbance rejection response is not flat with the PI+CI controller. Nevertheless the controller is still capable of better performance over the PI controller as shown in Baños and Vidal (2012); Baños and Davó (2014). The controller design is done as follows. First k_p^{bus} and k_i^{bus} are calculated considering the controller as standard PI without reset. They are designed to have a settling time of 0.6 s for disturbance rejection. Since the proposed control loop presents a system with integrator in it, the ρ_r value is chosen to be 1 as suggested in Baños and Vidal (2012).

4. RESULTS AND DISCUSSION

The simulation results for the proposed controller will be presented here. The performance of PI+CI controller will be compared with that of the system controlled by the PI controller to highlight the improvement in performance achieved. The simulation was done with the average model of the whole system developed in MATLAB Simulink. The Fig.6 shows current drawn from the grid under varying load profile (top) and the comparison of the DC grid voltage profile under the load variation for a system employing a PI+CI controller and PI controller (bottom). It can be noticed from Fig.6 that when the load variation is introduced in both systems there is a deviation in grid voltage until the first instance of zero error (nominal value). After this the reset action introduced by the reset con-

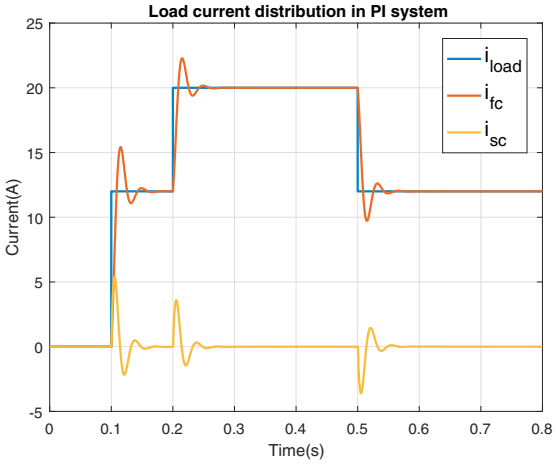

Fig. 7. Load current distribution among The FC and SC for the PI based system

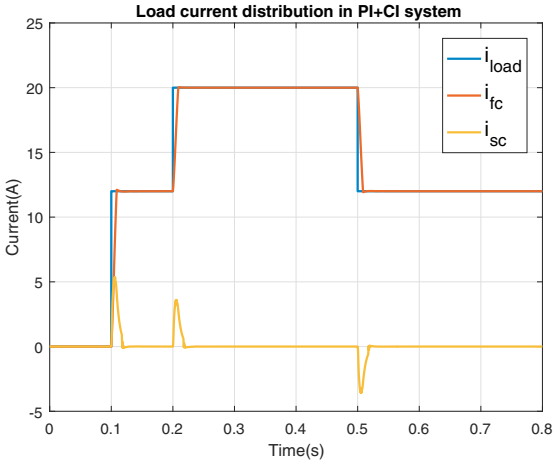

Fig. 8. Load current distribution among The FC and SC for the PI+CI based system

troller of the voltage regulating loop ensures that grid voltage remains at the nominal value bringing the system controlled by PI+CI controller into steady state. In comparison the PI based systems as can be seen in Fig.6 takes a longer time to settle with more ringing in the grid voltage. This represents a clear improvement in voltage regulation performance achieved by reset PI+CI controller.

The Fig.7,8 represent the distribution of load current among the different ESS for system with PI and PI+CI controller respectively. The FC delivers major portion of the load current in both cases and the SC supplies the demanded load current when the FC ramps up in power. It can be seen from the comparison in Fig.7 and 8 that the overshoot in the current delivered by the FC and SC converters are avoided using the PI+CI controller. The flat response achieved by the reset controller is clearly visible in Fig.8.

The Fig.9 and Fig.10 shows the control action of the controllers used in the voltage regulating loop of the SC converter and the current loop of the FC converter respectively. The figures compare the control action for PI and PI+CI controller along with error signal (for PI controller) for both voltage and current

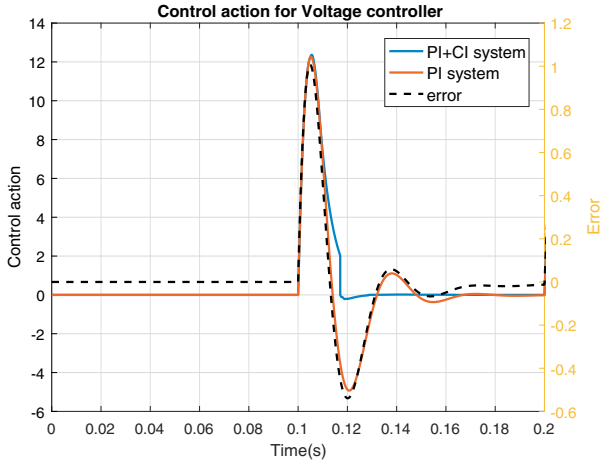

Fig. 9. Control action for the voltage regulating controller

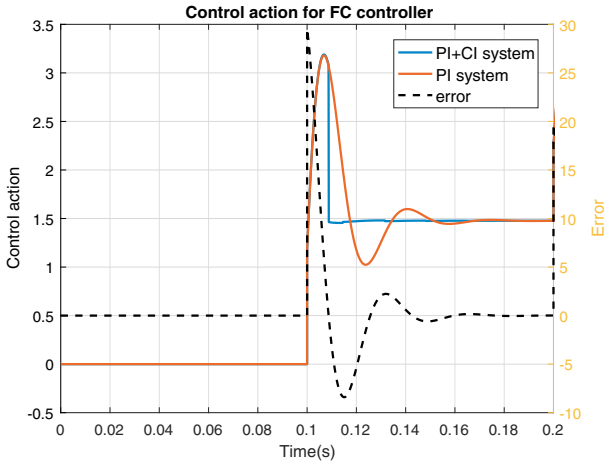

Fig. 10. Control action of the current control for FC loop

loops. The sharp reduction in the controller output for PI+CI caused by the reset action at zero error is visible in both figures.

5. CONCLUSION

The improvement in grid control performance obtained by the PI+CI controller is evident from the simulation results presented in this work. The performance achieved by the PI+CI reset controller is impossible with standard PI controller. Another major advantage with the PI+CI controller was that the design procedure is relatively simple and achieved with simple analytical equations as discussed above. Therefore additional complexities are not incurred in design and implementation of such converters. The main objective behind the formulation of this paper was to highlight the applicability of such reset controllers in grid connected system and improvement in performance that can be brought about by them. Grid connected systems are required to respond fast with minimum overshoot to maintain the system parameters within prescribed limits. To this extent this work has been able to highlight the improvement that can be brought about by reset controllers. The controllers where designed to respond as fast as possible and in comparison to PI controller has provided faster regulation and settling of the grid voltage under load variations, thereby proving the suitability of such controllers in grid connected application.

As for future work there is scope for more work in this area. The first step will be implementing this work into lab prototype and analysing the system performance under the influence of switching ripples introduced by the converters. More stress can be be given in future work on the deeper analysis of robustness and stability issues of such controller when applied to grid connected systems.

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