Enhanced Systematic Design of a Voltage Controlled Oscillator using a Two-Step Optimization Methodology

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***Abstract*—In this paper a design strategy based on bottom-up design methodologies is used in order to systematically design a voltage controlled oscillator. The methodology uses two computer-aided design tools: AIDA, a multi-objective multi-constraint circuit optimization tool, and SIDe-O, a tool that characterizes and optimizes integrated inductors with high accuracy (around 1% when compared to electromagnetic simulations). By using such tools, the difficult trade-offs inherent to radio-frequency circuits can be explored efficiently and accurately. Furthermore, with the capability that AIDA has at considering process parameter variations during the optimization, the resulting methodology is able to obtain truly robust circuit designs.**

Keywords—radiofrequency; process parameter variations; multi-objective optimization; voltage controlled oscillator; integrated inductors modeling

I. INTRODUCTION

First-pass fabrication success has always been a constantly-pursued, yet difficult-to-attain, aspiration for the integrated circuit (IC) designer. By ensuring a first-pass success, the designer avoids costly re-design cycles and post-fabrication tuning work [1], which considerably decreases the efficiency of the design process. Radiofrequency (RF) circuits are among the most difficult ones to ensure first-pass fabrication success due to their complexity and high operation frequencies. In the last few years, there have been tremendous advances in RF technologies, pushing forward the state-of-the-art with higher operation frequencies and improved circuit performances, enabling technologies such as 5G [2]. Therefore, the design of such RF circuits is nowadays very defiant and challenging, pushing the RF designer to its limit.

Nowadays, designers use an established manual design procedure that relies on their own experience. In traditional and manual design approaches, the designer follows an iterative procedure to size each active and passive device in the circuit, as in [3]. Additionally, in this type of design procedures, analytical equations that describe the basic circuit behaviour are commonly used. This set of equations is specifically derived for each circuit topology, limiting their general use. Moreover, this kind of design approach also presents the following drawbacks. Firstly, the analytical expressions used to model the circuit performances and the impact of the device physics are usually too simplified (to be of any practical use), and, hence, inaccurate. Secondly, passive devices such as, integrated inductors, are very difficult to model and most analytical models do not present a reliable characterization. Thirdly, the device extreme performances (e.g., process corners) are usually not taken into account on a first design iteration, and are only considered after a functional nominal design is reached.

Due to the abovementioned issues, it is clear why these manual design strategies usually need to be refined by a considerable number of design iterations. Therefore, in order to avoid these iterations and speed up the design process, new systematic approaches are required to reduce the development cycles of RF circuits.

In this sense, evolutionary computation techniques have been applied to the design of RF circuits in recent years [4]-[7]. The use of optimization-based methodologies tries to overcome the traditional knowledge-based methodologies by using optimization algorithms that automatically explore the design space in order to find optimal designs. However, most optimization-based methodologies still use inaccurate inductor models, such as analytical models (e.g., the π-model in [8]), and most of them do not consider process parameter variations during optimization, drastically reducing the possibility of achieving robust designs.

In order to accurately model highly sensitive passive components, such as integrated inductors, designers aiming for high performance designs typically rely on electromagnetic (EM) simulators. Some approaches integrate these accurate simulations into optimization-based methodologies [4][9]. In these approaches, the optimization loop becomes computationally intensive due to the EM simulations, and, therefore, the efficiency of the design process dramatically deteriorates. Alternatively, relying on inductor libraries provided by the foundries [6], overcomes the efficiency problem. However, these libraries offer limited inductor choices and, therefore, reduce the possibility of finding an optimal inductor for a given application. Alternately, lumped-element models (e.g., the π-model [8])

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relating performance parameters with the inductor geometric parameters can provide a wide range of inductor choices on a reasonably efficient evaluation time-cost. Unfortunately, these models are not entirely accurate, especially at high frequencies [10].

In this work, an optimization-based approach is adopted to systematically design a voltage-controlled oscillator (VCO) [11], where the passive component problem is tackled by using a state-of-the-art surrogate modelling technique that provides less than 1% error when compared with EM simulations. Furthermore, by considering extreme corner performances for each candidate design during the optimization, robust designs are achieved.

The remainder of this paper goes as follows. Section II describes the basics of VCO design and their design parameters, as well as the most relevant performances, illustrating the problems faced in manual-design strategies. Section III presents an automated corner-aware design approach, and, Section IV presents experimental results. Finally, conclusions are drawn in Section V.

II. Voltage Controlled Oscillator Design Insights

The VCO is a circuit whose oscillation frequency is controlled by an input voltage. From the several VCO topologies available, in this work a cross-coupled double-differential VCO is considered, as depicted in Fig.1. In order to have an oscillation, a negative resistance must be generated to compensate the parasitic resistance of the VCO tank (formed by the capacitor, *C,* and inductance, *L*). In the circuit presented in Fig. 1, both the PMOS and NMOS transistors are used to provide sufficient negative resistance to make the oscillator operate uninterruptedly. This LC-VCO topology shows good phase noise performance as well as low power consumption [3]. From the available voltage and current biasing techniques, the current one is selected in this work due to its lower power consumption [3].

In this specific topology, there are 16 initial design variables: the p-type and n-type MOS transistors' dimensions (w_{n1}, w_{p1}, l_{n1} and l_{p1}), the geometric parameters of the integrated inductor (number of turns n, inner diameter D_{in}, turn width w and spacing between turns s), the varactor dimensions (w_{var} and l_{var}), the capacitor value (C), the dimensions of the transistors used to bias the circuit (w_d, w_{dd}, l_d and l_{dd}), and also, the bias current (I_{Bp}).

Typically, the most important performance parameters in VCO designs are the oscillation frequency (f_{osc}), the phase noise (PN), the frequency tuning range, the power consumption (P_{DC}), the output voltage swing (V_{OUT}), and also, the circuit area, which is extremely important as it directly relates to the manufacturing cost in IC technologies. Based on the desired performances, a design strategy must be considered.

In order for a VCO to oscillate properly, the designer has to guarantee that the negative resistance (given by the MOS transistors) is higher than the resistance imposed by the tank (mainly by the inductor). Therefore, an established rule-of-thumb is that the following condition, the so-called start-up condition, is reached:

$$g_{active} \geq \alpha \times g_{tank} \tag{1}$$

where g_{active} and g_{tank} are the transconductance of the MOS transistors and the tank loss, respectively, and α is a constant value, often between 2 and 4. The oscillation frequency f_{osc} is given by:

$$\frac{1}{\sqrt{LC_{max}}} \geq f_{osc} \geq \frac{1}{\sqrt{LC_{min}}} \tag{2}$$

where L is the inductance and C_{min} and C_{max} are the tank minimum and maximum capacitance, which vary due to the varactors.

Apart from f_{osc}, which does not need special design techniques, other performances that must be considered demand special design techniques, such as the minimization of phase noise or power consumption [3]. These strategies are not trivial and require some specific design procedure and a great deal of tweaking that comes of the expert knowledge from the designer. One of the most common design strategies that usually fulfils both, phase noise and power specifications, can be summarized as follows. The designer must find the minimum inductance that satisfies both the start-up condition and the output power. Then, the maximum bias current allowed by the design specifications is chosen. This will ensure the maximization of the output swing and the minimization of the phase noise. Furthermore, the tank capacitance also introduces a trade-off in the design, where large capacitances improve the phase noise but reduce the tuning range [3][12].

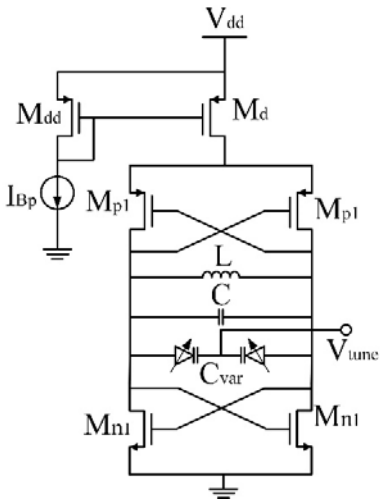

Fig. 1. Cross-coupled double differential VCO topology.

In summary, the design of such VCOs is not trivial and, frequently, re-design iterations are needed in order to achieve the desired specifications. Moreover, in these traditional design methodologies, adopted by the majority of RF designers, the corner simulation is only performed after the sizing task is completed. Therefore, this introduces even more discrepancies, which leads to even more re-design iterations between circuit sizing and final tape-out, due to the fact that

the impact of the devices' extreme corner performances is in most times harsh. Therefore, in order to solve the re-design issues, an optimization algorithm that searches for optimal designs can be considered. Also, in order to obtain more robust designs, a corner analysis can be included during the optimization using a corner-aware approach.

III. VCO Systematic Design

A. Optimization Approach

The systematic design of any given circuit can be mathematically formulated as (for a maximization problem):

$$\begin{aligned} &\text{maximixe } F(x); \qquad F(x) = \left\{ f_1(x),..., f_n(x) \right\} \\ &\text{such that } G(x) \geq 0; \quad G(x) = \left\{ g_1(x),..., g_m(x) \right\} \qquad (3) \\ &\qquad \text{where } x_{Li} \leq x_i \leq x_{Ui}, i \in [1, p] \end{aligned}$$

where x is a vector with p geometric parameters, each design parameter being restricted between a lower limit (x_{Li}) and an upper limit (x_{Ui}). The functions $f_j(x)$, with $1 \leq j \leq n$, are the objectives that will be optimized, where n is the total number of objectives. The functions $g_k(x)$, with $1 \leq k \leq m$, are design constraints which can be defined independently for each optimization problem. When only one performance is minimized or maximized (n=1) the problem can be solved with a single-objective optimization algorithm. When two or more conflicting objectives are minimized/maximized (n>1), a multi-objective optimization algorithm can be used if a set of solutions showing the trade-offs between the different optimization objectives is desired. In the multi-objective case, a solution a is said to constrain-dominate solution b if and only if a has a smaller constraint violation than b, or, if all constraints are met, $f_i(a) \leq f_i(b)$, for every $i \in \{1,...,n\}$ and $f_j(a) < f_j(b)$ for at least an index $j \in \{1,\ldots,n\}$. A point $y \in \Omega$ is Pareto-optimal if it is not dominated by any other point in Ω. The set of all the Pareto-optimal solutions is the Pareto Set (PS). The set of all the Pareto-optimal objective vectors is the Pareto-optimal front (POF).

These optimization problems can be solved by an iterative loop involving an optimization algorithm that generates new candidate solutions at each iteration, and, an evaluator that provides the necessary information to compare and rank solutions.

B. Design Methodology

The core of any systematic circuit design flow is an optimization algorithm linked with an RF circuit performance evaluator such as EldoRF or SpectreRF. At each iteration, the optimization algorithm searches the design space (defined by the circuit design variables of the circuit, as the ones described for the VCO of Fig. 1) for optimal solutions, while several testbenches with several different analyses can be performed to obtain the circuit performances (e.g., f_{osc}, PN, etc.). In most common methodologies, the inductor performances are given either by a π-model [7], EM simulations [9] or inductor libraries provided by the foundries [6]. Also, the inductor performances are usually generated during the optimization loop (see Fig. 2 for the example using the π-model).

However, a different methodology, shown in Fig. 3, is used in this work. The first step of the methodology consists in the generation of the inductor POF (discussed in the next Sub-Section). In the second step of the methodology, an optimization algorithm linked with a RF circuit performance evaluator is used to maximize/minimize one or more objectives under a set of constraints.

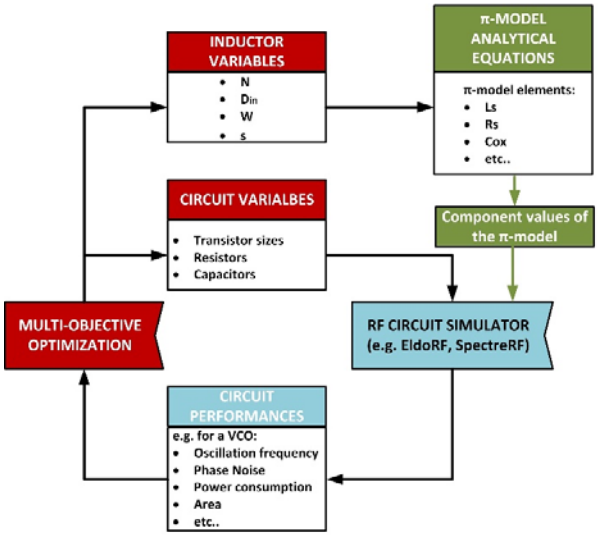

Fig. 2. Flow diagram of a typical circuit optimization methodology. In this flow, the inductors are evaluated with a π-model and the circuit is later simulated with any common RF circuit simulator.

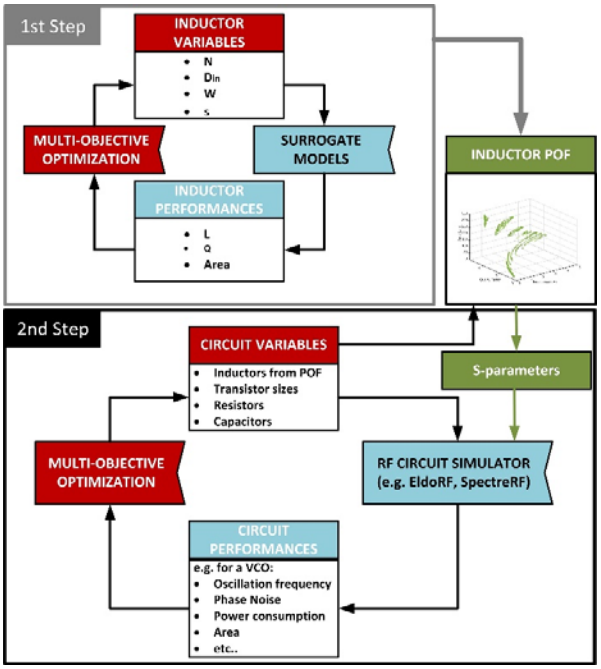

Fig. 3. Flow diagram of the enhanced two-step optimization methodology. In this flow, the first step is performed by SIDe-O tool and the second step is performed by AIDA tool.

The main difference to traditional approaches, is that in this approach the inductors are selected from a previously generated POF rather than using its geometric variables to

calculate the inductor performances within the VCO optimization loop. Furthermore, the inductor performances are incorporated into the circuit evaluator as S-parameter matrices.

C. Inductor POF Generation

In this work, the accuracy and efficiency of surrogate modeling approaches is exploited. Therefore, in order to generate the inductor POF, SIDe-O is used [13]. This toolbox is based on surrogate models that allow an accurate characterization with less than 1% error when compared with EM simulations [14]. Furthermore, SIDe-O is also very efficient, drastically reducing the simulation time of inductors (on approximately three orders of magnitude when compared with EM simulations). This fact is extremely important especially when optimization loops are carried out, where typically thousands of inductors are evaluated.

In Fig. 4, an octagonal symmetric inductor is presented, which is later going to be used in the circuit under study in this work. The geometry of this planar spiral inductor is usually defined by four geometric parameters: number of turns (N), the inner diameter (D_{in}), the turn width (W) and the spacing between turns (S). Several different modeling strategies were considered for the accurate modeling of integrated inductors [10]. However, the most accurate strategy, which is used in SIDe-O, is discussed in detail in [14].

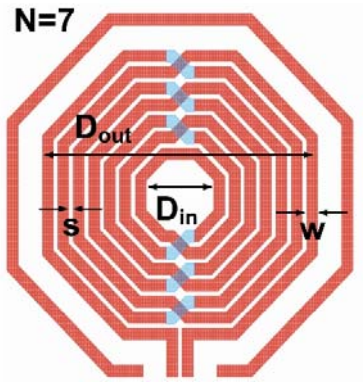

Fig. 4. Inductor geometric parameters for an octagonal symmetric spiral inductor.

While being optimized, the inductors have to be subject to several constraints in order to guarantee their proper behaviour at the entire frequency band. These constraints are also used to take into account the unavoidable manufacturing variations. The constraints are:

$$\begin{cases} area < 400\mu m \times 400\mu m \\ \left|\dfrac{L_{@WF} - L_{@WF+0.05GHz}}{L_{@WF}}\right| < 0.01 \\ \left|\dfrac{L_{@WF} - L_{@WF-0.05GHz}}{L_{@WF}}\right| < 0.01 \\ \left|\dfrac{L_{@WF} - L_{\text{at 0.1GHz}}}{L_{@WF}}\right| < 0.05 \\ Q_{@WF+0.05GHz} - Q_{@WF} > 0 \end{cases} \quad (4)$$

where $L_{@WF}$ and $Q_{@WF}$ are the inductance and quality factor at the working frequency (WF). The inductance and quality factor at any frequency can be easily obtained from the S-parameters [15]. The second to fourth constraint in (4) guarantee that the inductance is sufficiently flat up to around the working frequency. The last constraint in (4) guarantees that the maximum of the quality factor is beyond the working frequency and, therefore, the SRF will be still at higher frequencies. Hence, there is no risk that the SRF becomes close to the working frequency even under the presence of process variations.

By using such accurate model (less than 1% when compared to EM simulations), the obtained POF will already consider an accurately-evaluated impact of the inductors parasitic effects at high frequencies, drastically reducing re-design cycles.

D. Inductor Mapping for Hierarchical Circuit Optimization

Special attention is needed for the inductor hierarchical selection when the circuit is being optimized. The inductor POF is a set of inductors. These inductors have some geometrical variables that map to a set of performances (e.g., L, Q and Area). Neither the inductor geometrical parameters or its performances are regularly distributed, thus, it would be difficult to apply the operators (e.g., mutation) used by the optimization algorithms. Therefore, the inductors must be organized in such a way that these operators can operate meaningfully.

Over the years, several representation and ordering strategies have been proposed. In [16], each lower level POFs is represented as one integer index and the neighbourhood for each solution is pre-computed, to ensure proximity among each solution when applying evolutionary computation operators. In a multi-objective optimization problem with m objectives, the solutions of the POF impose a relationship between these m objectives, and therefore, can be naturally represented by (m–1) parameters. This is the approach followed in [4], where the lower level POF is handled as a pair of integer coordinates that are used to index the inductors in a matrix. This approach has demonstrated to be especially advantageous in hierarchical synthesis of analog circuits, as, unlike in [16], the POF indexes have not to be reordered for each new set of interconnection conditions [17]. Both of these representations take into account the order/performance of the points on the lower level POFs in order to index them. However, although the distance between points is considered for the indexing process, it does not play a role in the selection.

In [18], a method was proposed (the so-called weighted nearest P-neighbourhood with tail, WNNT), that represents the points as one integer, and also considers the distance between points in the performance space, but the novelty is that it defines, for each inductor i, a neighbourhood θ_i of the T closest inductors, and the probability of any point in θ_i being selected as the neighbour of i is inversely proportional to their distance. In addition, the same residual value is assigned to all

points outside θ_i. The probability of inductor j being selected on a neighbourhood of inductor i is inversely proportional to the distance between i and j according to:

$$p_i(j) = \begin{cases} \dfrac{\left(\frac{1}{d_{i,j}}\right)}{\sum_{k\in\theta_i}\left(\frac{1}{d_{i,k}}\right) + 2\cdot\left(\frac{1}{d_{i,P+1}}\right)} & \forall\, j \in \theta_i \\ \dfrac{\left(\frac{2}{(N-P-1)*d_{i,P+1}}\right)}{\sum_{k\in\theta_i}\left(\frac{1}{d_{i,k}}\right) + 2\cdot\left(\frac{1}{d_{i,P+1}}\right)} & \forall\, j \notin \theta_i \end{cases} \quad (5)$$

where $j \in \theta_i$, is the set of T closest elements from solution i, and $d_{i,j}$ is the Euclidean distance from solution i to solution j. Fig. 5 shows the probability for the neighborhood of one of the inductors of a given inductor set. The effects of this inductor mapping technique are studied in the practical example in Section IV.

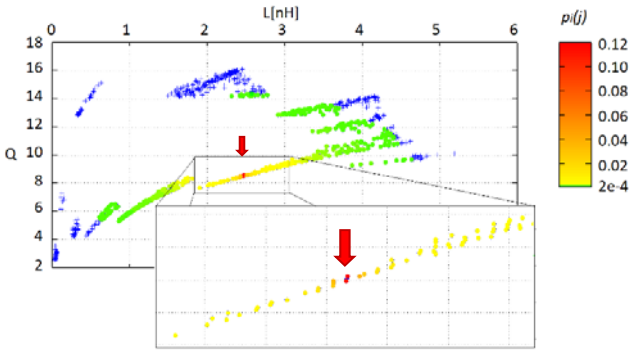

Fig. 5 Illustration of the probability of the inductors in the obtained inductor front being selected by the operator from signaled inductor with the arrow. The inductor set is plotted as a projection of the 3D space *L*, *Q*, and *Area* to *L* and *Q*.

E. Circuit Optimization

For the circuit optimization, AIDA is used [19]. The AIDA automatic analog IC design flow follows the traditional analog IC design steps. Starting from the circuit netlist, created by hand or exported from a schematic editor, several analyses can be performed using different testbenches. The tool links an optimization algorithm with an electrical simulator which is able to predict the performances of a given circuit. AIDA encourages the robustness of solutions at circuit level by providing the possibility of taking into account extreme variations by considering device corners during the optimization.

In AIDA, different optimization strategies can be defined (from single- to multi-objective optimizations and considering different algorithms). However, in this work, we are interested in exploring the different trade-offs inherent to VCOs. Hence, a multi-objective optimization algorithm, the Non-dominated Sorting Genetic Algorithm (NSGA-II) [20], is used in order to obtain a POF. The optimization process and the methodology itself are completely independent of the fabrication technology.

TABLE I
DESIGN VARIABLES FOR THE INDUCTORS USED IN THE VCO.

N		*D_{in}* (µm)		*w* (µm)		*s* (µm)
Min-Max	**Grid**	**Min-Max**	**Grid**	**Min-Max**	**Grid**	**Fixed**
1-8	1	10-300	1	5-25	0.05	2.5

IV. EXPERIMENTAL RESULTS

In this Section, experimental results are shown for the automated design of a VCO in a 0.35µm-CMOS technology.

A. Enhanced Two-Step Circuit Optimization

The first step in the enhanced optimization methodology, is to generate the inductor POF (step 1 in Fig. 3). In order to do so, SIDe-O is used. The design variables of the inductors used to generate the POF are shown in Table I. The inductor area was limited to a maximum square of 400µm x 400µm (a reasonable limit for any practical application). The spacing is fixed to 2.5µm, the minimum allowed by this technology, since no performance improvement is found with larger spacing.

The POF was obtained from an optimization with a population of 1000 individuals and 80 generations, which took around 10 minutes to run (see Fig. 6).

After obtaining the inductor POF, it is possible to proceed to the circuit optimization (step 2 in Fig. 3). The circuit design variables are shown in Table II. The optimization objectives and constraints can be seen in Table III. The circuit is intended to operate at V_{dd}=2.5V. Three analysis need to be performed in order to measure all the desired performances: a periodic steady-state (PSS) analysis, in order to calculate the oscillation frequency f_{osc} and the output voltage swing V_{OUT}, a steady-state noise analysis, in order to calculate the phase noise at different frequencies, and a DC analysis in order to extract the power consumption P_{DC}.

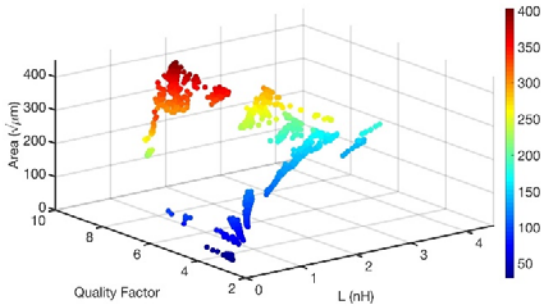

Fig. 6. Inductor asymmetric topology (shown in Fig. 4) POF obtained with SIDe-O.

The optimization results are shown in Fig. 7. The entire optimization took approximately 5 hours to run in an Intel® Core i7-3770 @ 3.4GHz workstation with 32Gb of RAM. It is important to recall that SIDe-O uses a highly accurate surrogate modelling that already incorporates the inductor parasitics at high frequencies. Yet, some performance deviations could still occur due to the usage of a surrogate model. Therefore, as a verification test, all the inductors were EM simulated and the VCOs were re-simulated. It was

TABLE II
DESIGN VARIABLES FOR THE VCO OPTIMIZATION.

Variables	Min	Max	Step
w_{n1} (µm)	10	200	10
$w_{p1,d,dd}$ (µm)	10	150	10
$l_{n1,p1,d,dd}$	Fixed @ 0.35 µm		
I_{Bp} (mA)	0.1	1.5	0.1
w_{Cvar} (µm)	Fixed @ 6.6 µm		
l_{Cvar} (µm)	Fixed @ 0.65 µm		
Inductors	Selected from the POF		
Row_{Cvar},Col_{Cvar} (1)	4	12	1
C (µm)	10.6	76.05	0.05

(1) Row_{Cvar} and Col_{Cvar} are the number of fingers per row and column of the varactors.

concluded that, due to the fact that the surrogate model is so accurate, all individuals still comply with constraints and the VCO performances suffer minimal variations (at *centesimal* level).

TABLE III
DESIRED SPECIFICATIONS FOR THE VCO OPTIMIZATION.

VCO Performance	VCO Specifications
Individuals	256
Generations	250
f_{osc} (V_{tune}= 0 V) (1)	> 2.525 GHz
f_{osc} (V_{tune}= 2.5 V) (1)	< 2.475 GHz
PN @ 10 kHz	< -65 (dBc/Hz)
PN @ 100 kHz	< -92 (dBc/Hz)
PN @ 1 MHz	Minimize < -113 (dBc/Hz)
PN @ 100 MHz	< -134 (dBc/Hz)
P_{DC}	Minimize < 20 mW
V_{OUT}	> 0.15 V
Area (µm²) (2)	Minimize

(1) By applying these constraints we ensure that the VCO covers the target oscillation frequency of 2.5 GHz.
(2) The area of each VCO is approximated as the sum of all device sizes.

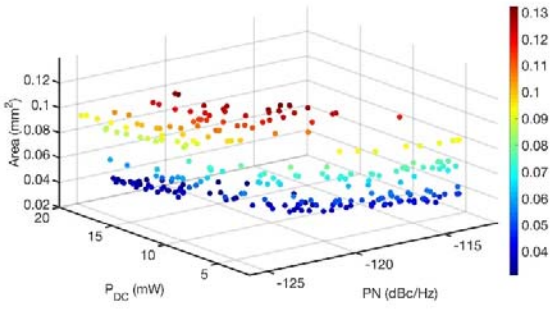

Fig. 7. VCO POF obtained from the enhanced two-step optimization considering only typical corners.

The inductor POF used in the VCO optimization was indexed according to the WNNT technique described in Section III.D. It is interesting to compare the VCO optimization results under the same optimization conditions when the inductor POF is indexed using this method or the matrix mapping (MM) technique reported in [4]. Being stochastic optimization algorithms, ten optimizations with 256 individuals and 250 generations using each inductor mapping technique were executed to perform statistical studies.

In order to inspect the advantages of the used method, the hypervolume and set coverage of each approach were calculated, as shown in Table IV. The hypervolume is calculated as the union of the hypercubes determined by each solution in the objective space and a reference point [21]. The hypervolume metric accounts for convergence and diversity of the Pareto front. As our goal is to compare the Pareto fronts generated with different mapping techniques, and the hypervolume metric depends on the selected reference point, the same reference point is used in all cases. Furthermore, given two solution sets, A and B, the set coverage C(A, B) is defined as the ratio of solutions in B that are dominated by at least one solution in A, e.g., if C(A,B)=1, it means that all solutions in B are dominated by A**.** The motivation to use set coverage is that allows performing binary comparisons between two fronts as the percentage of points of each front dominated by the other one are determined.

From Table IV, it is possible to conclude that the WNNT method systematically has a highest coverage set and also presents a higher hypervolume. Therefore, this justifies the use of this method in this work.

TABLE IV
MEAN AND STANDARD DEVIATION OF THE COVERAGE SET AND HYPERVOLUME OF TEN DIFFERENT POFS USING TWO MAPPING STRATEGIES.

C(A,B)		B				Hypervolume	
		MM		WNNT			
		Mean	SD[1]	Mean	SD[1]	Mean	SD[1]
A	MM	-	-	0.020	0.022	3.84e-8	4.67e-10
	WNNT	0.647	0.120	-	-	4.07e-8	2.73e-10

[1]Standard Deviation

B. *Verification*

Some important aspects of the circuit design were still unconsidered during the optimization above, such as the device corners. Therefore, in order to inspect how damaging could the corner evaluation be to the designs available in the POF, all the VCO designs were re-simulated considering their corners. The following corners were considered: the worst-case power condition (WP), the worst-case speed condition (WS), the worst-case one (WO), where the circuit is designed with fast NMOS & slow PMOS and the so-called worst-case zero (WZ) where the circuit is designed with slow NMOS & fast PMOS.

It was found that from the 256 VCOs designs obtained in the POF from Fig. 7, none of them complied with constraints after being evaluated at corner conditions. In Fig. 8 it is possible to observe the PN vs. P_{DC} projection (of the POF obtained in Fig. 7 in blue crosses) and how the POF was displaced, in red crosses (the area is not affected by the corners). The corner performances depicted are the worst possible for each corner of the design. This means that for the VCO designs depicted with red crosses in Fig. 8 their

TABLE V
DESIRED PERFORMANCES AND SPECIFICATIONS FOR THE VCO OPTIMIZATION. COMPARISON BETWEEN THE TYPICAL CORNER AND WORST CORNER PERFORMANCES.

VCO Performance	Point 1		Point 2		Point 3		Point 4		Point 5	
	Typical	WC[(1)]	Typical	WC[(1)]	Typical	WC[(1)]	Typical	WC[(1)]	Typical	WC[(1)]
f_{osc} (V_{tune}= 0 V) > 2.55 GHz	2.551	2.429	2.553	2.406	2.666	2.511	2.746	2.586	2.556	2.420
f_{osc} (V_{tune}= 2.5 V) < 2.45 GHz	2.325	2.441	2.135	2.262	2.268	2.397	2.372	2.512	2.284	2.415
PN @ 1 MHz < -113 dBc/Hz	-125.1	-122.8	-123.5	-120.0	-119.2	-115.8	-117.4	-114.2	-114.8	-103.7
P_{DC} < 20 mW	17.9	25.9	11.1	14.8	5.1	5.8	6.7	7.4	3.1	3.6
V_{OUT} > 0.15 V	1.83	1.51	1.39	0.98	1.09	0.93	0.75	0.50	0.6	0.16

[(1)]Worst corner performance: in red the ones that fail to meet the constraint and in green the ones that meet the constraint

performances may not be authentic, as the PN value may be due to one corner and the P_{DC} value due to another corner.

Typically, and as expected, the designs have higher phase noises and higher power consumption when simulated in its corners.

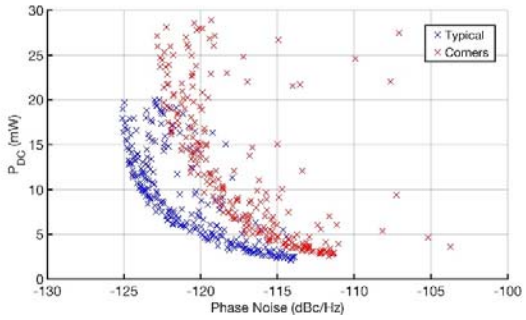

Fig. 8 PN vs. P_{DC} projection of the VCO typical POF (from Fig. 6) compared with the same designs simulated with its corners (worst corner performance depicted).

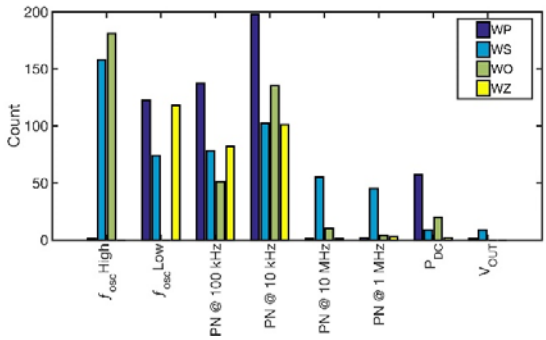

Fig. 9. Histogram showing the number of designs (Y-axis) that fail each constraint at each considered corner.

A more complete analysis of how many designs failed to meet the performances after corner simulation was also performed. The results are shown in Fig. 9. It shows, that the most affected performances by corners are the oscillation frequency and the phase noise nearer the carrier (<100 kHz offset), which correspond to the Flicker (or $1/f$) noise region [22]. This increase in the Flicker noise is most affected due to the WP corner; this seems plausible, since this type of noise is directly related to the direct current flowing through the devices, and therefore its power consumption. Furthermore, in Table V, five points from the typical POF are shown in more detail, with their typical and worst-corner performances. It can be noticed that some of the performances are over-estimated in a pre-corner analysis (e.g., PN) while others are under-estimated (e.g., P_{DC}).

This means that although this approach is already a step forward towards robustness, due to the modelling technique used for inductors, which already incorporates detailed inductor parasitics, it is still not enough. Consequently, in order to increase the solution robustness even more, the device corners must be considered during optimization. This will be studied in the next Sub-Section.

C. *Enhanced Two-Step Circuit Optimization: Considering Device Corners*

In this Sub-Section, an optimization was performed in the same conditions as the optimization in Sub-Section IV.A, but also considering the abovementioned technology process corners. The new optimization was performed simulating all corners for each individual VCO and ensuring constraints on all corners. The obtained POF can be seen in Fig. 10.

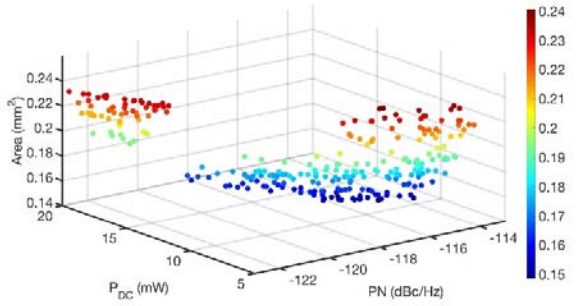

Fig. 10. VCO POF obtained from the enhanced two-step optimization considering all corners (worst corner performances depicted).

The optimization took approximately 10 hours in an Intel® Core i7-3770 @ 3.4GHz workstation with 32Gb of RAM, which is twice the computation effort than the previous optimization presented in Fig. 7, but the obtained POF is much more reliable. It can be concluded that relatively poorer phase noises are achieved with similar power consumptions; however, the biggest price to pay is area, as it seems that the designs usually use larger device sizes in order to comply with the constraints in all corners.

In order to study this issue, the device sizes of the VCOs from the POF considering corners were compared with the device sizes of the VCOs from the POF without corners. The comparisons can be seen in Fig. 11. It is possible to observe that almost every device needs larger area in order to comply with constraints when the corner analysis is considered. This is particularly noticeable in the area of the capacitors and varactors. In order to comply with the tuning range specifications in all extreme corners, the varactors need larger area. Consequently, larger varactors have higher capacitance value, and therefore, in order to maintain the same f_{osc}, the inductance has to be smaller (see Eq. (2)), and this is why the inductors used in the POF considering corners use inductors with only two turns (which typically have lower inductance values than inductors with more turns).

Afterwards, a more detailed analysis of one of the VCOs is also performed (the chosen VCO has the lowest phase noise from the POF shown in Fig. 10). The design was simulated in its typical and extreme corners. The performance variations of the circuit among all these corners can be observed in Fig. 12. This design complies with all design specifications at all corners, and is therefore very robust.

It can be concluded that by using this so-called corner-aware optimization approach, more reliable and robust designs can be achieved compared to the optimization that solely considers the typical device models, bringing the designer closer to a first-pass fabrication success.

V. Conclusions

In this work a corner-aware automated design methodology was applied to the design of a cross-coupled double-differential VCO. The optimizations performed use an enhanced optimization approach that is based on a two-step approach. First, an inductor POF is obtained, which is later used in the second step (circuit optimization) as search space for the inductors used in the circuit. In the circuit optimizations, the device process variations are taken into account by performing corner analysis of the designs. By using such corner-aware methodology assisted by multi-objective optimization algorithms and accurate passive component modeling, the complex trade-offs inherent to RF circuits are efficiently explored and the designs obtained are much more reliable, bringing the designer a step closer to a first-pass fabrication success.

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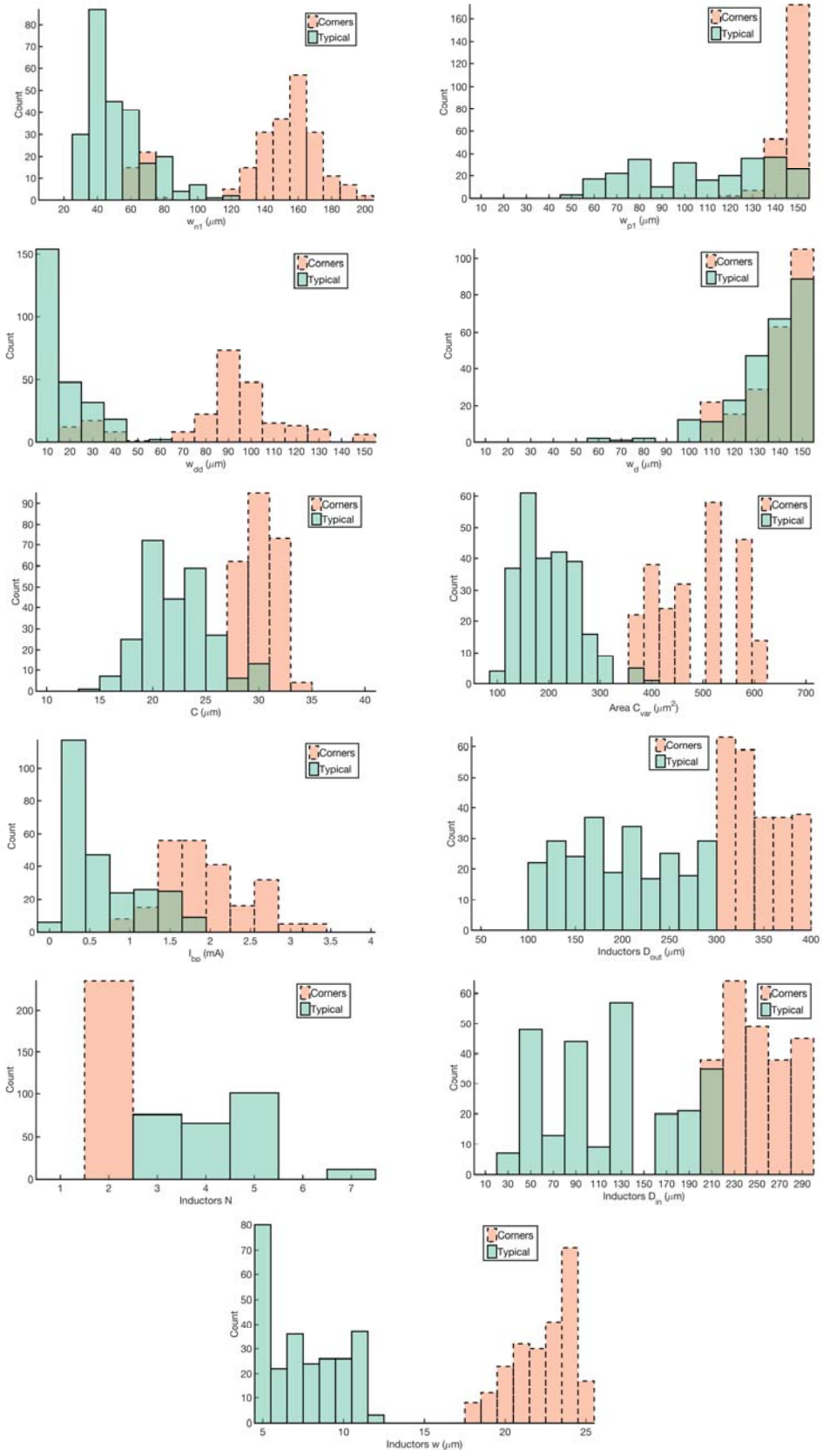

Fig. 11. VCO device sizes from the POF considering corners versus the POF with only typical models.

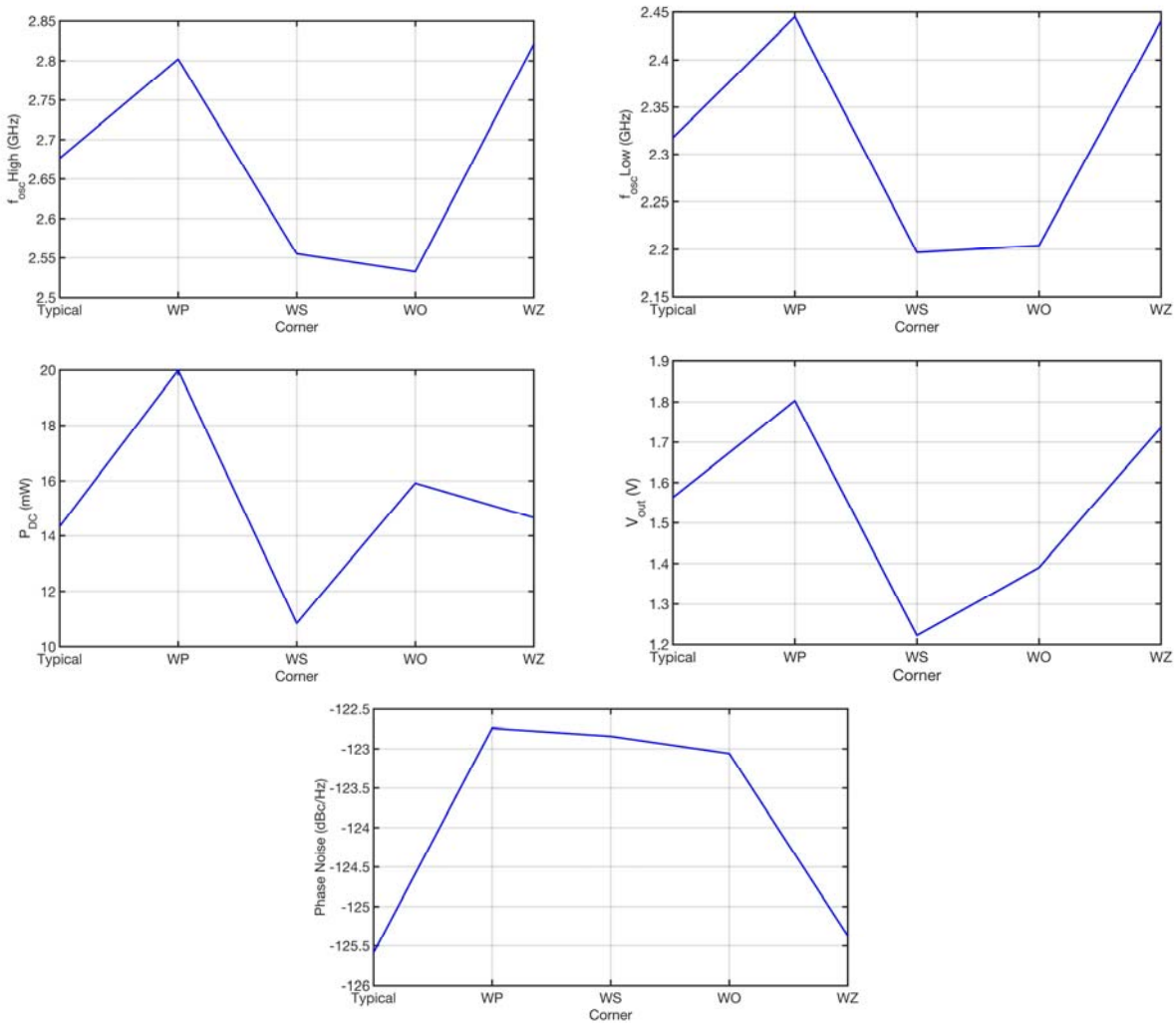

Fig. 12. VCO performance variations for one design of the obtained POF, both the typical and the corner models.