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Abstract

This paper presents a fully-integrated NEMS resonator together with a compact built-in CMOS interfacing circuitry. The proposed low-power CCII circuit allows measuring the mechanical frequency response of the nanocantilever structure in the MHz range. Detailed experimental results at different DC biasing conditions and pressure levels are presented for a real mixed electro-mechanical system integrated through a combination of in-house standard CMOS technology and nanodevice post-processing based on nanostencil lithography. The proposed read out circuit can be adapted to operate the nanocantilever in closed loop as a stand alone oscillator.

1 Introduction

Recently, nanotechnology has become a promising approach to integrate both sensors [1,2] and actuators [3,4] in CMOS technologies. Also, electromechanical devices can save power consumption and silicon area for specific functions compared to their purely electronic counterparts, specially in mobile applications. In particular, the possibility of using nano-electromechanical systems (NEMS) to replace the costly and bulky quartz crystal devices is of high interest for the implementation of integrated oscillators [5,6].

However, in order to take advantage of the emerging nanotechnologies, the resulting nanodevices must be compatible with standard CMOS processing, and specific circuits

have to be developed either for testing these NEMS or simply for their interfacing within the final mixed electromechanical system-on-chip.

This paper presents both, a fully-integrated nanocantilever operable at frequencies in the MHz range, together with a specific low-power and compact CMOS read out circuit for its experimental characterization and interfacing. From a technological point of view, the NEMS fabrication is based on nanostencil lithography [7], while from the design side a new low-power CMOS interface topology is proposed based on second generation current conveyors (CCII) [8]. Finally, the mixed electro-mechanical system is fully integrated through a combination of in-house standard CMOS technology and nanodevice post-processing [9].

Next section introduces a general overview of the mixed NEMS-CMOS system. Then, the modeling of the nanoresonator device is explained in Section 3, while the novel low-power CCII CMOS topology for its interface is proposed in Section 4. Experimental results of the resulting mixed integrated circuit are reported in Section 5, and conclusions are finally summarized in Section 6.

2 NEMS Read Out Scheme

Schematically, NEMS resonators based on nanocantilevers include the main parts shown in Figure 1(a). The device consists of a driver, mechanically anchored, and a cantilever placed very close to the driver and clamped at one end only, so it can freely bend around the static position at a given oscillation frequency.

[Figure 1 about here.]

Following the ideal read out scheme illustrated in the same Figure 1(a), the fixed driver is used to bias the required DC voltage V_{static} (typically between 1V and 20V) and to act as the input terminal for the frequency stimulation V_{osc} (typically from -30dBm to 0dBm). On the other hand, the cantilever acts as the output terminal, allowing the read out of the NEMS resonator output current I_{res} (typically in the nA range) and the corresponding voltage signal V_{meas} across the load resistor R_{load}. The resonance frequency f_{res} (typically from 1MHz to 10MHz) depends on the cantilever material and dimensions, as detailed later on in Section 3.

Unfortunately, the ideal read out scheme of Figure 1(a) is not feasible in practice due to the MΩ range values of the NEMS resonator at f_{res}, which limits the allowed output capacitance C_{load} far below the pF range. Hence, a built-in interface circuit is

required. Several implementations based on the passive integration of I_{res} through C_{par} have been reported in the literature [6, 10, 11]. However, the resulting integration gain is still strongly dependent on the layout parasitics. In order to solve this drawback, the alternative strategy of Figure 1(b) is proposed, where a built-in CMOS CCII is inserted in between the NEMS resonator and the output. This new scheme is equivalent to Figure 1(a) for $V_{static} = V_{bias} - V_{ref}$, but it addresses the previous drawback in two directions: the new resonator output capacitance C_{par} can be easily kept in the sub-pF range as it is no more related with C_{load}, and also its effects are minimized by ensuring a constant voltage bias at the output of the resonator. Furthermore, the proposed CCII interface amplifies I_{res} for either external measurement at V_{meas} or internal feedback to V_{osc} (e.g. stand alone oscillator), as detailed in Section 4.

3 NEMS Resonator

The basis of the fabrication process is described in [10] and consists of post-processing standard CMOS wafers, where a polysilicon area for nanodevice integration has been reserved. However, the novelty here is the lithography technique employed for patterning the nanodevices: an enhanced resolution down to 200nm and full-wafer parallel processing are obtained [9] by applying nanostencil lithography (nSL) [7]. In this new process, and after concluding the fabrication of the CMOS circuits, nanodevice areas are selectively patterned with a 80nm thick aluminum layer by nSL. Subsequent process steps consist on reactive ion etching of silicon to transfer the aluminum pattern to the polysilicon structural layer, wafer dicing and silicon oxide wet etching to release the mechanical structure, combined with a critical point drying process (CO_2 dryer) in order to avoid stiction phenomena. Following this procedure, surrounding CMOS circuits show no degradation of their analog performance.

As a result of the above CMOS post-processing, the polysilicon structure of Figure 2(a) is obtained, where W, L, H and D stand for the cantilever width, length, height and gap to driver, respectively. In our case, typical dimensions for the NEMS device are listed in Table 1.

[Figure 2 about here.]

[Table 1 about here.]

According to [12, 13], the use of continuum mechanics is still valid to predict the mechanical behavior of resonating structures with cross-sectional areas larger than few nm^2. As a result, the analytical expression of the natural (i.e. without any electrostatic force) resonance frequency for undamped (i.e. ideal vacuum) lateral flexion is found to be:

$$f_{res} = \frac{1.015}{2\pi}\sqrt{\frac{E}{\rho}}\frac{W}{L^2} \tag{1}$$

where E and ρ stand for the Young's modulus and the density of the nanocantilever material, respectively. Around the resonance frequency of the considered mode, the nanocantilever moves laterally and its mechanical motion is translated into an electrical signal. In fact, the read out is based on capacitive detection according to:

$$\begin{aligned} I_{res} &= \frac{dQ_{res}}{dt} \\ &= (C_{stat} + C_{mot})\frac{dV_{osc}}{dt} + (V_{bias} - V_{ref} + V_{osc})\frac{dC_{mot}}{dt} \\ &\simeq C_{stat}\frac{dV_{osc}}{dt} + (V_{bias} - V_{ref})\frac{dC_{mot}}{dt} \end{aligned} \tag{2}$$

where C_{stat} and C_{mot} are the static plate and the motion capacitances, respectively. Thus, the NEMS output current is a sum of two contributions: one arising from the static structure (i.e. $C_{stat}\frac{dV_{osc}}{dt}$) and the other coming from the nanocantilever motion itself (i.e. $(V_{bias} - V_{ref})\frac{dC_{mot}}{dt}$). This second part allows the measure of the frequency response of the mechanical resonator.

In practice, either due to air environment or other second order effects, the NEMS resonator can exhibit important losses that translate into a decrease of its quality factor Q. In these cases, the nanomechanical resonator can be described through a small signal equivalent RLC model [5], as depicted in Figure 2(b). The main physical parameters of this model are the cantilever dissipation, mass and elasticity, which are electrically equivalent to R_{res}, L_{res} and C_{res} respectively, and the static plate capacitance C_{stat}. In addition, the cantilever output capacitance C_{cant} and the fringing coupling to the driver C_{coup} are included here, while the driver own capacitance C_{driv} can be neglected according to the read out scheme of Figure 1(b). It is important to note that R_{res} depends on the Q factor, whose theoretical calculation is difficult to obtain. Therefore, R_{res} is estimated from experimental data of Q, as illustrated in Section 5.

4 Current Conveyor Circuit

As already argued, the purpose of the CMOS interfacing circuit in Figure 1 is to ensure a constant bias at the output of the NEMS resonator and to read out its capacitive current. In this sense, the compact CMOS circuit shown in Figure 3 is proposed, which consists of an input low-impedance stage (M1-M4) and an output current scaler (M5-M12).

[Figure 3 about here.]

Firstly, the input low-impedance is achieved by the cascode transistor M4, which is continuously controlled by the telescopic differential amplifier M1-M3. According to the advanced EKV MOSFET model [14], the resulting small-signal input resistance at X is found to be:

$$r_{in} = \left(\frac{1}{n + \frac{gm_{g1}}{gm_{d1}}} \right) \frac{1}{gm_{g4}} \tag{3}$$

where n stands for the subthreshold slope factor. Hence, the error amplifier M1 scales down r_{in} by the gain factor $\frac{gm_{g1}}{gm_{d1}}$ compared to the impedance of the single M4 transistor $\frac{1}{gm_{g4}}$. As a result, this stage generates an input voltage V_X that follows V_Y.

Secondly, the NEMS current sensed by M4 is amplified by the geometry scaling factors $M = \frac{(W/L)_{7,8}}{(W/L)_{5,6}}$ and $N = \frac{(W/L)_{11,12}}{(W/L)_{9,10}}$ of the two-stage cascode current mirrors M5-M8 and M9-M12 biased at V_{casp} and V_{casn}, respectively. In order to reduce the overall power consumption, a K/M fraction of the biasing is subtracted before the second amplification stage.

In conclusion, the proposed circuit qualitatively behaves like a classic CCII- [8], but with an extra gain from the I_X to I_Z signals:

$$\begin{bmatrix} I_Y \\ V_X \\ I_Z \end{bmatrix} = \begin{bmatrix} 0 & 0 & 0 \\ 1 & 0 & 0 \\ 0 & -MN & 0 \end{bmatrix} \begin{bmatrix} V_Y \\ I_X \\ V_Z \end{bmatrix} \tag{4}$$

In fact, the new CCII- topology introduced in Figure 3 is an improvement of the input stage [15] in order to allow a wider voltage range for both V_X and V_Y thanks to the symmetry of the M1 and M2 drain connections. Also, compared to other similar CCII- evolutions like [16], the proposed circuit saves power consumption by minimizing the transistor count of the input stage.

Applying the above circuit model to the general read out scheme of Figure 1, we obtain the final design equations:

$$\Delta V_{meas} = R_{load} M N \Delta I_{res} \quad \text{and} \quad V_{cant} \equiv V_{ref} \tag{5}$$

where V_{cant} stands for the voltage biasing at the NEMS resonator output. The MOS device dimensions for the proposed CCII- are listed in Table 2, while the simulated performance is summarized in Table 3 and illustrated in Figure 4 for a typical set of design values. Thanks to the low transistor count of the proposed CCII-, the CMOS interfacing circuit is compatible with low-power operation and compact integration.

[Table 2 about here.]

[Table 3 about here.]

[Figure 4 about here.]

5 Experimental Results

Following the proposals of Sections 3 and 4, a compact 1.5MHz NEMS resonator together with the CMOS interfacing circuit has been integrated through the in-house standard CMOS double polysilicon technology and the full-wafer post-processing steps based on nanostencil lithography described in [9]. As shown in Figure 5, the resulting size of the complete mixed electromechanical circuit without pads is around $800\mu\text{m}\times400\mu\text{m}$ (0.32mm^2). Since the in-house CMOS technology is a 2.5μm lithography process, a considerably smaller implementation can be obtained using modern submicron CMOS technologies.

[Figure 5 about here.]

Taking advantage of the built-in interfacing circuit, the NEMS resonator has been characterized. In this sense, the typical transfer function of the nanoresonator measured in vacuum is depicted in Figure 6. As it can be easily seen, the NEMS device exhibits a clear and narrow mechanical resonance around f_{res}=1.5MHz, which matches with theoretical estimations within $\pm5\%$, showing important magnitude losses outside this band. The mechanical Q factor is estimated around 8500 in these vacuum conditions. All magnitude transfer functions in this section are normalized to $R_{load}MN/R_{res}$. However, in case of fully integrated closed loop operation (e.g. stand alone oscillator), this attenuation factor

can be compensated up to 0dB by choosing larger M, N and R_{load} design values, as the CCII- load capacitance is then $C_{driv} \ll C_{load}$.

From the Q factor and the V_{bias}-V_{ref} DC biasing of Figure 6, the model parameters of Table 4 are deduced. The validity of the circuit model described in Section 3 has been tested for different cantilever widths, thicknesses and cantilever/driver gaps. Apart from extracting the equivalent RLC parameters, the interfacing CMOS circuit also allowed the experimental study of the nanoresonator under different pressure and biasing conditions.

[Figure 6 about here.]

[Table 4 about here.]

In the first case, different environment pressure levels were applied in Figure 7, returning very good quality factors at vacuum levels below 10Pa, as illustrated in Figure 8. The most pronounced evolution occurs above 10Pa, where the Q factor can be enhanced by three orders of magnitude, while it tends to saturate not far below 10Pa. These results confirm that viscous damping plays a key role regarding the value of the quality factor of nano and microresonators, whereas at low pressure intrinsic loss mechanisms dominate.

[Figure 7 about here.]

[Figure 8 about here.]

Finally, different biasing levels has been tested in Figure 9 using the same circuit. These results fit the dependence of the resonance frequency on the square of the DC biasing, as depicted in Figure 10. The negative slope here corresponds to a classical spring-softening case, which means that the electrostatic effect dominates over mechanical stiffening when applying an electrostatic driving force.

[Figure 9 about here.]

[Figure 10 about here.]

6 Conclusions

A compact NEMS resonator together with its CMOS interfacing circuitry has been successfully integrated and experimentally characterized. The new low-power CCII read out circuit allows detailed measurements in the MHz range of the nanodevice for model extraction

under different pressure and DC biasing conditions. In this sense, the proposed interfacing circuit can be easily adapted (e.g. choosing a larger value for R_{load} and scaling factors) to allow the close loop operation of the nanocantilever as a mixed electro-mechanical stand alone oscillator.

Acknowledgments

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keywords: Low-power, current-conveyor, NEMS, resonator, read out.

List of Figures

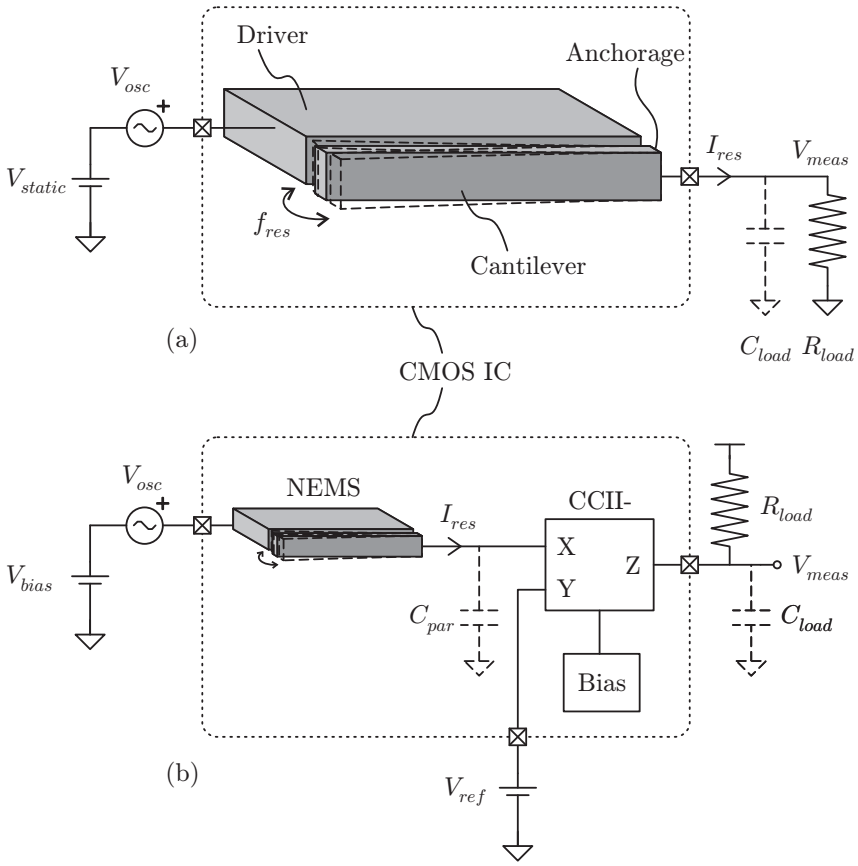

Figure 1: NEMS parts and ideal read out scheme (a), and proposed monolithic CMOS solution (b).

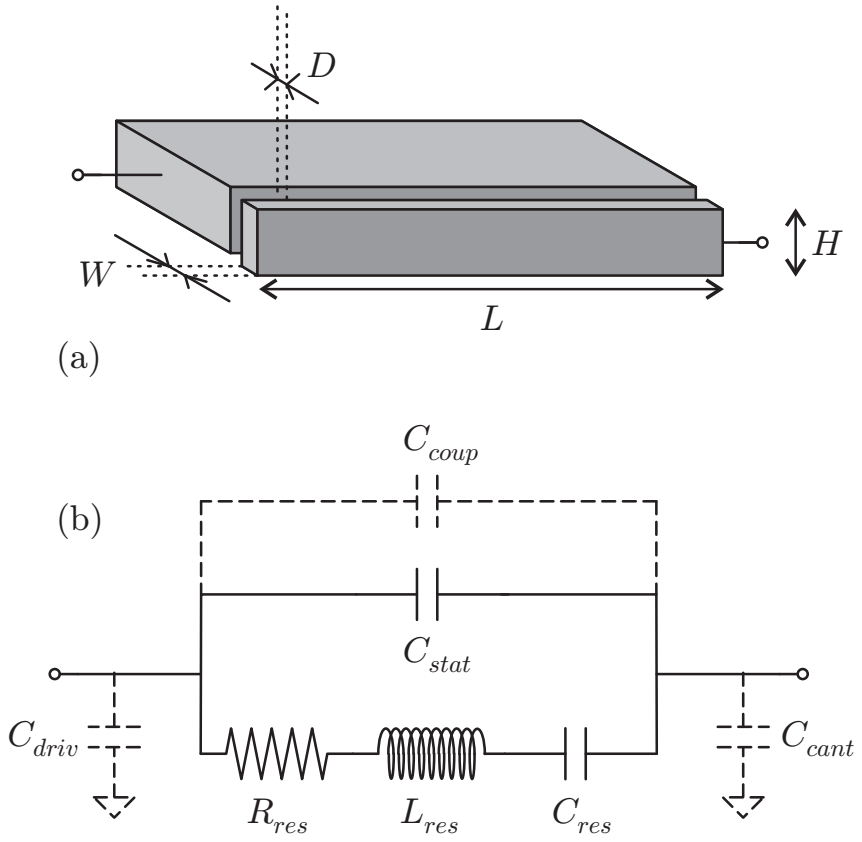

Figure 2: Mechanical (a) and electrical equivalent circuit model (b) of the NEMS resonator. Top drawing not in scale.

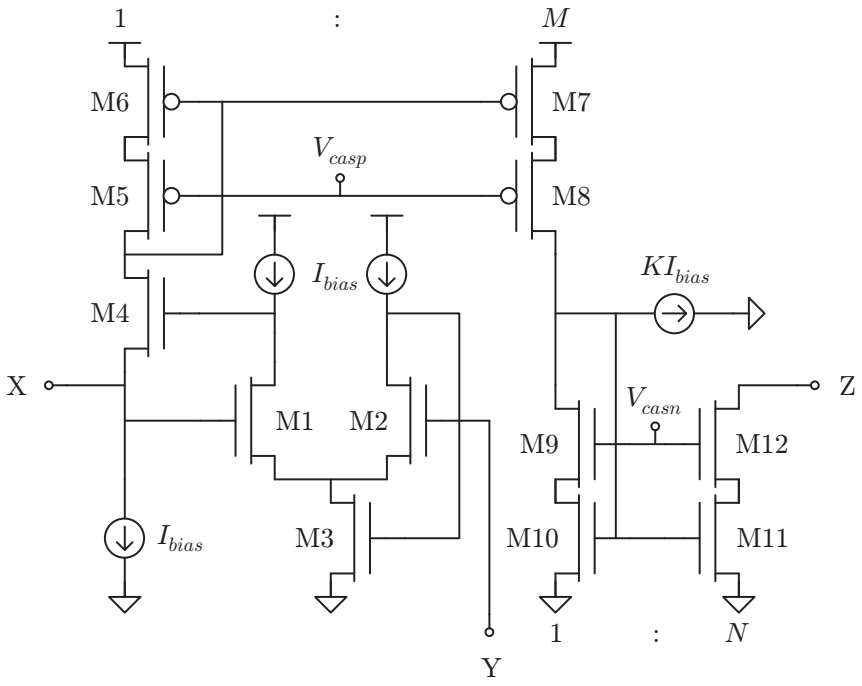

Figure 3: Simplified schematic of the CMOS CCII- circuit.

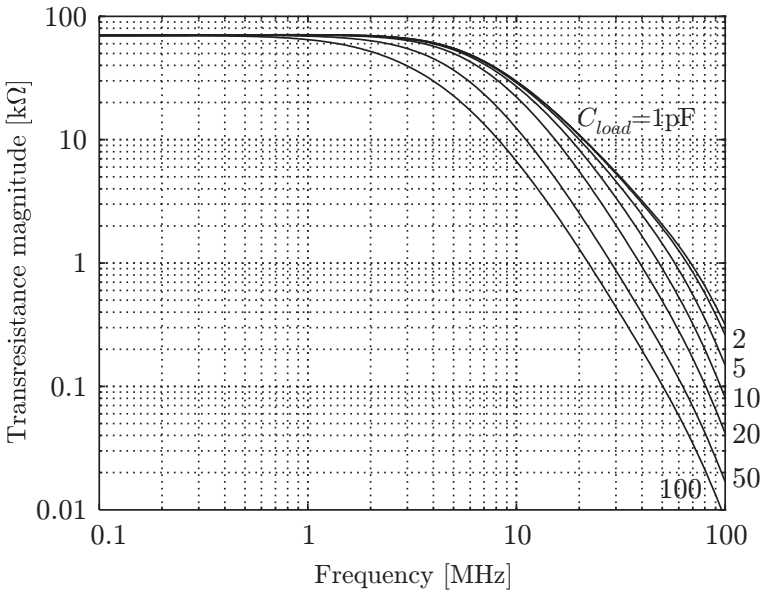

Figure 4: Simulated transfer function of the CCII- circuit of Figure 3 according to the design variables of Table 3 and for different load capacitance conditions.

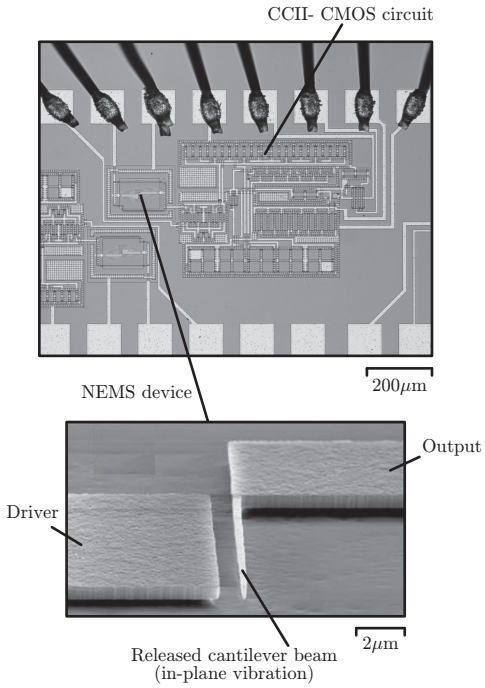

Figure 5: Microscope photography (top) of the mixed NEMS-CMOS circuit and SEM image (bottom) of the NEMS device.

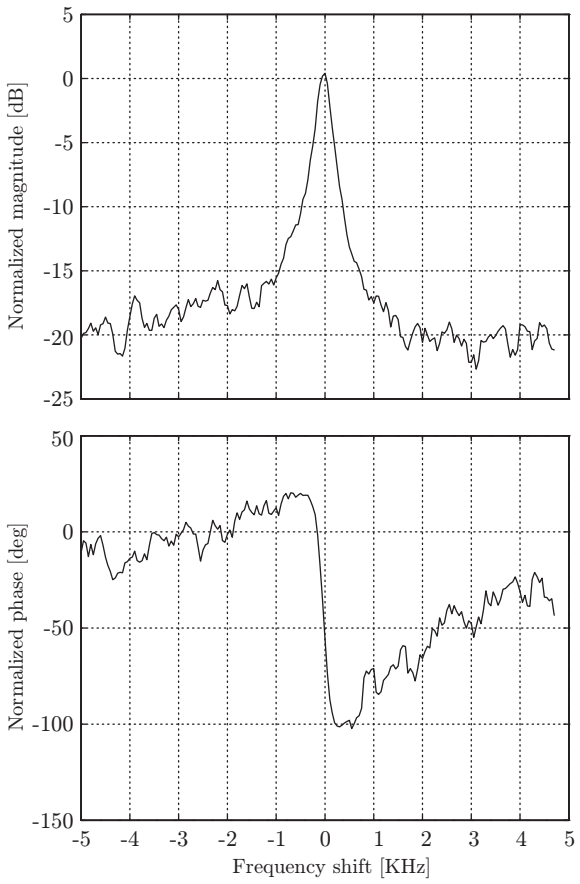

Figure 6: Experimental NEMS transfer function in vacuum (0.9Pa) for V_{bias}-V_{ref}=2V, V_{osc}=-26dBm and $R_{load}MN/R_{res}$=-68dB, resulting in $f_{res}\simeq$1.5MHz and $Q\simeq$8500.

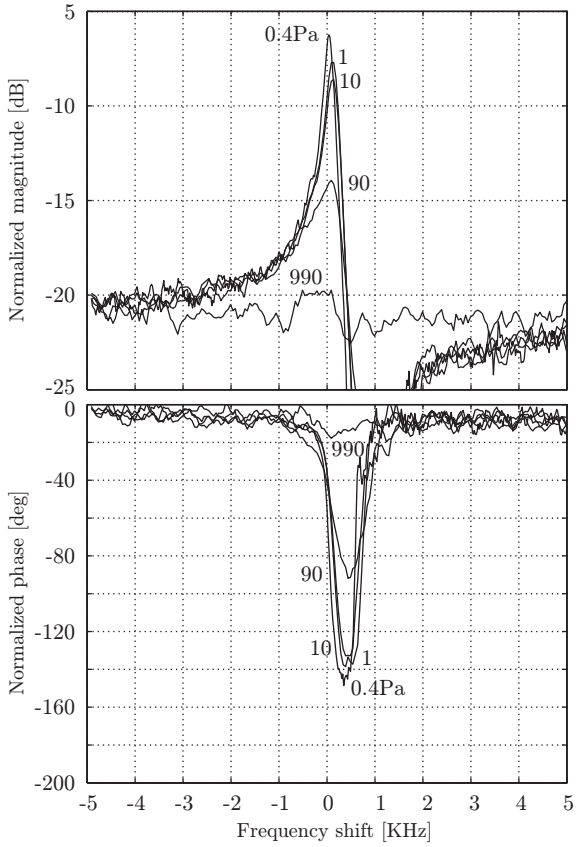

Figure 7: Experimental NEMS transfer function for different vacuum levels and V_{bias}-V_{ref}=1V, V_{osc}=-20dBm, $R_{load}MN/R_{res}$=-76dB and $f_{res}\simeq$1.5MHz.

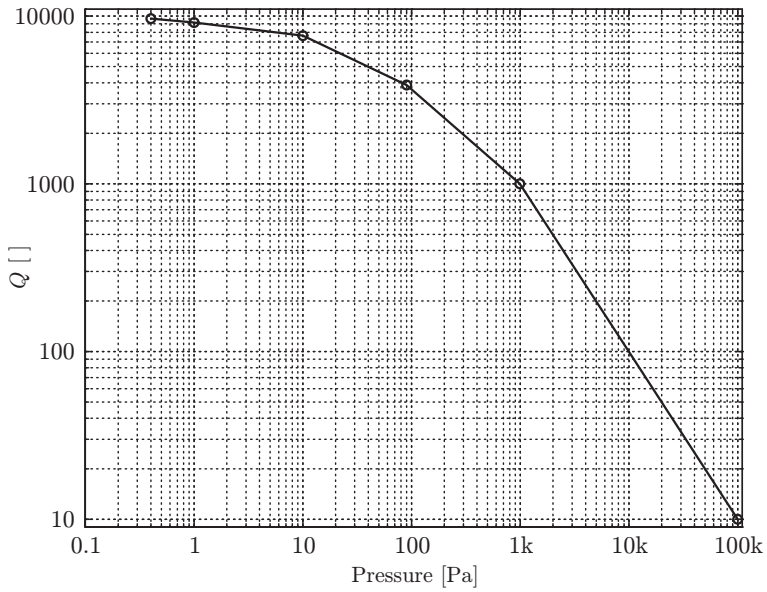

Figure 8: Experimental NEMS quality factor for different vacuum levels, under the same conditions of Figure 7.

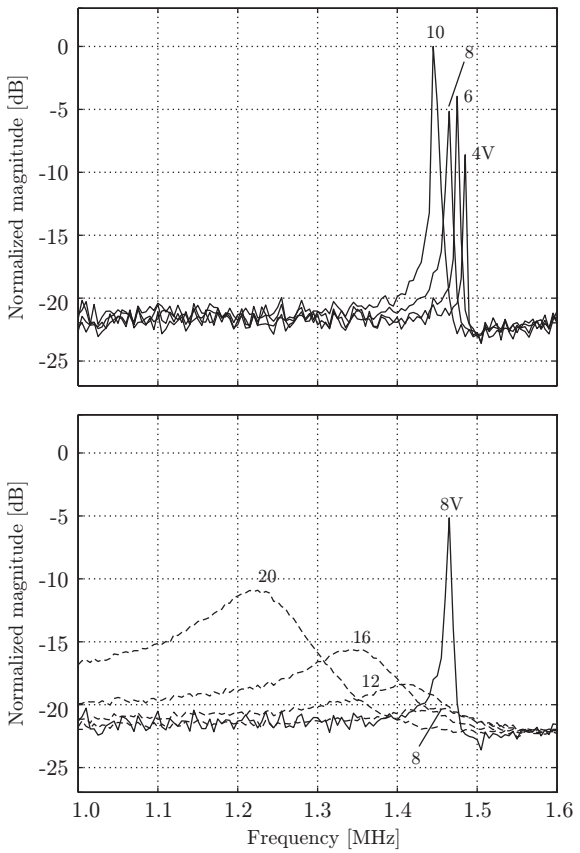

Figure 9: Experimental NEMS transfer function comparisons between vacuum (solid, <5Pa, V_{osc}=-10dBm) and air pressure (dashed, V_{osc}=0dBm) for different V_{bias}-V_{ref} levels. Due to limited frequency resolution, peak values are approximative.

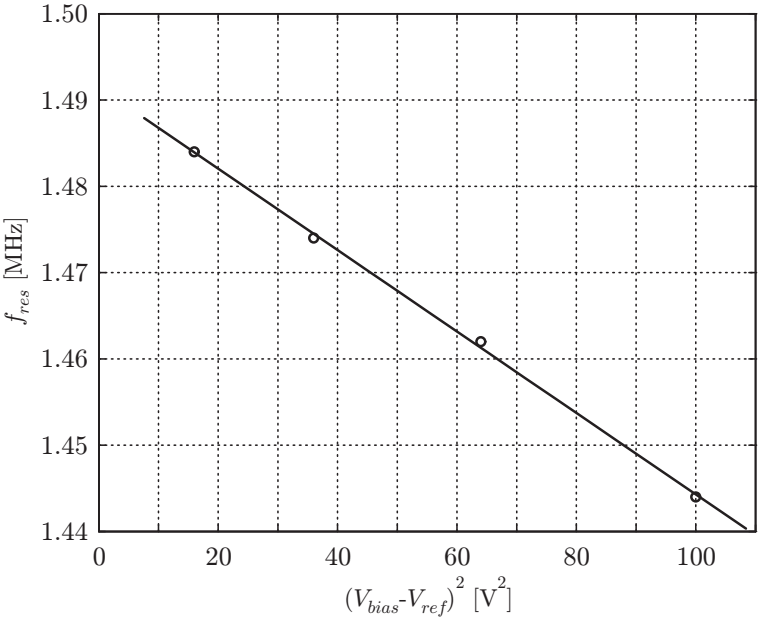

Figure 10: Experimental (circles) and numerical fitting (solid) of the NEMS resonance frequency for different biasing levels (2Pa, V_{osc}=-20dBm).

List of Tables

Parameter	Value	Units
W	260	nm
L	14.5	μm
H	570	nm
D	820	nm

Table 1: Physical dimensions of the NEMS resonator of Figure 2.

Transistor	$\frac{W}{L}$ $[\frac{\mu\mathrm{m}}{\mu\mathrm{m}}]$
M1-2	$4 \times 30/5$
M3	$2 \times 15/10$
M4	$30/3$
M5-6	$10/5$
M7-8	$M \times 10/5$
M9-10	$50/5$
M11-12	$N \times 50/5$

Table 2: Device dimensions for the CCII- of Figure 3

Parameter	Value	Units
Transresistance	70	KΩ
Bandwidth	4.5	MHz
In-band input impedance	<3	KΩ
In-band input current noise	0.5	$pA/\sqrt{Hz}$
Supply voltage	5	V
Current consumption	185	μA

Table 3: Overall performance of the read out circuit for I_{bias}=8μA, M=N=10, K=9, R_{load}=700Ω and C_{load}=30pF.

Parameter	Value	Units
R_{res}	84	MΩ
L_{res}	76	kH
C_{res}	0.15	aF
$C_{stat} + C_{coup}$	90	aF
C_{cant}	$<$50	fF

Table 4: Equivalent RLC parameters extracted from the experimental results of Figure 6.