Electrical characterization of atomic-layer-deposited hafnium oxide films from hafnium tetrakis(dimethylamide) and water/ozone: Effects of growth temperature, oxygen source, and postdeposition annealing

Hector García, Helena Castán, Salvador Dueñas, Luis Bailón, Francesca Campabadal, Oihane Beldarrain, Miguel Zabala, Mireia Bargallo González, and Joan Marc Rafi

Citation: *Journal of Vacuum Science & Technology A* **31**, 01A127 (2013); doi: 10.1116/1.4768167

View online: <http://dx.doi.org/10.1116/1.4768167>

View Table of Contents: <http://scitation.aip.org/content/avs/journal/jvsta/31/1?ver=pdfcov>

Published by the AVS: Science & Technology of Materials, Interfaces, and Processing

Articles you may be interested in

Interface trap characterization of atomic layer deposition Al₂O₃/GaN metal-insulator-semiconductor capacitors using optically and thermally based deep level spectroscopies

J. Appl. Phys. **113**, 204505 (2013); 10.1063/1.4808093

Influence of interlayer trapping and detrapping mechanisms on the electrical characterization of hafnium oxide/silicon nitride stacks on silicon

J. Appl. Phys. **104**, 094107 (2008); 10.1063/1.3013441

Equivalent oxide thickness reduction of interpoly dielectric using ALD- Al₂O₃ for flash device application

J. Vac. Sci. Technol. B **22**, 2295 (2004); 10.1116/1.1781659

Effect of deuterium postmetal annealing on the reliability characteristics of an atomic-layer-deposited HfO₂ / SiO₂ stack gate dielectrics

Appl. Phys. Lett. **81**, 4038 (2002); 10.1063/1.1523636

Effects of interfacial layer growth on the electrical characteristics of thin titanium oxide films on silicon

Appl. Phys. Lett. **74**, 3143 (1999); 10.1063/1.124089

Instruments for Advanced Science

Contact Hiden Analytical for further details:
W www.HidenAnalytical.com
E info@hiden.co.uk
[CLICK TO VIEW](#) our product catalogue

Gas Analysis

- › dynamic measurement of reaction gas streams
- › catalysis and thermal analysis
- › molecular beam studies
- › dissolved species probes
- › fermentation, environmental and ecological studies

Surface Science

- › UHV TPD
- › SIMS
- › end point detection in ion beam etch
- › elemental imaging - surface mapping

Plasma Diagnostics

- › plasma source characterization
- › etch and deposition process reaction
- › kinetic studies
- › analysis of neutral and radical species

Vacuum Analysis

- › partial pressure measurement and control of process gases
- › reactive sputter process control
- › vacuum diagnostics
- › vacuum coating process monitoring

Electrical characterization of atomic-layer-deposited hafnium oxide films from hafnium tetrakis(dimethylamide) and water/ozone: Effects of growth temperature, oxygen source, and postdeposition annealing

Hector García,^{a)} Helena Castán, Salvador Dueñas, and Luis Bailón

Department of Electronics, ETSI Telecomunicación, University of Valladolid, 47011 Valladolid, Spain

Francesca Campabadal, Oihane Beldarrain, Miguel Zabala, Mireia Bargallo González, and Joan Marc Rafí

Institut de Microelectrònica de Barcelona, IMB-CNM (CSIC), Campus UAB, 08193 Bellaterra, Spain

(Received 26 July 2012; accepted 5 November 2012; published 27 November 2012)

The electrical properties of HfO₂-based metal–insulator–semiconductor capacitors have been systematically investigated by means of I–V and C–V characteristics, admittance spectroscopy, deep level transient spectroscopy, conductance transient, and flat band voltage transient techniques. Attention is also given to the study of the temperature dependence of the leakage current. HfO₂ films were grown on p-type silicon substrates by atomic layer deposition using hafnium tetrakis(dimethylamide) as hafnium precursor, and ozone or water as oxygen precursors. The growth temperature ranged from 150 to 350 °C. Low growth temperatures prevent decomposition and high growth rate, as well as high contamination levels. As a result, the leakage current is lower for lower deposition temperatures. Some of the deposited samples were submitted to a postdeposition annealing at 650 °C in N₂ atmosphere, showing a decrease in the leakage current and an increase in the equivalent oxide thickness (EOT), whereas interfacial state density increases and defect density inside the dielectric bulk decreases. Regarding dielectric reliability, in our experimental conditions, HfO₂ layers grown at 150 °C exhibit the largest EOT and breakdown voltage. The electrical behaviour is clearly linked with structural properties, and especially with the formation of an interfacial layer between the HfO₂ layer and the silicon substrate, as well as with the presence of several impurities. © 2013 American Vacuum Society. [<http://dx.doi.org/10.1116/1.4768167>]

I. INTRODUCTION

The continuous scaling down of devices in CMOS technology requires the replacement of SiO₂ as the gate dielectric. Many high-k dielectrics have been extensively studied^{1–3} in order to fulfil the CMOS scaling down laws. Among all high-k dielectrics, hafnium oxide and hafnium silicates are the most promising materials, and they are currently being used, in combination with metal gate electrodes, for transistor production in sub-30 nm CMOS technology nodes.⁴ However, many critical issues, such as thermal stability, have yet to be understood. Therefore, hafnium oxide is still the subject of intensive research. Indeed, the formation of an interfacial layer (IL) due to thermal steps after gate dielectric fabrication has been observed.⁵ This interlayer between the high-k dielectric and the semiconductor can strongly influence the electrical behavior of the fabricated structures, inducing leaking paths.⁶ In order to keep a good leakage control, the introduction of thin SiO₂ or SiO_xN_y interfacial layers has been suggested.⁷

As for the choice of a suitable high-k dielectric layer deposition method, it is worth to say that since the first study dealing with atomic layer deposition (ALD) of HfO₂,⁸ the ALD technique has been considered as a promising method providing the growth of HfO₂ films with acceptable conformality, density, and dielectric performance.^{9,10} Hafnium halides, such as HfCl₄, have been widely used as precursors for ALD of HfO₂. However, it has been demonstrated that this

process leads to significant residual chlorine content, which cannot be completely removed by annealing.¹¹ Moreover, HfCl₄ is a solid precursor with low vapor pressure, so it does not provide precursor transport with efficiency comparable to that of liquid precursors.¹² Chlorine-free precursors such as alkylamides have been used as ALD precursors. For example, HfO₂ has been grown from hafnium tetrakis(ethylmethylethylamide) (TEMAH), Hf[N(CH₃)(C₂H₅)]₄, and H₂O,^{13,14} from hafnium tetrakis(dimethylamide), Hf[N(CH₃)₂]₄, and H₂O,^{15–18} and from hafnium tetrakis(diethylamide) (TDMAH), Hf[N(C₂H₅)₂]₄, and H₂O.¹⁹ Besides H₂O, ozone (O₃) and NH₃ radicals can successfully assist in alkylamide-based ALD of HfO₂.²⁰ Earlier studies under identical growth conditions at 300 °C, under the same reactor pressure and with the same time parameters for both, alkylamide and halide precursors, have revealed that alkylamides can provide higher thickness uniformity and lower impurity levels than those measured in the films grown from HfCl₄,²⁰ and also may result in lower equivalent oxide thickness (EOT) than provided by HfCl₄.¹⁶ On the other hand, it has been reported that when using TEMAH and water as precursors in ALD processes, the high concentration of hydroxyl groups in the films degrades the dielectric interface during the postdeposition annealing (PDA).²¹ To solve this problem, O₃ can be used as an alternative oxidant due to its strong oxidizing and high volatility.²²

Besides CMOS devices, it is known that the physical and electrical properties of silicon carbide (SiC) make it an attractive material for high frequency, high power devices. The use of high-k oxides deposited onto SiC, as an alternative to SiO₂,

^{a)}Electronic mail: hecgar@ele.uva.es

has also been investigated.^{23,24} The ALD deposition of HfO₂ layers on SiC, Si/SiC, and SiO₂/SiC by using TDMAH as hafnium precursor has been reported.²⁵ It has been shown that in comparison to the HfO₂/SiC structure, the HfO₂/Si/SiC one minimizes leakage, thus providing a method for integrating HfO₂ into the SiC gate architecture.²⁵

The aim of this work is to study the effect of several technological parameters on the electrical characteristics of ALD HfO₂-based metal–insulator–semiconductor (MIS) structures. Hafnium precursor was TDMAH. The influence of growth temperature (150, 225, or 350 °C), oxygen precursor (O₃ or H₂O), and postdeposition annealing (at 650 °C in a N₂ ambient for 30 min) on the interface quality and current density was investigated. The electrical characteristics of the samples were exhaustively studied by means of the following techniques: capacitance–voltage (C–V), admittance spectroscopy, deep level transient spectroscopy (DLTS), conductance transients, flat band voltage transients (V_{FB}-t), and current–voltage (I–V). Dielectric reliability characterization was also performed. We present experimental results and discuss the influence of the technological parameters on the electrical properties and current conduction mechanisms through the films. Thus, the knowledge obtained earlier about the alkylamide ALD process will be complemented with a complete electrical characterization, focussing in processes carried out at low growth temperatures and using ozone as oxygen precursor. Our goal is to establish the better growth conditions of HfO₂ layers to be used in potential micro-nanoelectronics applications, including high power silicon carbide devices (with thicker dielectric),²⁵ resistive random-access memories,²⁶ and nanodevices.²⁷

II. EXPERIMENT

A. Sample preparation

HfO₂ layers were grown by atomic layer deposition in a Cambridge NanoTech Savannah 200 system equipped with TDMAH, H₂O, and O₃ as precursors, and N₂ as carrier and purge gas. The ALD process was carried out at different growth temperatures, T_g, with processes of 100 ALD cycles, being one ALD cycle the following sequence: an O₃ pulse of 10 ms, a purge in N₂ for 9 s, followed by a TDMAH pulse of 50 ms and a purge in N₂ for 5 s. The deposition of HfO₂ has been carried out on p-type (100) silicon wafers with 0.1–1.4 Ω cm resistivity. The film thickness was measured using a Nanospec (AFTmodel200) interferometer and the obtained values are shown in Table I.

In order to electrically characterize the deposited HfO₂ layers, MIS structures were fabricated. The fabrication process started with standard wafer cleaning followed by a wet thermal oxidation process at 1100 °C leading to a 400-nm-thick SiO₂ layer. This field oxide was patterned by photolithography and wet etching. Next, the wafers were cleaned using H₂SO₄ + H₂O solution, followed by an HF dip, deionized water rinse, and nitrogen blow dry. This cleaning sequence was done just before transferring the samples into the ALD reactor; therefore, the deposition was performed on a hydrogen-terminated silicon surface. After growth of the dielectric film, some samples underwent a PDA process at 650 °C in N₂ atmosphere for 30 min. A 500 nm thick Al/0.5% Cu layer was then deposited, which was patterned by photolithography and wet etching. The back side of the wafers was also metalized with aluminium for electrically contacting the silicon substrate. Finally, the wafers underwent a forming gas (N₂/(10%)H₂) annealing at 350 °C for 20 min. The fabricated MIS structures are square-shaped with different surface areas (A) ranging from 9.604×10^{-3} to 6.4×10^{-5} cm². Capacitors with HfO₂ deposited at 225 °C using H₂O as the oxygen precursor were also used for comparison purposes. A detailed description of the fabrication process can be found in Ref. 18.

B. Electrical characterization setup

The study of the electrical characteristics of the MIS structures has been first carried out through the measurement of C–V and current–voltage (I–V) characteristics at room temperature in a light-proof, electrically shielded probe station. C–V curves were recorded using an HP4192-A impedance analyzer in the parallel configuration at a frequency of 100 kHz and 30 mV ac signal level. For the current–voltage measurements, an HP4155B semiconductor parameter analyzer was used. The MIS structures were biased in accumulation, i.e., applying negative voltages to the metal gate with respect to the p-type substrates, so electrons were injected from the metal gate electrode.

In order to record the electrical parameters at several temperatures varying between liquid nitrogen temperature (77 K) and room temperature, samples were first cooled in darkness from room temperature to 77 K at zero bias in an Oxford DM1710 cryostat. An Oxford ITC 502 controller was used to monitor the temperature during the measurements. The capacitance measurements were carried out in this case with the assistance of a 1 MHz Boonton 72B

TABLE I. Physical thickness measured using a Nanospec (AFTmodel200) interferometer and extracted EOT, V_{fb}, and N_{eff} values from C–V characteristics at 100 kHz of HfO₂ based capacitors for the different ALD process conditions.

ALD	Non-PDA				PDA			
	T _{ox} (nm)	EOT (nm)	V _{fb} (V)	N _{eff} (cm ⁻²)	T _{ox} (nm)	EOT (nm)	V _{fb} (V)	N _{eff} (cm ⁻²)
150 °C (O ₃)	12	5.9	−0.72	-0.6×10^{12}	11.8	5.3	−0.65	-1×10^{12}
225 °C (O ₃)	11.4	3.9	−0.8	-0.5×10^{12}	11.2	4.5	−0.63	-1.2×10^{12}
350 °C (O ₃)	10.8	3.4	−0.99	0.6×10^{12}	10.4	4.4	−0.63	-1.2×10^{12}
225 °C (H ₂ O)	10.7	3.4	−0.65	-1.5×10^{12}	10.6	4.2	−0.65	-1.2×10^{12}

capacitance meter. For DLTS measurements, the Boonton 72B capacitance meter and an HP54501 digital oscilloscope to record the capacitance transients were used. A Keithley 617 programmable electrometer was used together with an HP214B pulse generator to introduce the quiescent bias and the filling pulse, respectively. The experimental setup of the conductance transient technique consisted of an HP 33120A arbitrary wave form generator to apply the bias pulses, an EG&G 5206 two-phase lock-in analyzer to measure the conductance, and an HP 54501 A digital oscilloscope to record the complete conductance transient. Finally, a Keithley 6517A working as a programmable bias source and a 1 MHz Boonton 72B capacitance meter were used for recording flat band voltage transients at constant-capacitance.

III. RESULTS AND DISCUSSION

A. Electrical characteristics

The leakage current densities (J) versus gate voltage (V_G) characteristics in the accumulation regime measured at room temperature are shown in Fig. 1 for the three growth temperature values studied. In the case of nonannealed HfO_2 layers

FIG. 1. (Color online) Current density vs gate voltage under gate injection for non-PDA (a) and PDA (b) based layers at room temperature.

[Fig. 1(a)], the current is larger for higher ALD deposition temperatures, with a current enhancement of more than two decades between 150 and 350 °C layers at $|V_G| > 3$ V.

Kukli *et al.*¹⁷ reported the effect of substrate temperature on the growth and physical properties of thin atomic layer deposited HfO_2 films from TDMAH and H_2O . They attributed the increase in the growth rate at temperatures higher than 350 °C to the thermal decomposition of the alkylamide molecules and violation of the ideal self-limiting ALD growth regime, and also observed that the best current values were obtained for intermediate growth temperatures. Decomposition and high growth rate are undesired properties in the ALD processes, and therefore growth temperature values as high as 400 °C must be avoided. In the present work, growth temperature values ranged between 150 and 350 °C; hence, it is expected that these undesired effects do not occur and, also, the residual contamination levels are maintained into acceptable limits. In our experimental conditions, the lower current values correspond to the lowest growth temperature. This difference could be connected to the highest amounts of hydrogen related impurities detected in Ref. 17 at the highest and lowest growth temperatures, which leads to high leakage currents and poor breakdown resistance. In our case, due to the fact that oxygen precursor is O_3 instead of H_2O , the presence of hydrogen contamination is more limited and the deterioration of film quality is only observed at the highest growth temperatures.

A rather different behavior is observed in the case of annealed layers [Fig. 1(b)]. For the case of $T_g = 150$ °C, the current increases when a PDA is carried out, while for the two higher deposition temperatures the current decreases. This different behavior can be influenced by a local reconstruction of the HfO_2 layers and an IL formation after thermal annealing treatments.^{28,29} In fact, it is known that due to the presence of oxygen in the ALD precursors, an interfacial SiO_x layer can be formed during high- k film deposition, thus increasing the EOT values. Indeed, oxygen diffusion in high- k films is usually higher than in SiO_2 . Besides, some structural defects such as oxygen vacancies and interstitials are usually present. Some of these defects may be healed by applying a PDA to the high- k film. The effect of the PDA strongly depends on the temperature and ambient used. Calculations indicate that N_2 and NH_3 together with their ions and derivatives can bond to oxygen vacancies in various charge states, or initiate an oxygen substitution process.⁵ On the other hand, at low deposition temperatures interfacial layer growth during high- k layer deposition is mostly limited by the initially grown IL layer, which may act as an effective barrier for further oxygen diffusion. Hence, the lower portion of the interfacial layer is expected to be oxygen deficient to a high degree. This fact could explain the different influence of the PDA on the electrical behavior of samples growth to different temperatures.

As for the oxygen precursor influence, we can see that H_2O based samples exhibit larger current compared to their O_3 counterparts, which can be linked to the presence of larger amount of residual impurities related to a high concentration of hydroxyl groups in the former case. On the other

hand, when measuring J–V characteristics in the accumulation regime at several temperatures we can observe that the current behavior is governed by a Poole–Frenkel emission mechanism, which indicates that the conduction mechanism through the dielectric is bulk limited, as usual in high- k insulator based MIS structures.³⁰ All J–V curves were well fitted according to the Poole–Frenkel emission model considering the well-known current relationship

$$J = CE \exp\left(-\frac{q\phi_T - \beta_{PF}\sqrt{E}}{k_B T}\right), \quad (1)$$

where C is a constant, ϕ_T is the potential well depth, E is the electric field, T is the temperature, and the β_{PF} is the Poole–Frenkel coefficient which is related to the barrier lowering by the applied field.

Figure 2 shows the plot of $\ln(I/E)$ vs $E^{1/2}$ at different temperatures under the accumulation regime for HfO_2 deposited using O_3 as precursor at 150°C and with PDA. The area of the measured samples was $2.304 \times 10^{-3} \text{ cm}^2$. The β_{PF} parameters are indicated at each temperature in the same Fig. 2. In addition, the experimental β_{PF} parameters were also evaluated for each sample by means of the previous Poole–Frenkel relationship and, in all cases the values obtained were about $1\text{--}4 \times 10^{-5} \text{ eV m}^{1/2} \text{ V}^{-1/2}$. The theoretical β_{PF} value obtained from the permittivity value of HfO_2 at optical frequencies is $1.5 \times 10^{-5} \text{ eV m}^{1/2} \text{ V}^{-1/2}$, taking into account that the refractive index for HfO_2 ranges from 1.7 to 1.9.³¹ The experimental values are reasonably in agreement with the theoretical ones, being both of the same order of magnitude. The small discrepancy can be related to the physical structure of the films that differs from the theoretical case and also to the IL formation. Additionally, the conduction behavior could be influenced by other conduction mechanisms, which may contribute to the current, although this is mainly dominated by Poole–Frenkel emission.³²

FIG. 2. $\ln(I/E)$ vs $E^{1/2}$ measured at different temperatures. β_{PF} values are given for every temperature.

The C–V characteristics measured at 100 kHz of the studied HfO_2 based capacitors are shown in Fig. 3. The EOT has been extracted from the capacitance in the accumulation regime, without quantum corrections. The results are shown in Table I, where an increase of EOT between 0.6 and 1 nm after a postdeposition annealing is observed (except for layers grown at 150°C). The EOT increase could be due to an enhanced IL formation after annealing treatments.^{28,29} This result is consistent with the leakage current reduction described above.³³ As expected, 150°C based layers with and without PDA show the largest EOT values.

In order to evaluate the charge in the bulk of the dielectric, it should be mentioned that a negative shift of the flat band voltage (V_{fb}) with respect to the theoretical value indicates the presence of a positive charge, while positive shifts indicate fixed negative charge.^{34,35} The total effective charge (N_{eff}), which is composed by the oxide charge and the possible contribution of interface traps, can be defined as

$$N_{eff} = \frac{(\phi_{MS} - V_{fb})C_{ox}}{qA}, \quad (2)$$

where q is the electron charge, C_{ox} is oxide capacitance, and ϕ_{MS} is the metal–semiconductor work function. The extracted V_{fb} and N_{eff} values for the different ALD process conditions are shown in Table I.

FIG. 3. (Color online) Capacitance vs gate voltage for non-PDA (a) and PDA (b) based layers.

The presence of interface states is evidenced by the stretch-out of the C–V curves along the gate voltage axis, as a result of the different electronic character of the traps along the bandgap.³⁴ Additionally, conductance peaks are observed in the depletion region, resulting from a change in interface trap occupancy by capture and emission of carriers due to the ac gate bias charge.^{34,35} A first estimation of the interface state density (D_{it}) was obtained from the parallel conductance peaks (G_{p_max}) by^{34,36}

$$D_{it} \approx \frac{2.5}{q \cdot A} \cdot \frac{G_{p_max}}{\omega}, \quad (3)$$

where $\omega = 2\pi f$. D_{it} values were also evaluated by means of DLTS technique, obtaining similar results.

Our measurements indicate that when increasing the ALD temperature from 150 to 350 °C in non-PDA layers positive charges are generated (see Table I). However, no clear influence of the growth temperature on the interface state density is detected, where a D_{it} value of $\sim 9 \times 10^{10} \text{ cm}^{-2} \text{ eV}^{-1}$ is observed for the studied non-PDA based capacitors [Fig. 4(a)]. Besides, the use of a postdeposition annealing in O_3 based films generates negative bulk charges (Table I) and interface states [Fig. 4(a)].

C–V curves exhibit the typical hysteresis phenomena. This fact indicates that there are slow states in the dielectric films, i.e., defects distributed away from the interface to the

insulator³⁷ which can exchange electrons with the Si substrate through tunneling. These defects are called disordered induced gap states (DIGS) according to Hasegawa model.^{38,39} First, the hysteresis of the C–V characteristics has been evaluated from the difference between the extracted flat band voltages corresponding to C–V curves measured from inversion to accumulation and then sweeping back ($V_{FB_inv_to_acc} - V_{FB_acc_to_inv}$). According to Fig. 4(b), the use of a PDA reduces the counterclockwise hysteresis (except for the 150 °C case). This result, in agreement with previously published work,⁴⁰ can be explained by the oxidation of the Si interface after annealing^{29,41} and/or the reduction of an excess of hydrogen and/or hydroxyl groups in the layer introduced by the precursor chemistry.^{17,40} Additionally, lower hysteresis is observed for 350 °C layers compared to the 225 °C case. Similar results have been previously reported on H_2O based layers.⁴⁰ It should be noted in Fig. 4(b) that the use of H_2O as oxidant source without a PDA treatment enhances the counterclockwise hysteresis by a factor of 3. Furthermore, 150 °C non-PDA O_3 -based samples show the lowest slow trap response corresponding to the largest EOT value.

In order to evaluate the spatial and energetic distribution of the slow states, the conductance transient technique has been applied, which allows obtaining a three-dimensional plot of DIGS density as a function of energy and spatial position. In Fig. 5(a) three-dimensional graph of DIGS density corresponding to the 225 °C non-PDA H_2O -based sample is shown. DIGS density value inside the insulator is reduced when a PDA is applied, in agreement with the small hysteresis in C–V curves obtained in this case. Furthermore, the highest DIGS density was obtained for 150 °C PDA O_3 -based sample, about $6 \times 10^{11} \text{ cm}^{-2} \text{ eV}^{-1}$ in accordance with the above J–V discussion. In fact, this sample exhibited the larger hysteresis phenomena after postdeposition annealing [Fig. 4(b)].

FIG. 4. (Color online) Density of interface states (a) and hysteresis (b) for the studied HfO_2 based capacitors.

FIG. 5. Three-dimensional DIGS profile for the non-PDA sample grown at 225 °C using water as precursor.

Insulator trap charging and discharging mechanisms give rise to flat band voltage transients from which we can obtain information about phonon-assisted tunneling mechanisms between localized states in the band gap of the insulator.³² In order to obtain these transients, it is necessary to record the gate voltage while keeping constant the capacitance at the flat band condition. Figure 6(a) shows the amplitude of flat band transients measured at room temperature corresponding to the HfO₂-based samples without a PDA. As it can be observed, the flat band voltage transients which have previously been biased in inversion show a decreasing behavior unlike those previously biased from an accumulation regimen. This performance is clearly due to hysteresis features in C–V curves³² since the hysteresis was counterclockwise for all HfO₂-based samples. Moreover, it can also be noticed that the amplitude of flat band transients shows a visible dependency on the ALD deposition temperature and on the precursor used.

The transient amplitude for H₂O-based samples was higher, so the use of O₃ as oxidant precursor results in better

quality HfO₂ films. This result is in agreement with the previous C–V and J–V data. Hysteresis of 150 °C non-PDA O₃-based sample is negligible [Fig. 4(b)], so transients amplitude in this case is very small.

On the other hand, the activation energy of soft optical phonons that produces the ionization of traps of the insulator in this phonon-assisted tunneling conduction can be estimated by means of an Arrhenius plot. In Fig. 6(b), the amplitude of flat band transients measured at several temperatures corresponding to the 225 °C non-PDA H₂O-based sample has been depicted. The temperature–transient amplitude relation follows a linear trend with an activation energy of ~54 meV [see inset Fig. 6(b)], which is comparable to the soft optical phonon energies usually reported for high-k dielectrics.⁴²

B. Dielectric reliability characterization

In order to evaluate the HfO₂ layers reliability, ramped I–V characteristics of a set of 25 capacitors for each process condition was measured and the breakdown voltage (V_{BD}) was recorded. The Weibull cumulative breakdown distribution shown in Fig. 7 is defined as

$$F(V_{BD}) = 1 - \exp \left[- \left(\frac{|V_{BD}|}{\alpha} \right)^\beta \right], \quad (4)$$

where α is the voltage at which 63.2% of the capacitors are broken, and β is the Weibull slope indicating the width of the distribution. The obtained β and α values are shown in Table II.

The results indicate that layers grown at 150 °C exhibit the largest V_{BD} , being the most beneficial condition studied for layer reliability, while layers grown at 350 °C show the lowest V_{BD} values. Furthermore, it can be observed that H₂O based capacitors grown at 225 °C exhibit lower α values as compared to their O₃ counterparts. The obtained V_{BD} results are consistent with the extracted EOT values. Finally, no clear trends between the growth temperature and the dielectric breakdown voltage spread have been appreciated by means of the β value.

FIG. 6. Flat-band transients measured at room temperature corresponding to the HfO₂-based samples without a PDA (a) and transients measured at several temperatures (Arrhenius plot inset) for non-PDA H₂O-based HfO₂ layers (b).

FIG. 7. (Color online) Comparison of Weibull plot of the cumulative breakdown distributions F vs breakdown voltage. The dielectric breakdown voltage is detected as the sudden increase in the current of MOS capacitors during the voltage ramp measurements.

TABLE II. Physical β values and $|V_{BD}|$ at 63.2% of the cumulative breakdown distributions F vs breakdown voltage.

ALD	Non-PDA		PDA	
	β	α (V)	β	α (V)
150 °C (O ₃)	12.4	9.63	38.2	7.01
225 °C (O ₃)	34	6.66	7.3	6.19
350 °C (O ₃)	8.7	3.37	29	5.92
225 °C (H ₂ O)	16.6	4.28	18.1	5.98

IV. CONCLUSIONS

An exhaustive electrical characterization of the HfO₂-based MIS capacitors has been carried out. The results in our experimental work indicate that the leakage current is larger for higher deposition temperatures when samples were not annealed, but a different behavior was observed in the case of postdeposition annealed layers, which could be related, according to previous published works, to an IL formation, as evidenced by the increase of EOT after PDA treatments. Low growth temperatures prevent decomposition and high growth rate, as well as high contamination levels. As expected, the dominant leakage current mechanism was found to be Poole–Frenkel emission, with the β_{PF} values obtained close to the theoretical one.

Additionally, in our experimental work, the growth temperature for non-PDA samples does not play a significant role in the D_{it} values. However, when annealing the samples, the interface quality worsens. The hysteresis phenomena in C–V curves, due to defects inside the bulk of the insulator, are in most cases reduced when the postdeposition annealing has been carried out. This result has been confirmed using conductance transient technique and can be explained by the oxidation of the Si interface after annealing and/or the reduction of an excess of hydrogen and or hydroxyl groups in the layer introduced by the precursor chemistry. Conductance transients amplitude agrees with the hysteresis obtained in C–V curves. The temperature–transient amplitude relation follows a linear trend with an activation energy of about 54 meV, which is comparable to the soft optical phonon energies reported for high-k dielectrics.

Finally, and regarding dielectric reliability, HfO₂ layers grown at 150 °C exhibit both the largest breakdown voltage and the largest EOT values, being the most beneficial condition studied for layer reliability.

ACKNOWLEDGMENT

The study has been supported by the Spanish TEC2011 under Grant Nos. 27292-C02-01 and 27292-C02-02.

¹J. Robertson, *Solid-State Electron.* **49**, 283 (2005).

²M. Houssa, L. Pantisano, L.-Å. Ragnarsson, R. Degraeve, T. Schram, G. Pourtois, S. De Gendt, G. Groeseneken, and M. M. Heyns, *Mater. Sci. Eng. R* **51**, 37 (2006).

³J. Robertson, *Rep. Prog. Phys.* **69**, 327 (2006).

⁴S. M. George, *Chem Rev.* **110**, 111 (2010).

⁵G. Bersuker, P. Zeitzoff, G. Brown, and H. R. Huff, *Mater. Today* **7**, 26 (2004).

⁶H. Nishino, N. Hayasaka, K. Horioka, J. Shiozawa, S. Nadahara, N. Shooda, Y. Akama, A. Sakai, and H. Okano, *J. Appl. Phys.* **74**, 1349 (1993).

⁷H. Wong and H. Iwai, *Microelectron. Eng.* **83**, 1867 (2006).

⁸M. Ritala, M. Leskelä, L. Niinistö, T. Prohaska, G. Friedbacher, and M. Grasserbauer, *Thin Solid Films* **250**, 72 (1994).

⁹Y.-B. Kim, M.-S. Kang, T. Lee, J. Ahn, and D.-K. Choi, *J. Vac. Sci. Technol. B* **21**, 2029 (2003).

¹⁰M. Johansson, M. Y. A. Yousif, P. Lundgren, S. Bengtsson, J. Sundqvist, A. Harsta, and H. H. Radamson, *Semicond. Sci. Technol.* **18**, 820 (2003).

¹¹J. Aarik, A. Aidla, A.-A. Kiisler, T. Uustare, and V. Sammelselg, *Thin Solid Films* **340**, 110 (1999).

¹²A. Hand, *Semicond. Int.* **26**, 46 (2003).

¹³K. Kukli, M. Ritala, T. Sajavaara, J. Keinonen, and M. Leskelä, *Chem. Vap. Deposition* **8**, 199 (2002).

¹⁴K. Kukli, M. Ritala, J. Lu, A. Harsta, and M. Leskelä, *J. Electrochem. Soc.* **151**, F189 (2004).

¹⁵M. J. Biercuk, D. J. Monsma, C. M. Marcus, J. S. Becker, and R. G. Gordon, *Appl. Phys. Lett.* **83**, 2405 (2003).

¹⁶M. Cho, H. B. Park, J. Park, S. W. Lee, C. S. Hwang, G. H. Jang, and J. Jeong, *Appl. Phys. Lett.* **83**, 5503 (2003).

¹⁷K. Kukli, T. Pilvi, M. Ritala, T. Sajavaara, J. Lu, and M. Leskelä, *Thin Solid Films* **491**, 328 (2005).

¹⁸F. Campabadal, J. M. Rafi, M. Zabala, O. Beldarrain, A. Faigón, H. Castán, A. Gómez, H. García, and S. Dueñas, *J. Vac. Sci. Technol. B* **29**, 01AA07 (2011).

¹⁹A. Deshpande, R. Inman, G. Jursich, and C. Takoudis, *J. Vac. Sci. Technol. A* **22**, 2035 (2004).

²⁰T. Kawahara, K. Torii, R. Mitsuhashi, A. Mutoh, A. Horiuchi, H. Ito, and H. Kitayama, *Extended Abstracts of International Workshop on Gate Insulator*, Tokyo, Japan, 6–7 November 2003 (IEEE Service Center Single Publication Sales Unit, Piscataway, USA, 2003), p. 32.

²¹J. Fan, H. Liu, Q. Kuang, B. Gao, F. Ma, and Y. Hao, *Microelectron. Reliab.* **52**, 1043 (2012).

²²H. Kato, K. S. Seol, M. Fujimaki, T. Toyoda, and M. Takiyama, *Jpn. J. Appl. Phys., Part 1* **38**, 6791 (1999).

²³K. Y. Gao, T. Seyller, L. Ley, F. Ciobanu, G. Pensl, A. Tadich, J. D. Riley, and R. G. C. Leckey, *Appl. Phys. Lett.* **83**, 1830 (2003).

²⁴Q. Chen, Y. P. Feng, J. W. Chai, Z. Zhang, J. S. Pan, and S. J. Wang, *Appl. Phys. Lett.* **93**, 052104 (2008).

²⁵P. M. Gammon *et al.*, *Appl. Phys. Lett.* **97**, 013506 (2010).

²⁶C. Walczyk *et al.*, *IEEE Trans. Electron Devices* **58**, 3124 (2011).

²⁷A. Javey, J. Guo, D. B. Farmer, Q. Wang, D. Wang, R. G. Gordon, M. Lundstrom, and H. Dai, *Nano Lett.* **4**, 447 (2004).

²⁸J. M. Rafi, M. Zabala, O. Beldarrain, and F. Campabadal, *J. Electrochem. Soc.* **158**, G108 (2011).

²⁹C. C. Yeo, M. S. Joo, B. J. Cho, and S. J. Whang, *Thin Solid Films* **462–463**, 90 (2004).

³⁰A. Taube, R. Mroczynsky, K. Korwin-Mikke, S. Gieraltowska, J. Szmidi, and A. Piotrowska, *Mater. Sci. Eng., B* **177**, 1281 (2012).

³¹J. Frenkel, *Phys. Rev.* **54**, 647 (1938).

³²A. Gómez, H. Castán, H. García, S. Dueñas, L. Bailón, F. Campabadal, J. M. Rafi, and M. Zabala, *J. Vac. Sci. Technol. B* **29**, 01A901 (2011).

³³J. Swerts, N. Peys, L. Nyns, A. Delabie, A. Franquet, J. W. Maes, S. Van Elshocht, and S. De Gendt, *J. Electrochem. Soc.* **157**, G26 (2010).

³⁴D. K. Schroder, *Semiconductor Material and Device Characterization* (John Wiley & Sons, New York, 2006).

³⁵E. H. Nicollian and J. R. Brews, *MOS (Metal Oxide Semiconductor) Physics and Technology* (John Wiley & Sons, New York, 1982).

³⁶Y. Hwang, R. Engel-Herbert, N. G. Rudawski, and S. Stemmer, *Appl. Phys. Lett.* **96**, 102910 (2010).

³⁷D. M. Fleetwood, *IEEE Trans. Nucl. Sci.* **39**, 269 (1992).

³⁸L. He, H. Hasegawa, T. Sawada, and H. Ohno, *J. Appl. Phys.* **63**, 2120 (1988).

³⁹L. He, H. Hasegawa, T. Sawada, and H. Ohno, *Jpn. J. Appl. Phys., Part 1* **27**, 512 (1988).

⁴⁰J. M. Rafi, M. Zabala, O. Beldarrain, and F. Campabadal, *ECS Trans.* **28**, 213 (2010).

⁴¹K. Kukli, M. Ritala, M. Leskelä, T. Sajavaara, J. Keinonen, D. C. Gilmer, R. Hegde, R. Rai, and L. Prabhu, *J. Mater. Sci.: Mater. Electron.* **14**, 361 (2003).

⁴²M. V. Fischetti, D. A. Neumayer, and E. A. Cartier, *J. Appl. Phys.* **90**, 4587 (2001).