Flexible CMOS Low-Noise Amplifiers for Beyond-3G Wireless Hand-Held Devices

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ABSTRACT

This paper explores the use of reconfigurable Low-Noise Amplifiers (LNAs) for the implementation of CMOS Radio Frequency (RF) front-ends in the next generation of multi-standard wireless transceivers. Main circuit strategies reported so far for multi-standard LNAs are reviewed and a novel flexible LNA intended for Beyond-3G RF hand-held terminals is presented. The proposed LNA circuit consists of a two-stage topology that combines inductive-source degeneration with PMOS-varactor based tuning network and a programmable load to adapt its performance to different standard specifications without penalizing the circuit noise and with a reduced number of inductors as compared to previous reported reconfigurable LNAs. The circuit has been designed in a 90-nm CMOS technology to cope with the requirements of the GSM, WCDMA, Bluetooth and WLAN (IEEE 802.11b-g) standards. Simulation results, including technology and packaging parasitics, demonstrate correct operation of the circuit for all the standards under study, featuring NF<2.8dB, S_{21}>13.3dB and IIP3>10.9dBm, over a 1.85GHz-2.4GHz band, with an adaptive power consumption between 17mW and 22mW from a 1-V supply voltage. Preliminary experimental measurements are included, showing a correct reconfiguration operation within the operation band.

Keywords: Low-Noise Amplifiers, reconfigurable/adaptive RF CMOS circuits, multi-standard wireless telecom.

1. INTRODUCTION

Beyond-3G (B3G) hand-held terminals will require low-power *multi-standard chipsets*, capable to operate over a variety of standard specifications including different frequency bands, access techniques, number of channels, modulation schemes, data rates, as well as handling different signal conditions, battery status, while optimizing their power dissipation (portability) and silicon area (cost) [1-4].

The majority of reported multi-standard Radio-Frequency (RF) receivers use a single down-conversion scheme as conceptually depicted in Fig.1[5-6]. This architecture eliminates the need for both Intermediate-Frequency (IF) and Image Reject (IR) filtering and requires only a single oscillator and mixer, what makes it very suited for multi-standard applications because it increases the level of integration and facilitates hardware sharing. Moreover, the most common situation is that, in order to cope with the requirements of the different standards, separate (switchable) RF front-end paths (usually one per standard) are used whereas a single, digitally-programmed baseband section 0from the mixer to the Analog-to-Digital Converter (ADC) 0 is shared by all standards[5].

However, the trend is towards a maximum hardware reuse, by making as many transceiver building blocks as possible digitally programmable and reconfigurable[6]. Indeed, an ideal optimized multi-standard transceiver should be as conceptually depicted in Fig.2. Moreover, nanometer CMOS processes are expected to be the base technologies to develop this

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new generation of RF transceivers, assuring mass production at low cost through increased integration levels and extensive use of digital signal processing. Although there has been some approaches to implement an architecture similar to that in Fig.2[7,8], the integration of increasingly complex RF parts imposes a number of challenges and trade-offs that makes their design a key issue to guarantee the quality of service. Consequently, we are still far from applying this scheme to B3G wireless systems[1].

One of the most challenging circuits to implement the scheme in Fig.2 is the Low-Noise Amplifier (LNA). The design of this block is specially critical due to its position at the receiver front-end, having to simultaneously match the antenna and to amplify weak input signals with minimum noise contribution, high linearity and isolation from the rest of the receiver chain. This problem is aggravated in the case of multi-standard applications, in which LNAs must operate over different frequency ranges, whereas keeping reduced number of passives to increase the integration [5-8]. In order to solve the above-mentioned problems, several multi-standard LNAs have been reported in literature [9-16]. Most of them increase the number of integrated passive elements (basically capacitors and inductors) as compared to their mono-standard counterparts. These elements contribute significantly to the whole chip area and hence, do not offer a clear advantage with respect to Fig.1.
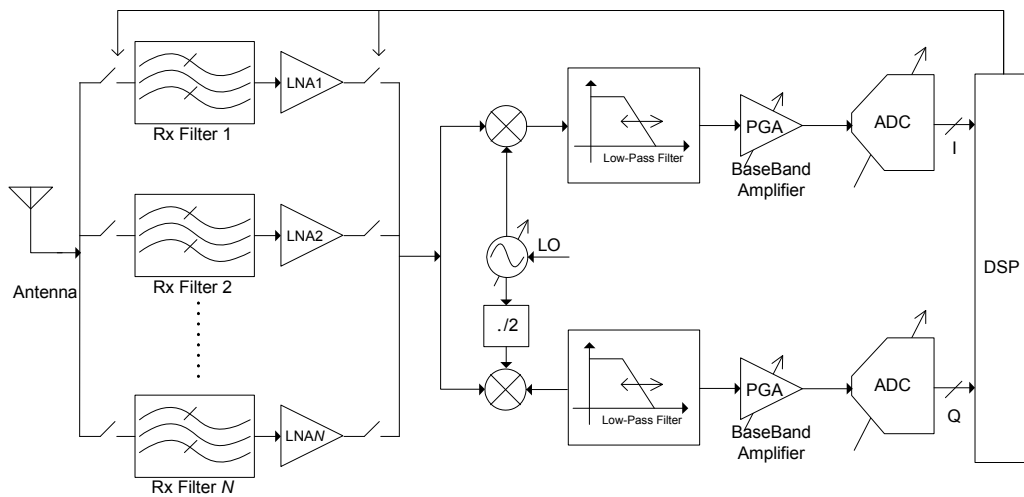

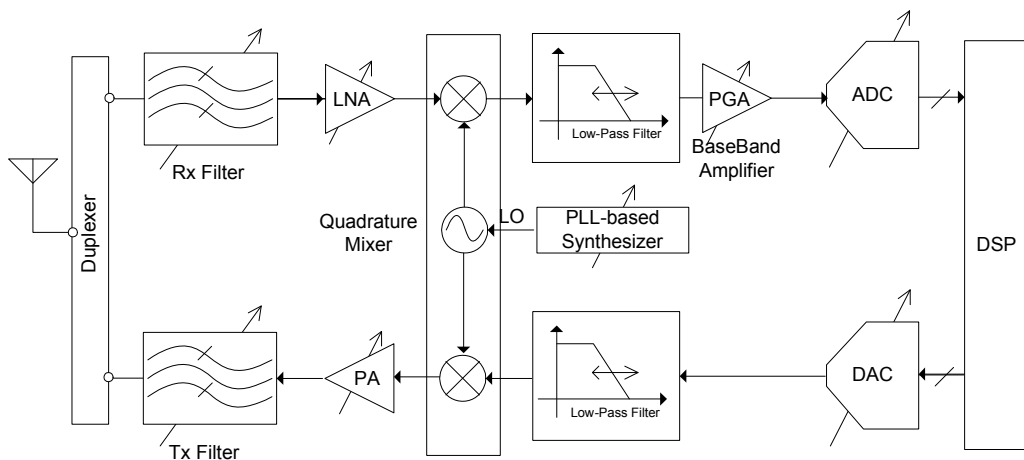Figure 1.   Commonly used multi-standard RF receiver architecture.

Figure 2.   Ideal multi-standard RF transceiver.

This paper contributes to this topic and presents the design and implementation of a flexible CMOS LNA for multi-standard transceivers. The circuit adapts its performance to the requirements of four standards (GSM, WCDMA, Bluetooth and WLAN) without increasing the number of inductors as compared to the mono-standard case. It employs a two-stage topology to separately control the input impedance and the signal gain. A PMOS-varactor tuning network is used in both stages in order to make the resonance frequency programmable without penalizing the LNA noise performance. SpectreRF simulations considering technology parasitics and chip-package effects are shown to verify the operation of the circuit.

2. BACKGROUND ON RECONFIGURABLE LOW-NOISE AMPLIFIERS

Most reported multi-standard CMOS LNAs are based on the use of a switchable passive network, as shown in Fig.3(a), to select the resonance frequency, thus preserving immunity to out-of-band interferers, although only one signal band is received at one time [10-12]. Besides, the use of switches forces a discrete frequency selection and introduces parasitic switch-on resistances and capacitances, with the subsequent trade-off between noise and speed. Thus, if a low switch-on resistance is used, the size of transistors implementing the switch must be enlarged, thus increasing the associated parasitic capacitances, whereas small switches lead to high switch-on resistances, thus penalizing the Noise Figure (NF).
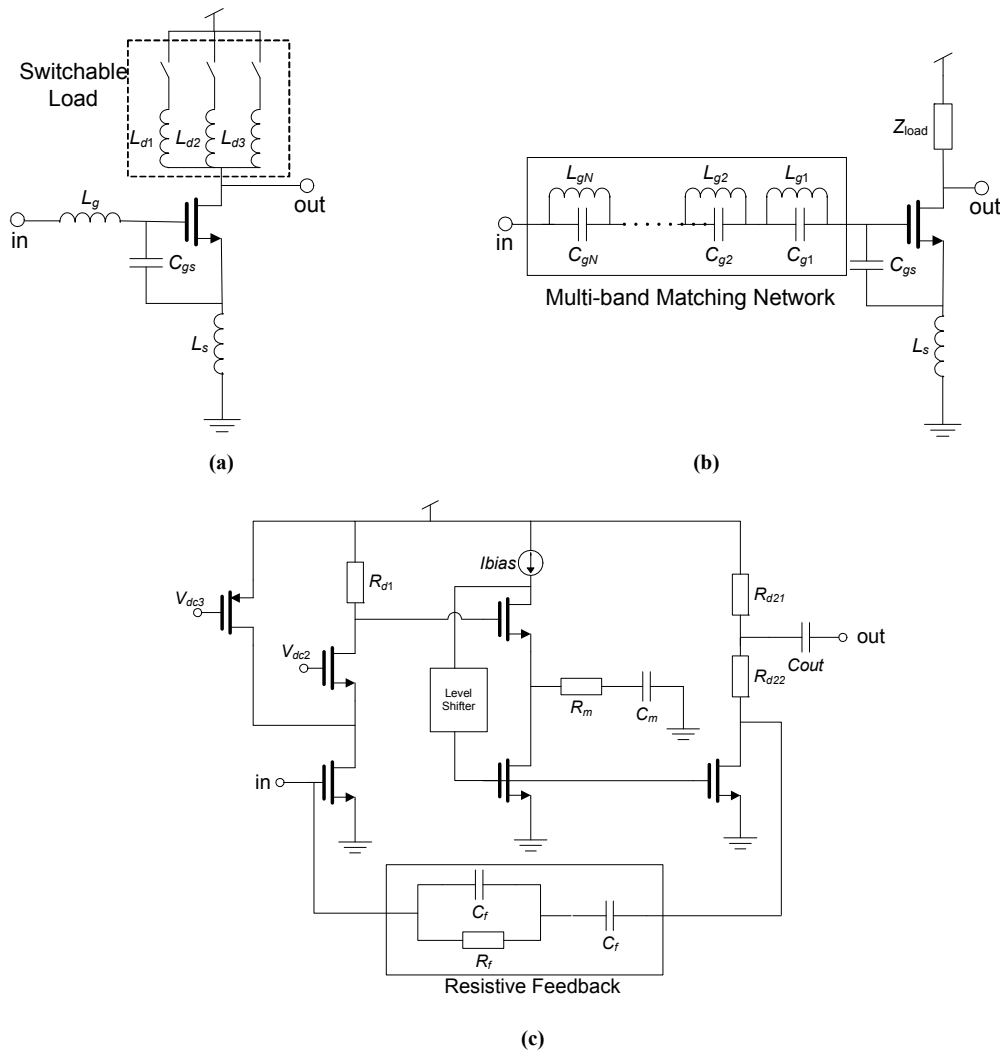

Figure 3. Different circuit techniques to implement multi-standard LNAs. (a) Switchable resonant tank [11]. (b) Multi-band matching network [15]. (c) Wideband amplification based on resistive feedback [16].

The above limitations can be partially solved by using concurrent multi-band LNAs [9,15], as illustrated in Fig.3(b), which allows a simultaneous reception of multiple signal bands without using switches. However, the spurs in one band may corrupt signals in other band due to the LNA non-linear operation.

A common issue in the multi-standard LNAs shown in Fig.3(a) and Fig.3(b) is the need of additional passive components for the input and output matching networks. This fact has motivated exploring other techniques, like the use of wideband resistive-feedback topologies [14] �‍ shown in Fig.3(c) �‍ that can achieve good performance in a wide signal bandwidth without using inductors [16], usually at the price of increasing noise.

3. PROPOSED ADAPTIVE LNA CIRCUIT

Fig.4 shows the complete schematic of the proposed reconfigurable LNA. It consists of a two-stage topology with separate tuning networks. The input stage, formed by transistors M_{n1} and $M_{pNF1,2}$, uses an inductively degenerated common-source structure to provide a specified real part for the input impedance and signal gain at a given frequency. The output stage of the LNA, made up of transistors M_{n2} and $M_{pGAIN1,2}$, provides higher gain without significantly degrading the noise performance.

Assuming that inductors L_g and L_s are ideal, and neglecting the effect of $R_{b1,2}$, the input impedance of the LNA is approximately given by:

$$Z_{in} \cong \frac{C_I + C_{gsn1}}{s C_I C_{gsn1}} + s\,(L_g + L_s) + \frac{g_{mn1} L_s}{C_{gsn1}}\left[1 - s\frac{g_{mn1} L_s C_{var\_D}}{C_{gsn1}}\right] \tag{1}$$

where g_{mn1} and C_{gsn1} are the small-signal transconductance and gate-source capacitance of M_{n1}. The real part of Z_{in}, given by $(g_{mn1} L_s)/C_{gsn1}$, is usually chosen to be equal to the RF source resistance, R_s, in the band of interest. In our case, as the LNA is fully integrated as a stand-alone circuit, a termination of $50\,\Omega$ is needed at both the input and the output terminals, within the whole band. For that purpose, in addition to the mentioned input impedance matching network, an output matching network, formed by L_O and C_O, is included in the circuit.
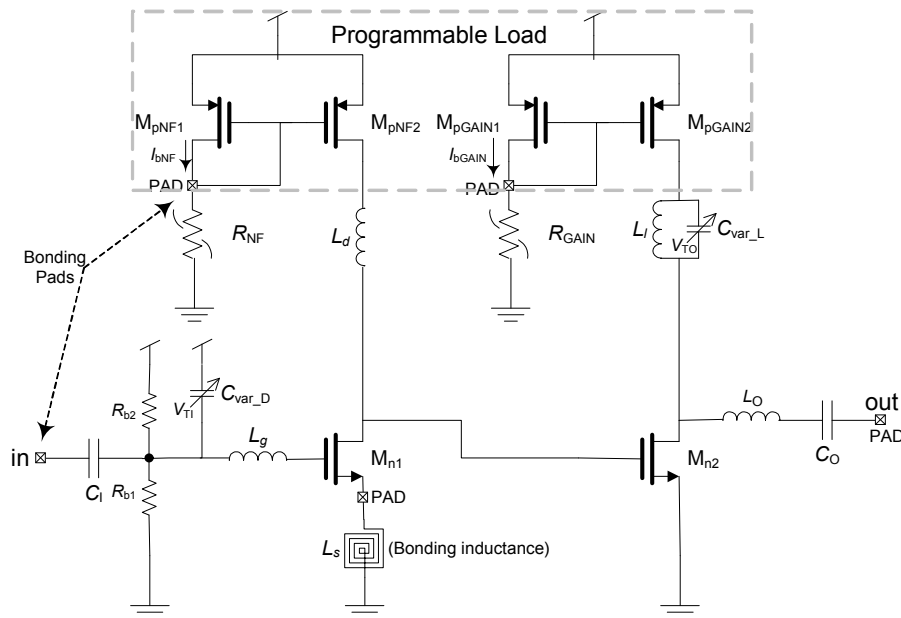

Figure 4. Schematic of the proposed adaptive LNA.

The tuning mechanism of the LNA is achieved by varying the resonance frequencies of the passive input- and output-tuning networks, respectively given by:

$$z_{in} \propto \frac{1}{\sqrt{C_{gsn1} \left[L_g + L_s - \left[(g_{mn1} L_s) / C_{gsn1} \right]^2 C_{var\_D} \right]}} ; z_{out} \propto \frac{1}{\sqrt{L_l C_{var\_L}}} \quad (2)$$

where C_{var_D} and C_{var_L} are implemented by accumulation PMOS varactors. The capacitance of these varactors, controlled by voltages V_{TI} and V_{TO}, can be varied from 20fF to 10pF, providing a resonance frequency of up to 20GHz.

Programmable biasing is used to separately control the real part of the load of both stages, implemented by transistors M_{pNF2} and M_{pGAIN2}. In this way, NF and the voltage gain can be individually controlled by diode-connected transistors M_{pNF1} and M_{pGAIN1}, respectively. Thus, the drain current of these transistors, I_{bNF} and I_{bGAIN}, are adapted to properly biasing the gate of M_{pNF2} and M_{pGAIN2}, in order to achieve the required specifications for each standard with reduced power dissipation. In this prototype, I_{bNF} and I_{bGAIN} are generated by external off-chip variable resistors, R_{NF} and R_{GAIN} (see Fig.4) in order to probe the concept. However, in a practical application, an on-chip implementation should be used.

4. CIRCUIT DESIGN PROCEDURE AND SIZING

The proposed reconfigurable LNA has been designed to fulfil the requirements of a multi-standard wireless direct-conversion receiver for the following standards: GSM, WCDMA, Bluetooth (BT) and WLAN. These requirements were extracted from a number of previously reported RF receivers [13,17,18]. In order to cope with the different sets of specifications, the following design procedure was followed:

- (1) Passive elements of the input matching network, C_I, L_g and L_s, are derived from (1) in order to get the required input impedance, i.e $Z_{in}=R_s=50\Omega$.

- (2) Transistors M_{n1} and $M_{pNF1,2}$, and R_{NF} are sized in order to achieve the minimum value required for NF in the signal bandwidth, whereas trying to achieve the maximum voltage gain possible with the least power dissipation through proper adjustment of R_{NF}. At this design step, the values of R_{b1} and R_{b2} are set to provide the operating point required at the gate of M_{n1}, considering both linearity and noise requirement.

- (3) Transistors M_{n2} and $M_{pGAIN1,2}$ and resistor R_{GAIN} are sized in order to get the maximum voltage gain.

- (4) L_O and C_O are calculated to get an output impedance matched to $Z_{out}= 50\Omega$.

- (5) L_g, L_l, C_{var_D} and C_{var_L} are computed from (2) to get the required LNA tuning frequencies for each standard.

- (6) Technology parasitics are considered in an interactive electrical simulation process to re-fine the sizing and biasing obtained in previous steps.

The outcome of the design procedure described above is the sizing and biasing of the LNA, summarized in Table 1. The performance of the circuit is adapted to the different standards specifications by varying the values of R_{NF} and R_{GAIN}. These values, together with varactor capacitances, are shown in Table 1.

Table 1: LNA Sizing

Transistors	W/L (µm/µm)	Capacitors (pF)	Inductors (nH)
M_{n1}	220/0.3	C_I = 5.7; C_O =13.5	L_d = 12.1
M_{n2}	124/0.3	C_{var_D} = (0.6,1.4)	L_g = 5.9
M_{pNF1}	1/0.1	C_{var_L}= (0.9,1.5)	L_s= 0.1
M_{pNF2}	124/0.1	**Resistors (kΩ)**	L_l= 4.7
M_{pGAIN1}	1/0.1	R_{NF} = 0.5-1	L_O= 7.1
M_{pGAIN2}	124/0.1	R_{GAIN} = 0.5-1	

5. LAYOUT, PACKAGING AND SIMULATION RESULTS

The LNA has been designed and implemented using a 90-nm CMOS technology with a single 1-V supply voltage. Fig.5 shows the layout of the chip highlighting their main parts. Integrated inductors have a patterned ground shield and octagonal shape. Input/output capacitors are implemented by M-O-M structures, which are based on the combination of stacked and finger metal-metal capacitors. All pads are ElectroStatic Discharged (ESD) protected. The die area, including pads, is 1.8 mm^2, with the core occupying 1.0 mm^2. As usual, a significant portion of this area is used by integrated inductors. However, in this circuit, and contrary to most reported multi-standard LNAs, the number of inductors is not increased as compared to the mono-standard case, with the subsequent area saving.

The circuit has been extensively verified using CADENCE SpectreRF. Technology parasitics and package effects were considered in the simulations. For that purpose, the circuit in Fig.6 was used. This circuit includes the package and the external components to be included in the PCB. A 4mmx4mm 12-pin QFN plastic package has been used. This package has been modelled using CADENCE PKG tool in order to take into account their associated parasitics during the design process.
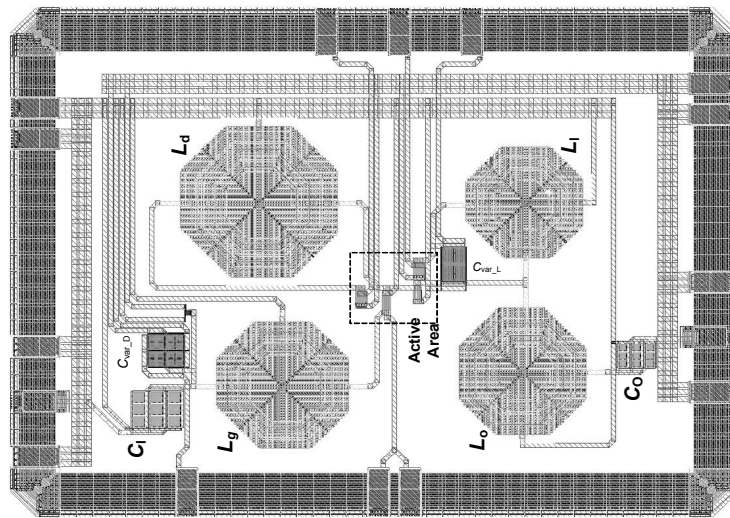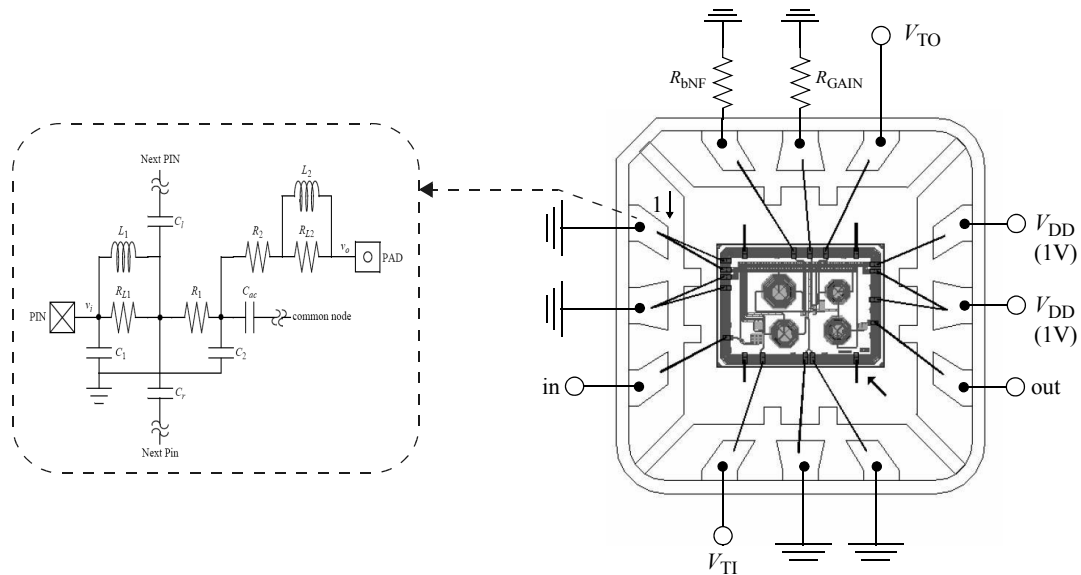

Figure 5.   Layout of the LNA.

Figure 6.   PCB conceptual schematic with QFN package and equivalent circuit.

Fig.7(a) represents NF vs. input frequency for all the standards under study. The overall minimum value of NF is 1.8dB, obtained at 2.4GHz, which corresponds to the WLAN operation mode. Fig.7(b) and Fig.7(c) show respectively the forward-gain (S_{21}) and the input reflection coefficient (S_{11}). The minimum value of S_{21} within the band of interest is above 13dB, corresponding to Bluetooth, whereas S_{11} and S_{22} are below −8.5dB for all standards. The linearity of the LNA has been also taken into account in the design process. The minimum and maximum values achieved of the 3rd-order inter-modulation intercept point, IIP3, are 10.9dBm and 19dBm, respectively for Bluetooth and WLAN, as illustrated in Fig.8.

In addition to the nominal simulations describe above, MonteCarlo and technology corners analyses were carried out. As an illustration, Fig.9 shows a 100-run MonteCarlo simulation of NF for Bluetooth, showing a worst-case value of 2.9dB in agreement with required specifications. Fig.10(a) shows the variations of S_{22} due to technology corners for WCDMA. Note that a worst-case value of −10.8dB is obtained, which is 3.9dB worse than the nominal case. This can be compensated in practice by tuning varactors using V_{TI} and V_{TO}, as illustrated in Fig.10(b).
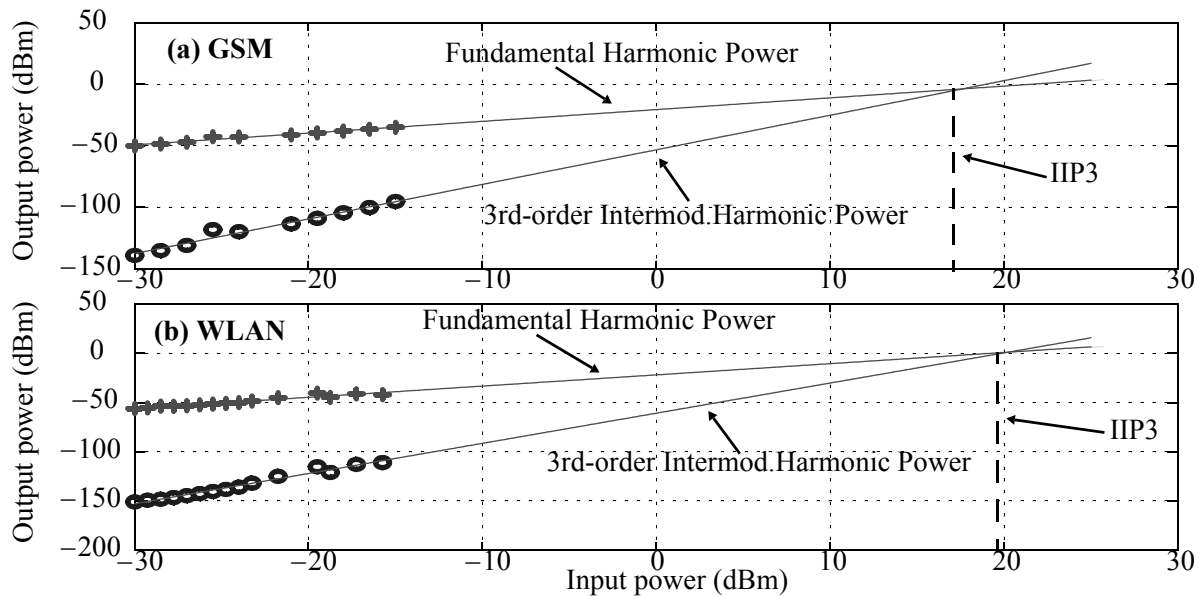
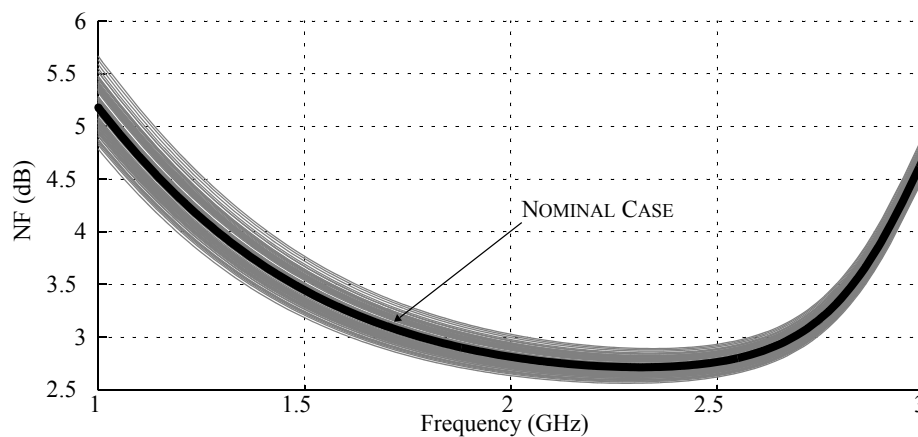

Figure 8. IIP3 for (a) GSM and (b) WLAN.

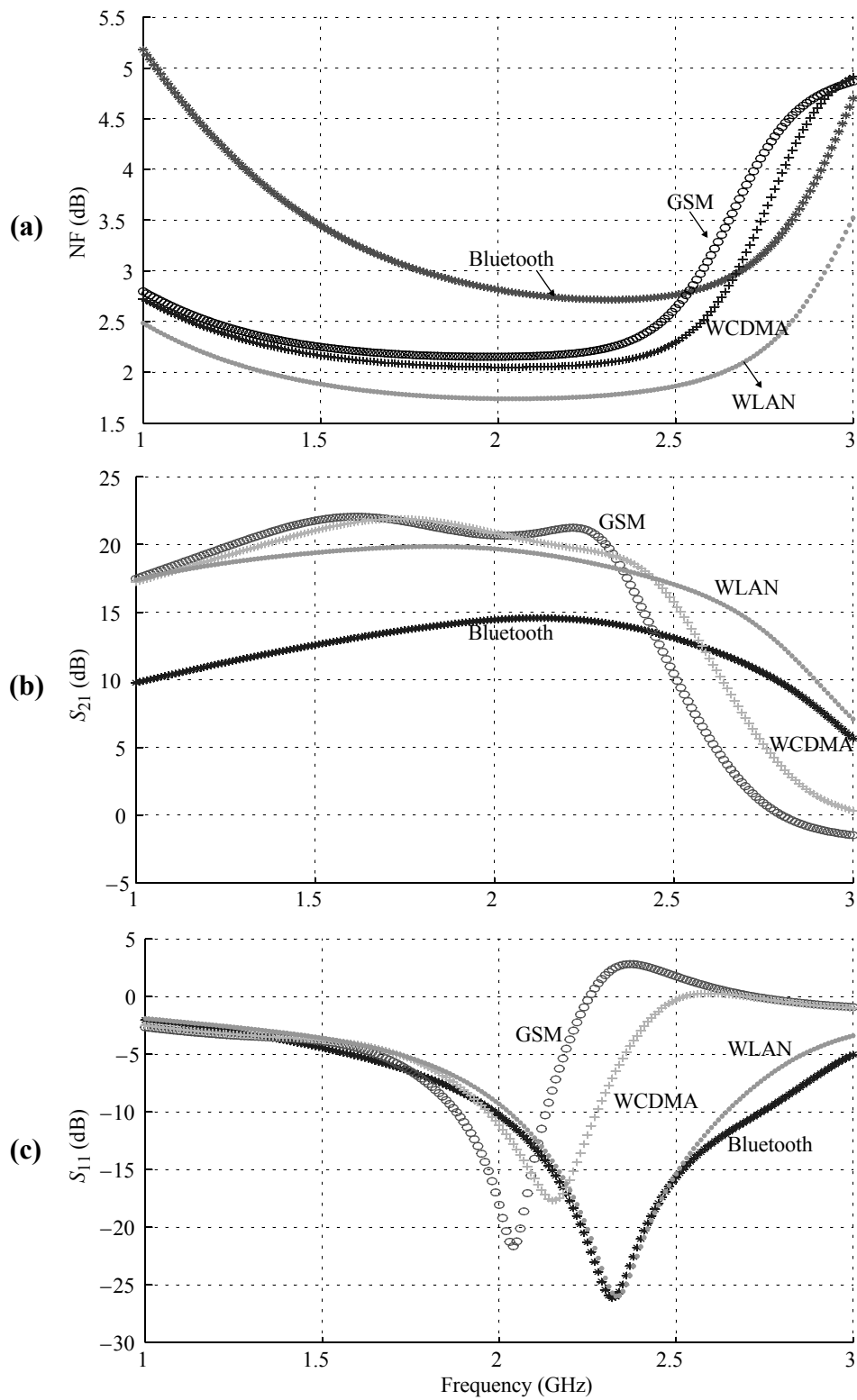Figure 9. MonteCarlo simulation of NF for Bluetooth standard.

Figure 7.   Simulation of NF and S-parameters. (a) NF. (b) S_{21}. (c) S_{11}.
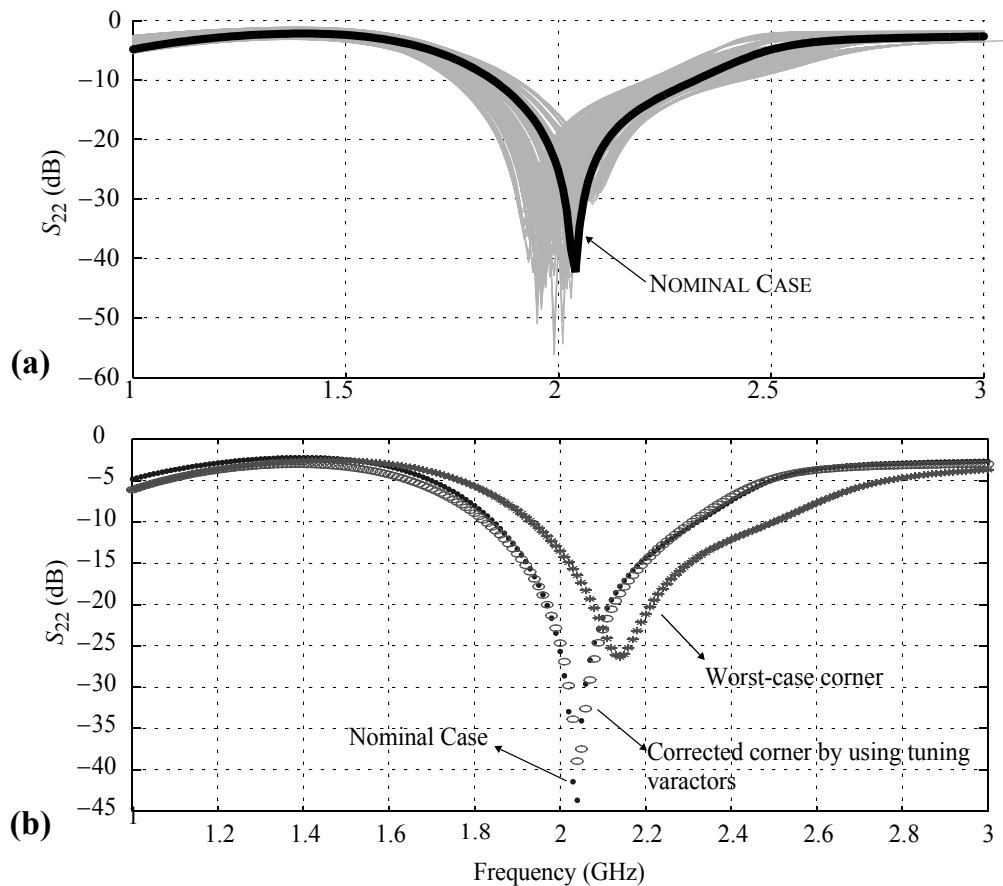
Figure 10. (a) Corner analysis of S_{22} for WCDMA. (b) Worst-case compensation by tuning.

Finally, Table 2 sums up the simulated performance of the LNA by showing the worst-case values of the different figures for each standard. This performance is compared with previous reported multi-standard CMOS LNAs[††], by using the following Figures Of Merit (FOM) [19]:

$$ \text{FOM}_1 = \frac{\text{Gain}}{(\text{NF-1}) \cdot \text{Power [mW]}}; \quad \text{FOM}_2 = \frac{\text{Gain} \cdot \text{IIP3 [mW]} \cdot f_c \text{ [GHz]}}{(\text{NF-1}) \cdot \text{Power [mW]}} \tag{3} $$

where f_c is the operating frequency of the LNA. Note that the circuit in this paper compares favourably to previous LNAs while covering a larger number of standards. Indeed, a very high value of FOM_2 is obtained as a consequence of the extremely high IIP3 achieved in the simulations (see Fig.8). In practice, measured IIP3 would be degraded as compared to simulations, giving rise to more realistic values of FOM_2.

[††] Although some LNAs in Table Table 2: (including the one in this paper) do not report experimental results, they are included in the comparison study for the sake of completeness. Those ones marked with * correspond to ICs showing experimental performance.

6. PRELIMINARY EXPERIMENTAL RESULTS

At the time of writing this paper, the prototype IC samples have been received and the test has been started. Fig.11(a) shows a chip microphotograph showing the main parts, namely integrated inductors, M-O-M capacitors and PADs. The chip is being tested using a PCB shown in Fig.11(b), that includes the necessary filtering for bias and power supplies as well as decoupling strategies and proper impedance termination to avoid signal reflections.

As an illustration, Fig.12 shows the measured S-parameters for the WCDMA standard, showing that S_{11} and S_{22} are below 015dB whereas the forward gain, S_{21}, is above 20dB, measured at ~2GHz. The effect of reconfiguration is shown in Fig.13 that depicts how measured S-parameters can be experimentally tuned for GSM, WCDMA and WLAN standards, showing that $S_{11,22} < 010$dB and $S_{21} > 18$dB for the standards considered.

Finally, NF has been also measured as illustrated in Fig.14. As can be seen, maximum values within the required bands is about 2dB larger than simulated value. This noise increment might be due to the measurement set-up and external noise sources that could be contaminating the chip. For that purpose, a Faraday cage is being fabricated in order to isolate the test chip as much as possible from external noise and interference sources in order to make a more precise measurement of NF.

Table 2: Comparison with Reported Multi-Standard CMOS LNAs

Ref.	Standard	NF (dB)	S_{21} (dB)	IIP3 (dBm)	f_c (GHz)	Power (mW)	FOM$_1$	FOM$_2$
10.	Bluetooth	2.2	15	3	2.4	7.2	1.2	5.7
	DECT	2.3	17	0.5	1.9	14.4	0.7	1.5
11.	WLAN IEEE 802.11 b-g	2.3	14	-1.5	2.4	50	0.1	0.01
	WLAN IEEE 802.11a	4.4	13	-1.5	5.3	50	0.05	0.2
	WiMAX	3.2	13.9	-10	3.5	50	0.09	0.03
12.	WCDMA	3.9	23.3	-6.3	2.1	9	1.1	0.5
	GSM	2.6	24.9	-21.6	0.95	9	2.4	0.02
13.*	DCS1800	5.2	28.5	-7.5	2.1	24	0.5	1
	WCDMA	5.6	23.4	0	2.4	24	0.2	0.2
	WLAN	5.8	23.4	-4.8	1.8	24	0.5	0.2
15.*	GSM	4.6	18	-12.8	1.9	32.4	0.1	0.02
	WLAN	4.4	24	-15.3	2.4	32.4	0.3	0.02
	Bluetooth	4.4	24	-15.3	2.4	32.4	0.3	0.02
16.*	0.3-2 GHz	4.5	12	-16	1.15	18	0.1	0.003
This Work	GSM	2.2	20.7	17.6	1.92	21.7	0.76	83.7
	WCDMA	2.1	19.9	17.5	2.05		0.7	84.3
	Bluetooth	2.8	13.3	10.9	2.44	17.4	0.3	8.8
	WLAN	1.8	17.2	19	2.44	21.7	0.6	126.1

(a)   **(b)**
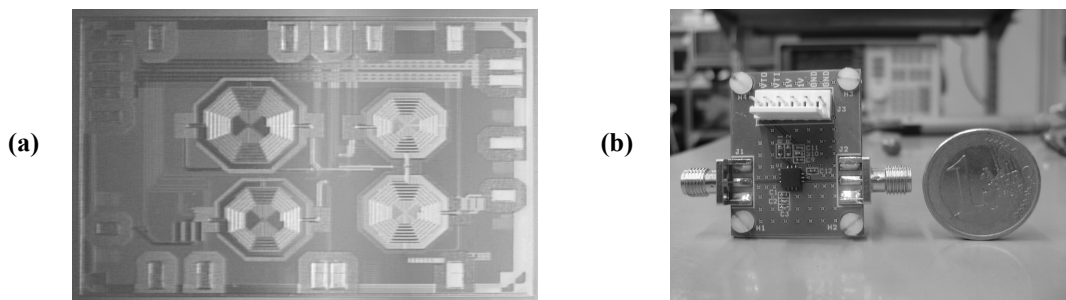
Figure 11. Chip Microphotograph and PCB.

(a)   **(b)**   **(c)**
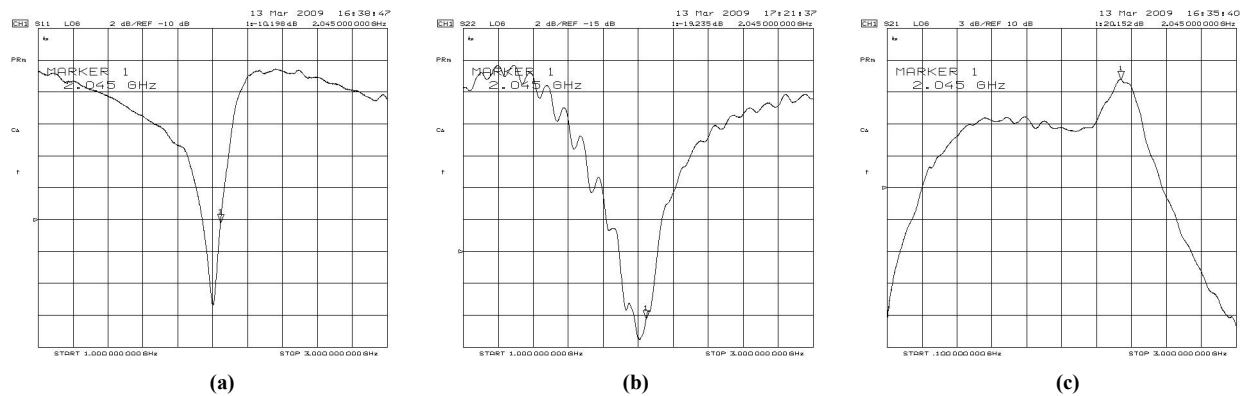
Figure 12. Preliminary measurements of S-parameters for the WCDMA standard configuration. (a) S_{11}. (b) S_{22}. (c) S_{21}.
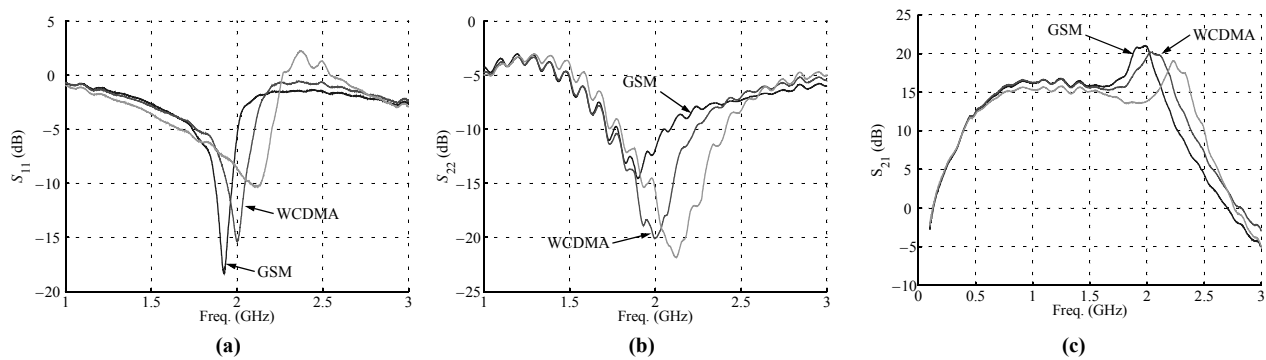

(a)   **(b)**   **(c)**

Figure 13. Preliminary experimental results showing the variation of S-parameters in the proposed reconfigurable LNA.
(a) S_{11}. (b) S_{22} and (c) S_{21}.

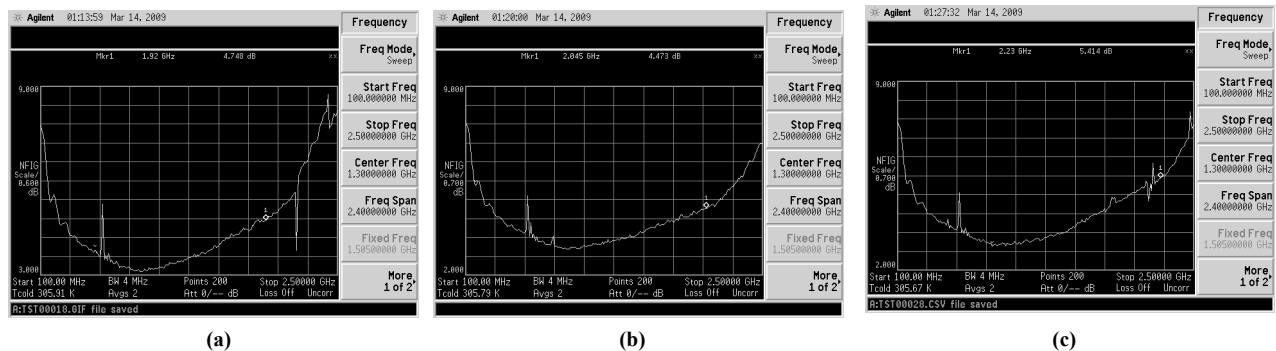

(a)   **(b)**   **(c)**

Figure 14. Preliminary measurements of NF for (a) GSM, (b) WCDMA and (c) WLAN.

CONCLUSIONS

The design and electrical implementation of a multi-standard 90-nm CMOS LNA has been presented. The use of reconfigurable loading and PMOS-varactor based tuning networks allows the amplifier to adapt its performance to the specifications of GSM, WCDMA, Bluetooth and WLAN standards. Simulation results including technology parasitics and packaging effects demonstrate a correct performance, showing a good comparison with previous reported designs. Preliminary experimental results show a correct operation of the circuit, demonstrating that the performance figures can be reconfigured within the desired frequency band.

ACKNOWLEDGMENTS

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