Guest Editorial Special Issue on Neural Networks Hardware Implementations

SINCE the very beginning of the neural network era, there has been the belief that to fully exploit the potential of this technology it would be necessary to also develop efficient hardware implementation techniques. In the last two decades, we have witnessed how the neural networks community is managing to acquire a more profound understanding of what neural networks can do and how. Neural networks knowledge has been enriched by developing more solid mathematical frameworks, by elaborating more efficient and powerful algorithms, by unfolding mysteries behind biological neural networks both at the individual neuron level and at different hierarchical levels of neuron ensembles and brain functions.

In the last decade, we have seen how the initial "euphoria" of neural network expectations has settled down to a solid knowledge and research capable of undertaking complex problems and providing powerful solutions. In the field of hardware implementations, progress has been continuing as well. The challenge has been and still is to follow what biology does and how, to be able to build more complicated and larger size systems, to implement efficient hardware learning techniques, to improve speed and/or lower power consumptions, to efficiently exploit or develop new signal/state representation techniques (e.g., continuous-time, pulse based, spiking nature, ...), to exploit noise and statistical properties, etc., and to apply all these ideas in real-world applications where efficient hardware solutions are necessary to provide compactness, high-speed and low-power consumptions.

In recent years significant progress in hardware solutions is being achieved. For this reason we believe it is a good point in time for a Special Issue on Neural Networks Hardware Implementations for the IEEE TRANSACTIONS ON NEURAL NETWORKS. The Special Issue Call for Papers had an overwhelming response. Originally, 70 papers were considered for possible publication. From those, 35 made it finally into the Special Issue. The review process was carried out by splitting the load between the four guest editors. The review process went quite smoothly thanks to the close cooperation between guest editors and the fast efficient response of reviewers. The final set of papers can be grossly classified into two main groups of similar size: the mainly digital papers and the mainly analog papers. Within the analog group are included also the mixed Analog–Digital implementation papers. Besides this main classification the subsequent subgroups are many times fairly arbitrary, because most of the times the possible classifications overlap depending upon different criteria. This reflects the richness of techniques, methodologies, and applications of neural hardware. We finally chose to classify them into the following groups.

A. Digital Neural Network Hardware

1) FPGA-Based Implementations: Quite impressive systems can be implemented using present day very powerful field-programmable gate arrays (FPGAs) commercial chips, as illustrated by the five papers in this category. Mehrtash *et al.* embrace a very sophisticated project involving Spiking Neurons. Anguita *et al.*discuss the Implementation of Support Vector Machines using FPGAs. Denby *et al.* apply FPGAs for very High Speed Pattern Recognition in High Energy Physics Experiments. Hikawa *et al.* exploit pulse mode techniques on FPGAs. Kim *et al.* use FPGAs for Blind Signal Separation and Active Noise Cancelling.

2) DSP-Based Implementations: Another interesting and powerful digital alternative is the use of commercial digital signal processing (DSP) chips, like in the two papers in this category. Venayagamoorthy *et al.*implement Neurocontrollers for Turbogenerator Power Systems, and Kehtarnavaz *et al.* perform Classification of Analog and Digital Modulation Signals.

3) ASIC-Based Implementation: More efficient and challenging tasks may require the design of special purpose application specific integrated circuits (ASICs). This is illustrated by the seven papers in this group. Bracco *et al.* demonstrate Hierarchical Vector Quantization (HVQ) combining an ASIC with commercial FPGAs. Hendry *et al.*implement an Intellectual Property (IP) core for a Self-Organizing Neural Network. Bermak *et al.* implement an impressive 3-D VLSI Classifier. Porrman *et al.*report on a very powerful implementation of Self-Organizing Feature Maps. Sato *et al.* implement a Stochastic Logic based Neurochip. Kocak *et al.* show a Spike based Random Neural Network Implementation. And Yagi *et al.* provide a Hardware Friendly Image Representation Algorithm for Neuro-Associative-Processor based Recognition Systems.

4) Mixed Digital Implementations: In this category, we have put a single paper in which Yang *et al.* compare FPGA, DSP, and ZISC implementations for Radial Basis Function (RBF) Neural Networks applied to face tracking/identification.

B. Analog Neural Network Hardware

1) Circuits and Components: In this category, we have those papers that emphasize circuits aspects of specific components. Gopalan *et al.* report on a Wide Range Euclidean

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Distance Circuit. Milev *et al.*show a Quadratic Nonlinearity Synapse and its application to a 2176 synapse neural matrix array for finger-print feature extraction. Hirose *et al.* provide a Recurrent Decision Circuit that improves convergence performance. Linares *et al.* report on mini-DACs based Calibrated Weighting Techniques.

2) Floating Gate MOS Techniques: Floating Gate MOSFET-based signal processing is a powerful, compact and very attractive technique for neural massive arrays. Beiu *et al.* provide an excellent overview on this topic applied to digital circuits or "Threshold Logic." Aunet *et al.* propose a design method based on Real-Time Reconfigurable Threshold Elements. Yamasaki *et al.* present a Soft-Pattern Matching Classifier using FGMOS technology.

3) Spiking Systems: In recent years, important progress has been made in spiking circuits and systems, which are very appealing because of their compactness, computational efficiency, circuit simplicity and biological flavour. Culurciello *et al.* discuss Address Merit Criteria and Tradeoffs for Address-Event Spike Communication Channels. Cosp *et al.* use a Neuromorphic Oscillatory Network for Scene Segmentation. Chicca *et al.*report on a learning network of Integrate-and-Fire Neurons. Asai *et al.* show a Competitive Frequency and Temporal Domain Neurochip of Integrate-and-Fire Neurons.

4) Active Waves and Central Pattern Generators: There are three papers in this very biologically inspired topic. Carmona *et al.* report on a complete 2-D Programmable Chip intended for Early Vision Applications. Serrano *et al.* exploit weak inversion MOS operation with Log-domain circuit techniques to reproduce those phenomena. Nakada *et al.* have developed a Central Pattern Generator analog chip for Quadrupled Locomotion.

5) Other Mixed Signal Systems: Finally in this category, we have included those papers that do not fit very well in the previous ones. Note that most of the previous papers could have been classified here as well. Kowalski reports a chip for Weighted Order Statistics Image Processing. Vidal *et al.* present a Neuro-Fuzzy Chip for handling complex tasks. Horio *et al.*introduce an impressive 10 000 Neurons Chaotic-based Chip. Kameda *et al.* present a Retina chip that includes bio-inspired Sustained and Transient Response channels. NG *et al.* show analog and digital implementations of Binary Relation Inference Networks for optimization problems. Finally Genov *et al.* report their Kerneltron chip which is a high speed Support Vector Machine.

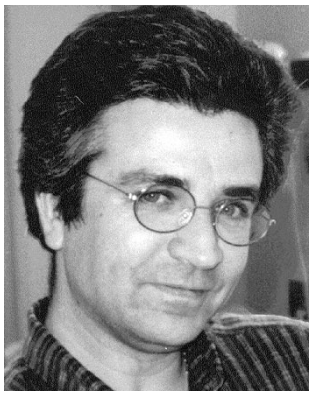
We may conclude that present day state-of-the-art in neural network hardware has reached an important level of maturity, where researchers and engineers are able to build very complex systems that can be applied to a variety of real-world problems.

BERNABÉ LINARES-BARRANCO, *Chief Guest Editor*
Instituto Microelectronica Sevilla (IMSE)
National Microelectronics Center, CNM-CSIC
Sevilla, 41012 Spain

ANDREAS G.ANDREOU, *Guest Editor*
Johns Hopkins University
Whitaker Biomedical Engineering Institute
Baltimore, MD 21218 USA

GIACOMO INDIVERI, *Guest Editor*
Swiss Federal Institute and the University of Zurich (ETHZ)
Institute of Neuroinformatics
Zurich, Switzerland

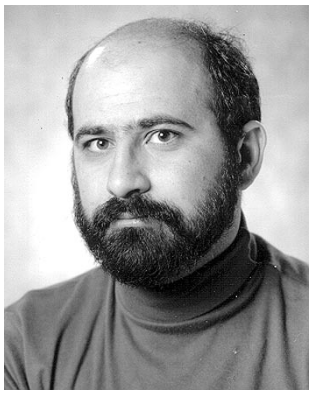
TADASHI SHIBATA, *Guest Editor*
University of Tokyo
Department of Frontier Informatics
Tokyo, Japan



Bernabé Linares-Barranco (S'90–M'93) received the B.S. degree in electronic physics in June 1986 and the M.S. degree in microelectronics in September 1987, both from the University of Seville, Seville, Spain. He received a first Ph.D. degree in high-frequency OTA-C oscillator design in June 1990 from the University of Seville, Spain, and a second Ph.D degree in analog neural network design in December 1991 from Texas A&M University, College-Station.

Since September 1991, he has been a Tenured Scientist at the "Sevilla Microelectronics Institute" (IMSE), which is one of the institutes of the "National Microelectronics Center" (CNM) of the "Spanish Research Council" (CSIC) of Spain. On January 2003 he was promoted to Tenured Researcher. From September 1996 to August 1997, he was on sabbatical leave at the Department of Electrical and Computer Engineering of the Johns Hopkins University, Baltimore, MD, as a Postdoctoral Fellow. During spring 2002, he was Visiting Associate Professor at the Electrical Engineering Department of Texas A&M University. He has been involved with circuit design for telecommunication circuits, VLSI emulators of biological neurons, VLSI neural-based pattern recognition systems, hearing aids, precision circuit design for instrumentation equipment, bio-inspired VLSI vision processing systems, transistor parameters mismatch characterization, Address-Event-Representation VLSI, RF circuit design, and real-time vision processing chips. He is coauthor of the book *Adaptive Resonance Theory Microchips* (New York: Kluwer, 1998).

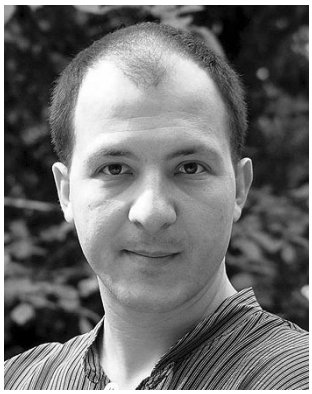
Dr. Linares-Barranco was corecipient of the 1997 IEEE TRANSACTIONS ON VERY LARGE SCALE INTEGRATION (VLSI) SYSTEMS Best Paper Award for "A Real-Time Clustering Microchip Neural Engine," and of the 2000 IEEE Circuits and Systems Society Darlington Award for the paper "A General Translinear Principle for Subthreshold MOS Transistors." He organized the 1994 Nips Post-Conference Workshop "Neural Hardware Engineering." From July 1997 until July 1999, he was Associate Editor of the IEEE TRANSACTIONS ON CIRCUITS AND SYSTEMS—PART II, and since January 1998 he is also Associate Editor for IEEE TRANSACTIONS ON NEURAL NETWORKS. He is Chief Guest Editor of the 2003 IEEE TRANSACTIONS ON NEURAL NETWORKS Special Issue on Neural Hardware Implementations.



Andreas G. Andreou (S'80–M'86) received the Ph.D. degree in electrical engineering and computer science from Johns Hopkins University, Baltimore, MD, in 1986.

Between 1986 and 1989, he was a Postdoctoral Fellow and Associate Research Scientist in the electrical and computer engineering department while also a member of the professional staff at the Johns Hopkins Applied Physics Laboratory. He became an Assistant Professor of Electrical and Computer Engineering in 1989, Associate Professor in 1993 and Professor in 1996. He is the founding director of the Whitaker lithography and fabrication facility at Johns Hopkins University‘. In 1995 and 1997, he was a Visiting Associate Professor and Visiting Professor, respectively, in the computation and neural systems program at the California Institute of Technology, Pasadena. In summer 2001, he was a Visiting Professor at Tohoku University, Japan. He now holds appointments in the electrical and computer engineering, computer science and Whitaker Biomedical Engineering Institute. His research interests include integrated circuits, sensory information processing and neural computation. He is a coauthor of *Adaptive Resonance Theory Microchips* (New York: Kluwer, 1998) and Associate Editor of the *Journal Neural Networks*.

Dr. Andreou is a recipient of a National Science Foundation Research Initiation Award and he is the co-founder of the Center for Language and Speech Processing at Johns Hopkins University. He was the corecipient of the 2000 IEEE Circuits and Systems Society Darlington Award.



Giacomo Indiveri received the Master degree in electrical engineering from the University of Genoa, Italy, in 1992 and won a postgraduate fellowship within the "National Research Program on Bioelectronic Technologies" from which he graduated (*cum laude*) in 1995.

He is a Research Assistant at the Institute of Neuroinformatics of the Swiss Federal Institute and the University of Zurich (ETHZ), Switzerland. From 1994 to 1996, he worked as a Postdoctoral Fellow in the Department of Biology at the California Institute of Technology, Pasadena, on the design of analog VLSI neuromorphic devices for low-level visual tasks and motion detection. His current research interests include the design and implementation of neuromorphic systems for modeling selective attention neural mechanisms, and for exploring the computational properties of networks of silicon integrate and fire neurons. He is a co-teacher of two classes on the analysis and design of analog VLSI Neuromorphic Systems at the Swiss Federal Institute of Zurich, coorganizer of the Workshop on Neuromorphic Engineering, held annually in Telluride, and coauthor of the book *Analog VLSI, Circuits and Principles* (Cambridge, MA: MIT Press).

Tadashi Shibata (M'79) was born in Hyogo, Japan, on September 30, 1948. He received the B.S. degree in electronic engineering and the M.S. degree in material science both from Osaka University, Osaka, Japan, and the Ph.D. degree from the University of Tokyo, Tokyo Japan, in 1971, 1973, and 1984, respectively.

From 1974 to 1986, he was with Toshiba Corporation, where he worked as a researcher on the R&D of VLSI device and processing technologies. He was engaged in the development of microprocessors, EEPROMs and DRAMs, primarily in the process integration and the research of advanced processing technologies for their fabrication. From 1984 to 1986, he worked as a production engineer at one of the most advanced manufacturing lines of Toshiba. During the period of 1978 to 1980, he was a Visiting Research Associate at Stanford Electronics Laboratories, Stanford University, Stanford, CA, where he studied laser beam processing of electronic materials including silicide, polysilicon, and superconducting materials. From April 1986 to May 1997, he was Associate Professor at the Department of Electronic Engineering, Tohoku University and was engaged in the research and development of ultraclean technologies. His main interest was in the area of low-temperature processing utilizing very-low-energy ion bombardment for promoting thin-film growth processes as well as in the development of the ultraclean ion implantation technology to form defect-free ultrashallow junctions by low-temperature annealing. Since the invention of a new functional device Neuron MOS Transistor (nMOS) in 1989, he has been engaged in the development of new-concept circuits and systems working in analog-digital merged decision-making principle. In May 1997, he became Professor at the Department of Information and Communication Engineering, The University of Tokyo, Japan. Since April 1999, he has been Professor at the Department of Frontier Informatics, School of Frontier Science, The University of Tokyo. His current research interest is the development of human-like intelligent VLSI systems based on the psychological model of a brain.

Dr. Shibata served as the Editor-in-Chief of *IEICE Transactions in Electronics* from 1997 to 1999 and as the Editor-in-Chief of the *Japanese Journal of Applied Physics* (JJAP) from 2000 to 2002. He is a member of the Japan Society of Applied Physics, the Institute of Electronics, Information and Communication Engineers (IEICE), and the IEEE Electron Devices Society, Circuits and Systems Society, and Computer Society.