Design Methodology for FPGA Implementation of Lattice Piecewise-Affine Functions

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- A piecewise-affine (PWA) function provides a linear (affine) output for each region in which the input domain, D, is partitioned.
- The lattice approach [1]
  - allows the implementation of any continuous PWA function.
  - selects the affine function without evaluating the boundaries.
- The algorithm extracts the lattice PWA representation using:
  - a simplied structure matrix ➔relation between regions
  - A simplied parameter ➔ affine regions

[1] C. Wen et al., Analytical expression of explicit MPC solution via lattice piecewise-affine function , Automatica, vol. 45, no. 4, pp. 910-917, 2009.

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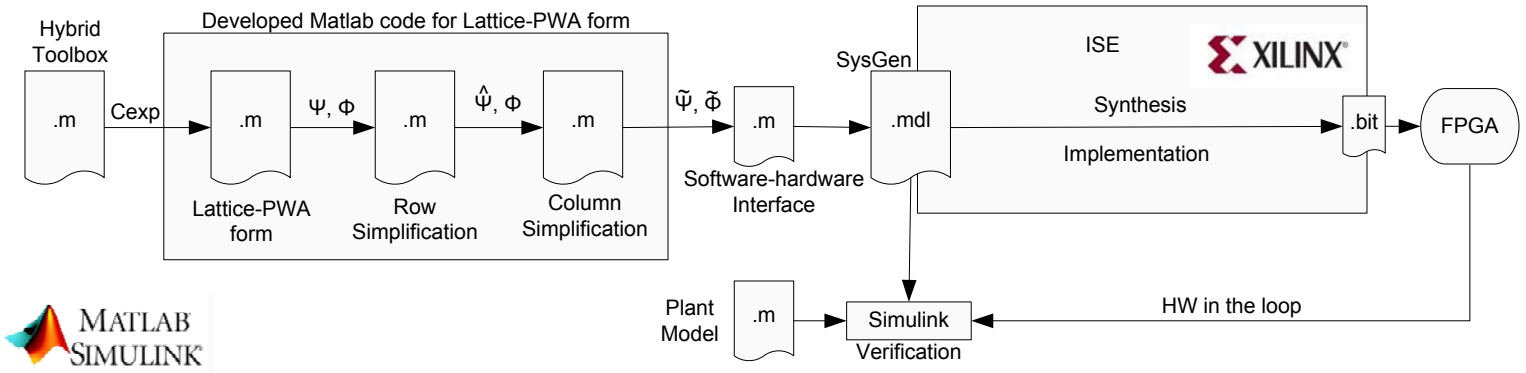

- The design methodology presented for FPGA implementation of continuous PWA functions based on lattice representation has been automated with Matlab&Simulink and ISE tools.
- The parameters required by the digital architecture are obtained from the algorithmic description of the problem.
- FPGA implementation results for applications in the control domain offer small size, high speed, and potentially no approximation error with regards to the optimum solution.