Multi-objective Performance Optimization of Planar Inductors

Abstract—Inductors play an essential role in the design of RF circuits. The parasitic effects plaguing integrated planar inductors require an accurate modeling and the careful exploration of their performance trade-offs. In this paper, a multi-objective performance modeling technique of planar inductors is presented, that supports both top-down and bottom-up design of RF circuits.

I. INTRODUCTION

The trend towards highly integrated wireless transceivers has motivated a growing need for an accurate modeling of inductances in RF circuits. Performance modeling techniques become a key factor to enable both conventional top-down design methodologies as well as emerging bottom-up design methodologies.

The behavior of integrated inductors is characterized by its equivalent inductance (L\text{eq}) and quality factor (Q\text{eq}). For illustration’s sake, Fig. 2 shows the equivalent inductance and quality factor of the inductor in Fig. 1. The most important performance characteristics of inductors are the extrapolated dc inductance, the quality factor at the frequency of interest, the self-resonance frequency (the frequency at which the inductor behavior becomes capacitive) and the inductor area. Most of the inductor performances are conflicting among them, i.e., any of them cannot be improved if some other is not worsened. Exploration of these trade-offs is essential for high-performance RF IC circuit design.

Section II in this paper reviews the possible approaches that can be followed both for manual design and CAD-supported methodologies. The proposed approach is presented in Section III and some experimental results are shown in Section IV.

II. PREVIOUS APPROACHES

When addressing RF IC design including planar inductors, the designer does not have many choices. The performance of these inductors is limited by numerous parasitic effects. A first option is to resort to analytical equations relating the inductor design parameters to the inductor performances. A number of approaches to the analytical modeling of planar inductances have been reported, with different level of accuracy and complexity [1]-[4]. But all of them represent a first-order approximation for initial rough design. Therefore, lengthy and unpredictable redesign iterations are necessary with full-wave electromagnetic solvers.

Fig. 1. Symmetrical square inductor.

Fig. 2. Equivalent inductance and quality factor for the inductor in Fig. 1.
Therefore, in most cases, the RFIC designer just resorts to the silicon-proven library of inductors provided by the corresponding foundry. In general, the library offer is very limited. For illustration's sake, the inductor library of a commercial 0.35µm CMOS technology contains 3 inductor types with 29, 7 and 14 inductors respectively. As these inductors must cover all possible performance combinations of inductance, quality factor and self-resonance frequency, the designers' choice is quite limited. When the library of inductors is used in automated design methodologies, e.g., [5],[6], the search space is very limited, yielding suboptimal results.

The design kits of some modern technology processes have considerably improved the support to the RF circuit designer. For example, a modern commercial 90nm CMOS technology offers a tool that provides the inductance, quality factor and self-resonance frequency for any inductor size. To provide this information, the foundry applied electromagnetic simulation to a high number of inductors of different sizes. Then regression techniques were applied to map the inductor parameter space to the inductor performance space. However, this approach has some limitations. First, the application of regression techniques introduces a fitting error in the performance evaluation. Second, the performance of all inductors, good or bad, are approximated, as the input inductor sizes are decided by the user. This makes the regression technique much harder and inaccurate as the complete parameter space must be modeled. However, for synthesis purposes we are only interested in the best performance trade-offs that the technological process can offer. Another consequence is that the search space must be necessarily reduced. For instance, all turn widths of spiral planar inductors must be equal, whereas it is known than inductors with different turn widths can improve the quality factor [7].

These problems are confirmed by the approach followed in [8], where an artificial neural network is used to model the mapping of inductor design parameters to inductor performances. For the fitting to become feasible, the search space must be discretized with a coarse grid for diameter of inner hole, number of turns, and turn width and spacing.

III. PROPOSED APPROACH

Analytical equations have not shown to provide enough accuracy for our purposes. Therefore, we intend to use full-wave electromagnetic simulation (EM) of the planar inductor structures.

The approaches followed by the tools provided by some foundries, that map inductor parameters to inductor performances, are not considered appropriate. The reason is that the complete parameter space is mapped to the performance space. This is necessary to quickly evaluate the inductor geometries provided by the foundry user. But we are only interested in the best performances that the process technology can offer. For the exploration of the corresponding trade-offs we will rely on its formulation as a multi-objective

![Fig. 3. Flow for inductor performance front generation.](image)
A multi-objective optimization problem can be mathematically formulated as:

\[
\begin{align*}
\text{Minimize} & \quad f(x); \quad f(x) \in \mathbb{R}^k \\
\text{such that:} & \quad g(x) \leq 0; \quad g(x) \in \mathbb{R}^m \\
\text{where} & \quad x_{i_{1}} \leq x_i \leq x_{i_{2}}, \quad i \in [1, p]
\end{align*}
\]  

The goal of multi-objective optimization is to provide the best trade-offs among the objectives, \( f(x) \).

A powerful solution to this kind of problems is provided by multi-objective evolutionary algorithms. Most of them are based on the concept of Pareto dominance. Given the minimization problem in (1), a solution \( x_A \), is said to dominate another solution \( x_B \), if \( f(x_A) \leq f(x_B) \) and the “<” relation verifies for at least one function \( i \). Solution \( x_A \) is said to be non-dominated if no other solution dominates it. The non-dominated set of the feasible search space is usually known as the Pareto-optimal front.

The proposed approach is illustrated in Fig. 3. The optimization process is based on the population-based multi-objective optimization algorithm NSGA-II [9], although any other would fit in the flow. At each generation of the optimization algorithm, a new set of inductor design parameters is generated. Different Cadence p-cells corresponding to different layout topologies are available, as shown in Fig. 4. The corresponding cells are instantiated and exported in GDSII format. This format is automatically transformed into a ADS-compatible layout format. The obtained inductors are then simulated with the EM simulator ADS Momentum. The key performances are extracted from the EM simulation and fed back to the optimizer.

Considering that an EM simulation typically takes in the order of minutes and that a few thousand simulations may be necessary to approximate the performance front, computation time may rise up to several days. However, two considerations must be taken into account. The first one is that the front generation process is easily parallelized. The second one is that the inductor performance fronts can be generated a priori, much before they are needed. Once generated, the front information can be stored and used whenever necessary.

IV. EXPERIMENTAL RESULTS

In this Section several inductor performance fronts are obtained for the symmetrical square inductor in Fig. 4(d). In all cases, a 0.35\( \mu \)m standard CMOS technology is used.

A. Inductance vs. area

A useful experiment to evaluate the capabilities of a technology process is to explore the inductance value that can be obtained for a given area. Therefore, in a first experiment we will consider only these two objectives. The design variables are the number of turns, the diameter of the inner hole, the turn width and the spacing among turns. The number of generations was set to 100. All optimization parameters of NSGA-II are set to their default values. The inductance vs. area trade-off is shown in Fig. 5. Inductors with different number of turns have been marked with different symbols and color.

B. Inductance vs. quality factor

In this case we wish to explore the trade-offs of inductance and quality factor for a fixed inductor area. The inductance and quality factor are measured at a frequency of 2.5GHz. Additional constraints are imposed to ensure that the inductance is sufficiently flat from dc to slightly above that frequency, and that the maximum of the quality factor is slightly above that frequency so that the self-resonant frequency is sufficiently above the working frequency. The obtained trade-offs for three different inductor areas are shown in Fig. 6.

C. Inductance vs. quality factor vs. area

Finally, a three-dimensional performance front generation is performed to obtain the trade-offs between inductance, quality factor and area. Again, inductance and quality factor are measured at 2.5GHz, the inductance is flat from dc to slightly above that frequency and the self-resonance frequency must be well above the frequency of operation.
The multi-objective optimization results are shown in Fig. 7. In this figure, the black points correspond to the optimal inductors arising from the optimization process. For better three-dimensional visualization a surface has been interpolated using spline interpolation. It must be noticed that this surface is obtained just for better visualization and many of its points may not correspond to real, feasible inductor designs.

V. CONCLUSIONS

Multi-objective optimization and full electromagnetic simulation has been coupled to generate accurate performance trade-offs of planar inductors. Future work includes the interpolation of the performance fronts and its evaluation in bottom-up synthesis methodologies.

REFERENCES


