A comparative study of low-noise amplifiers for neural applications

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Abstract – This paper presents a comparative study of three low-noise amplifiers for neural recording applications. The topologies are thoroughly analysed in terms of area, power consumption and noise performance. Further, the theoretical results are confirmed by simulations of transistor-level implementations in a 0.13μm CMOS technology at 1.2V supply voltage.

Index Terms – Amplifier, low power, low noise, neural recording, biomedical applications.

I. INTRODUCTION.

During the last years, there has been a growing interest on the design of neural recording interfaces with wireless transmission capabilities for the untethered measurement of brain activity [1-3]. These interfaces are expected to play a significant role both in clinical (as part of therapeutic procedures in patients with neurological diseases) and neuroscience applications. These systems are essentially composed by a set of microelectrodes to capture the neural activity, followed by a bank of low-noise amplifiers (LNAs) for signal conditioning and a mixed-signal circuitry to digitize and process the acquired data prior to wireless transmission. A key element in this architecture is the LNA which must be able to boost the weak signals detected by the microelectrodes and filter out the undesired frequency components, under severe area and power consumption constraints.

Different proposals can be found in the literature to efficiently solve the challenging noise-power-area trade-off demanded by neural LNAs [4-7]. In this paper, three of these approaches are reviewed and evaluated, paying special attention to their noise performances. Focus will be made in those realizations at transistor-level realizations in a 0.13μm CMOS technology for a 1.2V supply voltage. At the light of the theoretical treatment and the electrical simulations presented in the previous sections, Section IV summarizes the results of the comparative study.

II. LOW NOISE AMPLIFIER TOPOLOGIES

Table I shows the three topologies for neural spike recording considered for analysis. They are referred to as Capacitive Feedback Network (CFN) [1],[2],[5],[7], Miller Integrator Feedback Network (MIFN) [4] and Capacitive Amplifier Feedback Network (CAFN) [6] amplifiers. Assuming that all the Operational Transconductance Amplifiers (OTAs) are described by single-pole networks, the transfer functions of the three topologies are given by:

\[ H_{CFN}(s) \approx \frac{G(1+s/z_H)}{1+p_L(1+s/p_H)} \]

\[ H_{MIFN}(s) \approx \frac{G(1+s/z_I)}{1+p_L(1+s/p_H)} \]

\[ H_{CAFN}(s) \approx \frac{Gs}{1+p_L(1+s/p_H)} \]

where the poles \((p_L, p_H)\), zeros \((z_I, z_H)\) and DC gains \(G\) are defined in the second column of Table I under the usual assumptions expressed in the third column. The transfer functions in (1) have bandpass characteristics with a passband midgain, \(A_{sp}\), also defined in the second column of Table I. The fourth column gives expressions for the input-referred thermal noise, \(V_{rms}\), of the three structures, taking into account the contributions from the OTAs and the feedback resistors, \(R_f\). Parameter \(n\) stands for the transistor slope factor [9] and \(\gamma\) amounts 1 for single-ended and 2 for fully-differential amplifiers.

The fourth column of Table I also includes expressions for the theoretical limit of the LNA noise efficiency factor defined as [10]:

\[ NEF = \frac{V_{rms}}{\sqrt{2I_{tot}nU_i}} \frac{1}{4kT \cdot BW} \]

where \(I_{tot}\) is the total supply current of the LNA,

1. OTAs are characterized by their transconductances, \(g_{m,x}\); output resistances, \(R_o\); capacitances \(C_{g,x}, C_{m,x}\) at the input and output terminals, respectively; and noise excess factors \(\eta_x\) [11]. Sub-index \(x = 1, 2\) points out to amplifiers \(A_1\) or \(A_2\).
TABLE I. NEURAL AMPLIFIERS PERFORMANCE SUMMARY.

<table>
<thead>
<tr>
<th>Topology</th>
<th>Poles &amp; Zeros</th>
<th>Assumptions &amp; Parameter Definitions</th>
<th>Noise performance</th>
</tr>
</thead>
<tbody>
<tr>
<td>CFN</td>
<td>$G = -C_f R_f$, $z_e = 0$, $z_H = -g_m / C_f$, $p_L \approx -1 / R_f C_i$, $p_H \approx -g_m / A_m C_{t1}$, $A_m = -C_f / C_f$</td>
<td>$A_0, \beta \gg 1$, $A_m \gg 1$</td>
<td>Input-referred noise $V_{rms}$</td>
</tr>
<tr>
<td></td>
<td>$\frac{K T}{n q A_m C_i} + \frac{n}{2 C_{t1}} (1 + \eta_1)$</td>
<td>Minimum theoretical NEF</td>
<td></td>
</tr>
<tr>
<td>MIFN</td>
<td>$G = -1 / A_o 2$, $z_e = 0$, $z_H = -C_f R_f$, $p_L \approx -A_m / R_f C_i$, $p_H \approx -g_m / A_m C_{t1}$, $A_m = -A_o$</td>
<td>$g_m R_f / 1$, $g_m R_f / 1$</td>
<td>Input-referred noise $V_{rms}$</td>
</tr>
<tr>
<td></td>
<td>$A_o 1 \approx 1$, $A_o 2 \approx 1$, $g_m / C_{eq2} \approx \psi_2$, $C_{t1} = C_i + C_{po1}$, $C_{t2} = C_{po2} + C_{po1}$, $C_{eq2} = C_{po2} + C_{po1}$, $\beta = C_i / (C_{po2} + C_i)$</td>
<td>$\frac{K T}{A_m C_i} + \frac{n}{2 C_{t1}} (1 + \eta_1 + \psi_2)$</td>
<td>Minimum theoretical NEF</td>
</tr>
<tr>
<td>CAFN</td>
<td>$G = -R_f C_3$, $z_e = 0$, $z_H = -C_f R_f$, $p_L \approx -C_f / C_{t1} C_f R_f$, $p_H \approx -g_m / A_m C_{t1}$, $A_m \approx C_f / C_4$</td>
<td>$g_m R_f / C_{t1} C_4$, $g_m R_f / C_{t1} C_4$</td>
<td>Input-referred noise $V_{rms}$</td>
</tr>
<tr>
<td></td>
<td>$A_o 1 \approx (C_2 C_4) / (C_1 C_4)$, $A_o 2 \approx 1$, $g_m / C_{eq2} \approx \psi_2$, $C_{t1} = C_3 + C_4 + C_p$, $C_{eq2} = C_p 2 + C_{po1}$, $C_{po2} = C_2 / \beta_2$</td>
<td>$\frac{K T}{A_m C_i} + \frac{n}{2 C_{t1}} (1 + \eta_1 + \psi_2)$</td>
<td>Minimum theoretical NEF</td>
</tr>
</tbody>
</table>

$U_t = K T / q$ is the thermal voltage, and $BW$ stands for the LNA bandwidth which is essentially determined by the high-frequency pole, $p_H$, as

$$BW = g_m 1 / (2 \pi A_m C_{t1})$$

In the following, such NEF theoretical limits are explicitly derived for each LNA topology.

A. NEF for the CFN LNA

Assuming that the input differential pair of the OTA is biased in weak inversion with a tail current, $I_{tot1}$, the total supply current of the CFN LNA can be approximated by the expression

$$I_{tot} = I_{tot1} = k_1 n g_m U_t (1 + IC_1 i + 1)$$

where $k_1$ is an OTA-topology factor, and $IC_1$ is the inversion coefficient [12]. Replacing (3) and (4) into (2), taking also into account the expression for the input referred noise, $V_{rms}$, in Table I, it can be found that

$$NEF_{CFN} = \sqrt{n g_m (1 + IC_1 i + 1)}$$

where it has been assumed that $IC_1 \ll 1$. Given that typically $C_1 \approx C_{t1}$, the above expression can be further approximated as,

$$NEF_{CFN} \approx n g_m (1 + IC_1 i + 1)$$

B. NEF for the MIFN LNA

In this topology, the total supply current is determined by the sum of the current consumptions of the two OTAs. Assuming weak inversion operation,
\[ I_{to1} + I_{to2} \approx 2(k_1 + \alpha k_2)g_{m1}U_i \]  
where \( \alpha = \frac{g_{m2}}{g_{m1}} \) and the last approximation assumes low inversion coefficients, \( IC_1, IC_2 \ll 1 \). 
Replacing (3) and (7) into (2), and taking into account the input referred noise, \( V_{rms} \), in Table I, it can be found that 
\[ NEF_{MIFN} = \frac{1}{2} n \sqrt{k_1(1 + \eta_2)} \left( 1 + \eta_1 + \psi_2 \right) \] 
where it has been assumed that \( C_f > C_1 \). By derivating (8) with respect \( \alpha \), and equating to 0, it can be shown that \( NEF_{MIFN} \) is minimized if the transconductance ratio satisfies the condition: 
\[ \alpha = \frac{1}{\beta} \left( \frac{k_1(1 + \eta_2)}{k_2(1 + \eta_1)} \right) \] 
Replacing (9) into (8), the minimum noise efficiency is thus given by: 
\[ NEF_{MIFN} = \frac{1}{2} \frac{1}{\sqrt{n}} \sqrt{k_1^2(1 + \eta_1) + k_2^2(1 + \eta_2)} \] 
(C. NEF for the CAFN LNA)

As can be observed in Table I, in this topology the noise contribution of amplifier \( A_2 \) is divided by a factor \( (C_1^2 / C_4)^2 \). Therefore, a large \( C_1 \) value must be chosen for decreasing noise. Under this condition, CAFN exhibits a performance similar to the CFN architecture with a \( NEF \) given by, 
\[ NEF_{CAFN} = \frac{1}{2} \frac{1}{\sqrt{n}} \sqrt{k_1^2(1 + \eta_2)} \left( 1 + \frac{k_2 g_{m2}^2}{k_1 g_{m1}} \right) \] 

III. TRANSISTOR-LEVEL EXPLORATION

In order to quantify the pros and cons of the previous LNA topologies, we have realized a transistor-level implementation of the architectures in a 0.13µm CMOS technology. Common design objectives for the three topologies, assumed single-ended, are a midband gain of 47dB and an operation bandwidth from 250Hz to 7kHz. In all cases, a cascode current mirror amplifier [see Fig. 4(a)] has been used to implement \( A_1 \) OTAs whereas, a less noisy telescopic amplifier [see Fig. 4(b)] has been selected for the \( A_2 \) OTAs. OTA-related parameters are \( \eta_1 = 1.5 \) and \( k_1 = 2 \) for the current mirror amplifier, and \( \eta_2 = 0.5 \) and \( k_2 = 1 \) for the telescopic OTA.

Given these target specifications, the transistor-level exploration (applied to each LNA topology) has consisted on identifying that configuration which obtains the minimum area occupation for a given input-referred noise value. Additionally, the \( NEF \) is constrained to be no higher than 8% the minimum theoretical \( NEF \) derived in Section II. It is worth noting that, for a fixed bandwidth and noise level, a low \( NEF \) value also implies a reduced power consumption according to (2).

As an illustration, Fig. 5 depicts the transistor-level synthesis routine used for the CFN LNA (similar algorithms have been also developed for the other LNAs). The procedure uses as design variables the feedback, \( C_f \), and load, \( C_1 \), capacitances, and the inversion coefficient of the amplifier \( IC_1 \). These variables also act as running parameters in a optimization loop which evaluates at every iteration the accomplishment of the target specifications and select that valid configuration with the minimum power consumption. The sizing procedure starts by guessing initial values for the OTA parasitic capacitances, \( C_{m1}, C_{p1}, \) and DC-gain, \( A_{o1} \). Using these values, the feedback factor, \( \beta \), and equivalent closed-loop capacitance, \( C_{eq1} \), are computed and, thereafter, the transconductance, \( g_{m1} \), and feedback resistor, \( R_f \), based on bandwidth specifications. A transistor-level sizing routine, similar to that reported in [13], is then run to accurately estimate transistor sizes, bias currents and other electrical-level parameters of the LNA. This routine uses look-up tables of technology parameters, obtained from batches of electrical-level simulations, to complete the sizing task. At this point, the overall power consumption of the OTA, area (estimated in terms of the obtained sizes for transistors and capacitors), parasitics and DC-gain can be calculated. These values for the parasitics and DC-gain are compared to those originally estimated at the beginning of the procedure. If discrepancies (\( \Delta \)) are higher than a user-defined tolerance value, (\( \tilde{\delta} \)), the procedure is repeated again until
The results of the exploration are shown in Fig. 6, in which the power and area consumptions of the optimum solutions, as well as their NEFs, are represented against the input-referred noise. Plots are obtained from electrical simulations of the final configurations derived with the aforementioned synthesis routines. Observe that NEFs remain close to their minimum theoretical values: 4.25 for the CFN and CAFN LNAs, and 6.25 for the MIFN LNA. Also observe that, for a given input-referred noise, the CFN topology performs better in terms of area and power consumptions, contrary to what is claimed elsewhere [4], [6]. Furthermore, it can be noticed that the MIFN LNA obtains a noise efficiency factor higher than the remaining approaches due to the second OTA contribution.

Although the exploration has been realized for single-ended LNA topologies, similar conclusions can be drawn in the case of fully-differential structures, more suitable for low-voltage environments.

**IV. CONCLUSIONS.**

This paper compares the performance of three LNA topologies for neural spike recording applications. The study, based upon theoretical developments and transistor-level explorations, reveals that the CFN approach [1],[2],[5],[7] achieves the best performance in terms of area and power consumptions for a given input-referred noise specification.

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**REFERENCES**


