Basic Concepts and Architectures

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   - Single-bit single-quantizer architectures
   - Dual quantization
   - Multi-bit quantization
   - Bandpass ΣΔ modulators
4. Continuous-Time ΣΔ Modulators
   - Basic concepts and topologies
   - Synthesis methods
Introduction: Basic ADC process

- **Sampling process**
  - Limits the input signal frequency
  - Speed of the ADC

- **Quantization process**
  - Limits the input signal accuracy
  - Resolution of the ADC
Introduction: Resolution vs. conversion rate

CMOS ADCs

Resolution (bit)

Bandwidth (Hz)

Sigma-Delta

Pipeline

Flash, Folding, Interpolative

Other Nyquist ADCs

PRECISION MEASUREMENT

AUDIO

VOICE

BROADBAND WIRELINE COMMUNICATIONS

MOBILE COMMUNICATIONS

Nyquist ADCs

Introduction: Quantization

Midrise uniform quantization

Resolution (bits):
\[ B = \log_2(\text{# levels}) \]

Separation between adjacent input levels:
\[ X_{\text{LSB}} = \frac{X_{\text{FS}}}{(2^B - 1)} \]

Separation between adjacent output levels:
\[ \Delta = \frac{Y_{\Delta}}{(2^B - 1)} \]

Full-scale input range: \( X_{\text{FS}} \)

Gain:
\[ g_q = \frac{\Delta}{X_{\text{LSB}}} = \frac{Y_{\Delta}}{X_{\text{FS}}} \]
Introduction: Quantization

- Quantization input-output characteristic
  \[ y = g_q x + e_q(x) \]

- Quantization error

- White noise model
  - If \( x \) varies randomly from sample to sample
  - If the number of quantizer levels is high

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Introduction: Quantization - white noise model

- Probability Density Function
  \[ \rho_q(e) = \frac{1}{\Delta} \]

- Quantization error power
  \[ \sigma^2(e) = \frac{1}{\Delta} \int_{-\Delta/2}^{\Delta/2} e^2 de = \frac{\Delta^2}{12} \]

- Quantization error Power Spectral Density
  \[ S_E(f) = \frac{\sigma^2(e)}{f_s} = \frac{\Delta^2}{12f_s} \]
Introduction: Sampling

- **Oversampling**
  - Low-pass signals: $M = \frac{f_s}{2B_W}$
  - Band-pass signals: $M = \frac{f_s}{2(f_{IF} + B_W)}$ \(\approx\) \(\frac{f_s}{2B_W}\)

OSR = $M$ = Oversampling Ratio

- **Classification of ADCs**
  - Nyquist-rate ADCs ($M \sim 1$)
  - Oversampling ADCs ($M \gg 1$)

Fundamentals of $\Sigma\Delta$ ADCs: Oversampling

- **PSD of oversampled quantization noise**

- **In-Band Noise power (IBN or $P_Q$)**

$$P_Q = \int_{f_{IF} = B_W/2}^{f_{IF} = B_W/2} 2\cdot S_E(f)df = \frac{B_W}{6f_s} \cdot \frac{\Delta^2}{12M}$$
**Fundamentals of ∑Δ ADCs: Performance Metrics**

- **N-bit Nyquist-Rate ADC**
  - $f_s = f_N = 2B_w$
  - $SNR_{max} = 10\log_{10} \left( \frac{3}{2} (2^N - 1)^2 \right)$

- **B-bit Oversampled ADC**
  - $f_s = Mf_N (M > 1)$
  - $SNR_{max} = 10\log_{10} \left( \frac{3}{2} M(2^B - 1)^2 \right)$

\[
ENOB = \frac{SNR_{max} - 1.76}{6.02} = \log_2 (2^B - 1) + \frac{1}{2} \log_2 (M) \quad (N > 1)
\]

- **SNDR & SINAD:**
  \[
  SNDR(dB) = 10\log_{10} \left( \frac{P_{sig}}{P_Q + P_H} \right)
  \]

- **Effective Number Of Bits ENOB:**
  \[
  ENOB \approx \frac{SNDR - 1.76}{6.02}
  \]

- **SFDR:** Spurious-Free Dynamic Range

- **Harmonic Distortion:**
  - $HD_k$, $THD$
  - $IM_3$, $IP_3$
  - ...

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**Fundamentals of ∑Δ ADCs: Performance Metrics**

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  \]

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  \]

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- **Harmonic Distortion:**
  - $HD_k$, $THD$
  - $IM_3$, $IP_3$
  - ...

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**Fundamentals of ΣΔ ADCs: Quantization Noise Shaping**

- **Processing of the quantization error**
  
  \[ L = 1 \]
  \[ e_{q_{HP}}(n) = e_q(n) - e_q(n-1) \]
  \[ L = 2 \]
  \[ e_{q_{HP}}(n) = e_q(n) + e_q(n-2) - 2e_q(n-1) \]

- **In-band noise power and effective resolution**

  \[ N_{TF}(z) = (1 - z^{-1})^L \Rightarrow S_{E_{HP}} = |N_{TF}(f)|^2 S_E \]
  \[ P_{E_{HP}} = \int_0^{f_s/2} S_{E_{HP}}(f) df = \frac{\Delta^2}{12} \frac{\pi^2 L}{(2L+1)^2} \frac{M^{2L+1}}{2L+1} \]

  \[ N = \log_2 \left[ \frac{(2^B - 1)(2L+1)}{\pi^2 L} \right] + \left(L + \frac{1}{2}\right) \log_2(M) \]

**Fundamentals of ΣΔ ADCs: Basic ΣΔ ADC architecture**

- **ADC architecture**
  
  - **S/H**
  - **ΣΔ Modulator**
  - **DAC**
  - **Digital filter**
  - **Downsampler**
  - **Decimator**

- **Quad-ation noise (noise-shaping)**

- **Out-of-band components**

- **Anti-aliasing filter**
Fundamentals of $\Sigma\Delta$ ADCs: Nyquist-rate vs. $\Sigma\Delta$ ADCs

- HIGH-SELECTIVITY ANALOG FILTER for anti-aliasing
- Overall resolution obtained using HIGH-ACCURACY ANALOG BLOCKS
- LOW-SELECTIVITY ANALOG FILTER for anti-aliasing (1st/2nd order)
- High overall resolution obtained using LOW/MODERATE-ACCURACY ANALOG BLOCKS
- HIGH-SELECTIVITY DIGITAL FILTER

EASIER AND MORE ROBUST IN MODERN CMOS

Fundamentals of $\Sigma\Delta$ ADCs: Basic $\Sigma\Delta M$ architecture

- $H(z)$ with large gain within the signal band
- $STF(z) = \frac{g_b H(z)}{1 + g_b H(z)}$
- $NTF(z) = \frac{1}{1 + g_b H(z)}$

Within the signal bandwidth

$|STF(z)| = \frac{H(z)}{1 + H(z)} \rightarrow 1$
$NTF(z) = \frac{1}{1 + H(z)} \rightarrow 0$

$\Sigma\Delta$ Low-Pass

$Y(f)$

$\Sigma\Delta$ Band-Pass

$f_s/2$

In-band noise power, SNR and DR

$$P_Q = \begin{cases} \frac{\Delta^2}{6f_s} \int_{f_s/2-B_w/2}^{B_w} |N_{TF}(f)|^2 df & \text{for LP}\Sigma\Delta \\ \frac{\Delta^2}{6f_s} \int_{f_s/2-B_w/2}^{B_s} |N_{TF}(f)|^2 df & \text{for BP}\Sigma\Delta \end{cases}$$

SNR = $10\log_{10}\left(\frac{\Delta^2/2}{P_Q}\right)$

DR = $10\log_{10}\left(\frac{(X_{FS})^2/2}{P_Q}\right)$
Fundamentals of $\Sigma\Delta$ ADCs: Classification of $\Sigma\Delta$Ms

- Nature of the signals being handled: Low-pass vs. Band-pass
- Dynamics of the loop filter: Discrete-Time vs. Continuous-Time
- Number of bits of the embedded quantizer: single-bit vs. multi-bit
- Number of quantizers employed: single-loop, cascade, etc..
- Type of primitives available in the fabrication technology...

Fundamentals of $\Sigma\Delta$ ADCs: Basic control parameters

- $L$ th-order $\Sigma\Delta$M
- $Y(z) = z^{-L}X(z) + (1-z^{-1})E(z)$
- $STF(z) = \frac{g_zH(z)}{1+g_zH(z)}$
- $NTF(z) = \frac{1}{1+g_zH(z)}$
- $H(z)$ with large gain within the signal band
- Speed of analog circuitry
- Order of the shaping, $L$
- Stability of the $\Sigma\Delta$M
- Resolution of the internal quantizer, $B$
- Linearity of the DAC
Using a linear model for the quantizer

\[ Y(z) = z^{-1}X(z) + (1 - z^{-1})E(z) \]

\[ DR(\text{dB}) \geq 10\log_{10}\left(\frac{9M^2}{2\pi^2}\right) \]
**DT-ΣΔMs: 1st-order LP ΣΔ Modulator**

- **Noise pattern**

\[
\begin{align*}
e(n) &= x(n) - y(n) \\
u(n) &= u(n-1) + e(n) \\
y(n) &= \text{sgn}[u(n)]
\end{align*}
\]

**Table:**

<table>
<thead>
<tr>
<th>n</th>
<th>u</th>
<th>y</th>
<th>e</th>
<th>n</th>
<th>u</th>
<th>y</th>
<th>e</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>0</td>
<td>1</td>
<td>-1</td>
<td>0</td>
<td>1</td>
<td>-2/3</td>
<td>-1</td>
</tr>
<tr>
<td>1</td>
<td>-1</td>
<td>-1</td>
<td>1</td>
<td>-2/3</td>
<td>-1</td>
<td>4/3</td>
<td>-1/2</td>
</tr>
<tr>
<td>2</td>
<td>0</td>
<td>1</td>
<td>-1</td>
<td>2/3</td>
<td>1</td>
<td>-2/3</td>
<td>1</td>
</tr>
<tr>
<td>3</td>
<td>-1</td>
<td>-1</td>
<td>1</td>
<td>0</td>
<td>1</td>
<td>-2/3</td>
<td>1/2</td>
</tr>
<tr>
<td>4</td>
<td>0</td>
<td>1</td>
<td>-1</td>
<td>-2/3</td>
<td>-1</td>
<td>4/3</td>
<td>0</td>
</tr>
</tbody>
</table>

**Plot:**

- Relative Magnitude (dB)
- In-band

**DT-ΣΔMs: 2nd-order LP ΣΔ Modulator**

- **1st-order ΣΔ Modulator**

- **2nd-order ΣΔ Modulator**
### DT-ΣΔMs: 2nd-order LP ΣΔ Modulator

**Stability conditions:**

\[ g_{DAC_1} g_{x_1} g_d = 1 \]
\[ g_{DAC_2} = 2 g_{DAC_1} g_{x_2} \]

- **Linear analysis**

\[ Y(z) = z^{-2} X(z) + (1 - z^{-1})^2 E(z) \]

\[ P_Q \approx \frac{2 \alpha 4}{60 M^5} \Rightarrow DR \approx \frac{15 M^5}{2\pi^4} \]

- **Output spectrum and noise pattern**

#### 2nd-order ΣΔM

- Dependence on \( M \): 15 dB/oct.
- Example: digitize a 10kHz signal with 16 bits
  - \( M = 150 \) (\( f_s = 3 \) MHz) for a 2nd-order ΣΔM
  - \( M = 1500 \) (\( f_s = 30 \) MHz) for a 1st-order ΣΔM

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### DT-ΣΔMs: High-order Single-loop ΣΔ Modulators

#### 2nd-order ΣΔM

\[ Y(z) = z^{-2} X(z) + (1 - z^{-1})^2 E(z) \]

- Stable for inputs in \([-0.9\Delta/2, -0.9\Delta/2]\) if \( \xi_2 > 1.25\xi_1/\xi_2 \)

- High-order ΣΔM loops are only conditionally stable

#### Lth-order ΣΔM

- Pure differentiator FIR NTF

\[ \|NTF\|_\infty = 2^L \]

- Gain adjusted to satisfy Butterworth/Chbyshev poles

- Zeros at \( z = 1 \)

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**IIR NTFs**

\[ NTF(z) = \frac{(z-1)^L}{D(z)} \]

**Gain adjusted to satisfy**

\[ \|NTF\|_\infty \sim 1.5 \]
DT-ΣΔMs: High-order Single-loop ΣΔ Modulators

**OPTIMIZED IIR NTFs** [Schr93]

\[
\min \left[ \int_0^1 |\text{NTF}(f)|^2 df \right] 
\]

- Complex zeros at \( |z| = 1 \) with optimal positions within the signal band
- Butterworth/Chebyshev poles

**5th-order NTF** (OSR = 64)

![Graph showing the 5th-order NTF](image)

**IIR NTFs** [Lee87]

\[
\text{NTF}(z) = \frac{(z - 1)^L}{D(z)} 
\]

- Zeros at \( z = 1 \)
- Butterworth/Chebyshev poles

Gain adjusted to satisfy \( \|\text{NTF}\|_\infty < 1.5 \)

**DT-ΣΔMs: High-order Single-loop ΣΔ Modulators**

- Distributed feedback and distributed feedforward input

- Complexity (many feedback/feedforward coeffs)
- Large spread of coeffs (area, power)

**Feedforward summation + local resonators**

![Diagram showing feedforward summation and local resonators](image)
Systematic loss of resolution, but:

- Each stage re-modulates a signal containing the quantization error in the previous one.
- Digital processing is used to cancel out all quantization errors, but that in the last stage.

\[ NTF_i(z) = 0 \quad i = 1, ..., N - 1 \]

\[ Y(z) = z^{-dL} X(z) + d_{2N-1} (1 - z^{-1}) E_N(z) \]

- High-order stable operation is ensured by cascading low-order stages (\( L_i = 1, 2 \)).
- Relationships among ECL and \( \Sigma \Delta \) M to be fulfilled for perfect cancellation (Noise Leakage).

\[ P_0 = \frac{d_{2N-1}^2 \Delta_N}{12} \frac{z^{2L}}{(2L + 1) \text{OSR}^{2L+1}} \]

Properties:

- Smaller than for single loops
- Independent of OSR
- Small spread of analog coeffs
- ECL can be easily implemented
- Performance close to ideal
- Suited at low oversampling

\[ \Sigma \Delta \] MASH Ms:

- 4th-order 2-stage cascade
- 4th-order 3-stage cascade

Noise leakage precludes the cascading of a large number of stages to be practical.
DT-ΣΔMs: Multi-bit ΣΔ Modulators

- Increased dynamic range
  $B$ can trade for OSR (wideband)
- Better stability properties
  More aggressive high-order NTFs
- DAC non-linearities are directly added to the input
  The linearity of the ΣΔM will be no better than that

POSSIBLE APPROACHES

Correcting DAC errors
- Element Trimming
- Analog Calibration
- Digital Correction

Decorrelating DAC errors from the input
- DEM techniques

Introducing DAC errors at a non-critical position
- Dual quantization

Dynamic Element Matching (DEM)

- Elements selected to make DAC errors independent of the input signal
- Algorithms that try to average the error in each DAC level to zero
  (to push DAC errors to high freq.)
- Randomization: Distortion transforms into white noise
- Rotation: Distortion moves out of band (CLA)
- Mismatch-shaping: 1st/2nd order (ILA, DWA, DDS)
Dual Quantization
- Combines 1-bit and multi-bit quantizers (linearity/reduced error)

Concept applied to single-loop ΣΔMs [Hair91]
- Improved stability
- Noise leakage

Concept applied to cascade ΣΔMs [Bran91]
- Multi-bit quantization usually applied only in the last stage
- DAC errors shaped by L-LN
  - Relaxes DAC requirements
- Noise leakage (inherent to cascades)

DT-ΣΔMs: Dual-quantization ΣΔ Modulators

Analog Domain — Digital Domain

Analog quadrature mixer
(≡ I/Q mismatch, I/f noise, offset)
Two lowpass ADCs needed

Digital quadrature mixer
One IF (bandpass) ADC
Digital channel selection, gain control...

Digital mixing simplified for \( f_{IF} \neq f_s/4 \)
\[ Y(z) = S_{TF}(z)X(z) + N_{TF}(z)E(z) \]

\[ H_{bp}(z) = \left[ \frac{N_{RES}(z)}{(1-z^{-1}z_n)(1-z^{-1}z_n^*)} \right]^{-L} \]

\((N_{RES}(z) + (1-z^{-1}z_n)(1-z^{-1}z_n^*) = 1) \Rightarrow N_{TF}(z) = [1 - 2\cos(2\pi f_n T_s)z^{-1} + z^{-2}]^L\]

\[ P_Q = \frac{(\sin[2\pi f_n T_s])^{2L} \pi^2 X_{FS}^2}{12(2^N - 1)^2 (2L + 1) M^{2(L+1)}} \]

\[ DR = \frac{3(\sin[\pi f_n T_s])^{2L} 2(L+1) M^{2L + 1}}{2\pi^{2L} (\sin[2\pi f_n T_s])^{2L}} \]

\[ 6\text{th-Order BP (} L = 3 \text{)} \]
\[ 4\text{th-Order BP (} L = 2 \text{)} \]
\[ 2\text{nd-Order BP (} L = 1 \text{)} \]

\[ f_n = f_s / 4 \]

\[ 21\text{dB/oct} \]
\[ 15\text{dB/oct} \]
\[ 9\text{dB/oct} \]
**DT-$\Sigma\Delta$Ms: Bandpass $\Sigma\Delta$Ms - Signal band location**

- Trade-off at the IF Stage
  - The larger $f_n$, the lower $B_{af}$

- Trade-off at the RF Stage
  - The lower $f_n$, the lower $B_{1rf}$

- Optimum location for $f_n = f_s/4$ (at the middle of Nyquist band)
  - Forward path (analog) modulator filter realization can be simplified
  - Simplifies LP-to-BP transformation, $z^{-1} \rightarrow -z^{-2}$
  - Digital mixing to baseband is notoriously simplified:
    \[
    \cos(2\pi f \cdot f_T) = 1, 0, -1, 0, 1, 0, \ldots
    \]

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**DT-$\Sigma\Delta$Ms: LP-to-BP Transformation Method**

- L-order Lowpass $\Sigma\Delta$ Modulator
  - Lth-Order LP Filter
  - N-bit DAC
  - $z^{-1} \rightarrow z^{-2}$

- 2L-order bandpass $\Sigma\Delta$ Modulator
  - 2Lth-Order BP Filter
  - N-bit DAC

- $L$ zeroes at DC
- $L$ zeroes at $+f_s/4$
- $L$ zeroes at $-f_s/4$

- $S_{TF} = z^{-L}$
- $N_{TF} = (1 - z^{-1})^L$

- $SNR_Q = \frac{12(2^{B+1} - 1)(2L+1)2^L+1}{8\pi 2^L}$

- $S_{TF} = (-z^{-2})^L$
- $N_{TF} = (1 + z^{-1})^L$
DT-$\Sigma\Delta$Ms: Bandpass $\Sigma\Delta$ Modulators

- Other BP-$\Sigma\Delta$M architectures

![Diagram of bandpass $\Sigma\Delta$ modulators with transfer functions and poles/zeros](image)

- Bandpass decimation

![Diagram of bandpass decimation with digital BP filter and downsampler](image)

- Efficient decimation

![Diagram of efficient decimation with complex LP decimator](image)
CT-ΣΔMs: Basic Concepts

- Discrete-Time ΣΔMs
  - DT loop filter
  - All internal signals are DT
  - Sampling at the input

- Continuous-Time ΣΔMs
  - CT front (loop filter) part
  - DT back (quantizer) part
  - Sampling inside the loop

Pros of CT-ΣΔMs
- Implicit anti-aliasing filter
- Less impact of sampling errors
- No input switches – potentially better for low-voltage supply
- No “settling” error at the loop filter circuitry
- Potentially larger operation speed with less power consumption
- No sampling of the noise at the input capacitors
- Reduced digital noise coupling

Counters of CT-ΣΔMs
- Very involved dynamic due to the combination of non-linearity, CT and DT
- Larger impact of circuit non-linearities
- Time constant tuning is needed for correct loop filtering
- Large sensitive to time uncertainty ("jitter")
Linear analysis of CT-ΣΔMs, assuming [Bree01]:
- Linear model for the quantizer
- DAC gain is unity in the signal bandwidth

\[ Y(f) = \frac{H(f)}{1+H(f)} \cdot X(f) + \frac{1}{1+H(f)} \cdot E(f) \]

Example: Lth-order, B-bit single-loop architecture

\[ Y(f) = \frac{g_1}{g_1'} \cdot X(f) + (2\pi f r)^L \cdot E_q(f) \Rightarrow DR = \frac{3(2^B-1)^2(2L+1)L^{2L+1}}{2\pi^2L} \]

DT-to-CT synthesis method: pulse invariant transformation (freq. domain)
- Find an equivalent DT ΣΔM that fulfils the required specifications
- Based on a DT-to-CT equivalence [Cher00]

<table>
<thead>
<tr>
<th>DAC</th>
<th>H(z)</th>
<th>H(s)</th>
</tr>
</thead>
<tbody>
<tr>
<td>NRZ</td>
<td>( \frac{z^{-1} \cdot (1-z^{-1})}{1+z^{-2}} )</td>
<td></td>
</tr>
<tr>
<td>RZ</td>
<td>( \frac{1-z^{-2}}{2} \cdot z^{-1} - \left(\frac{1-z^{-2}}{2}\right) \cdot z^{-2} )</td>
<td></td>
</tr>
<tr>
<td></td>
<td>( \frac{\omega_o \cdot s}{s^2 + \omega_o^2} )</td>
<td></td>
</tr>
<tr>
<td>HRZ</td>
<td>( \frac{\sqrt{2}}{2} \cdot z^{-1} - \left(1 - \frac{\sqrt{2}}{2}\right) \cdot z^{-2} )</td>
<td></td>
</tr>
</tbody>
</table>

Open-loop configuration

\[ X_1(Z) = Z^{-L-1}[DAC(s)H(s)]_{\lfloor T - n T_s \rfloor} \]
Application of DT-to-CT method to cascade CT $\Sigma\Delta$Ms

- Every state variable and DAC output must be connected to the integrator input of the following stages in the cascade [Ortm01]
- Increases the number of analog components (transconductors and amplifiers)

Direct synthesis method [Bree01]

- Uses the desired NTF as a starting point, (as for the DT case)
- An Inverse Chebyshev distribution of the NTF zeros has advantages in terms of SNR and stability

Application to cascade architectures [Tort06]

- Optimum placement of poles/zeroes of the NTF
- Synthesis of both analog and digital part of the cascade CT $\Sigma\Delta$ Modulator
- Reduced number of analog components
Direct synthesis of cascade architectures (I) [Tort06]

- Sensitivity to mismatch (gm,C)
- A 2-1-1 example

Direct synthesis of cascade architectures (II) [Tort06]

\[
\hat{y}_d(z) = \sum_{k=1}^{m} y_k(z) CL_k(z)
\]

\[
y_k(z) = \frac{1}{1 - Z_{kk}} \sum_{i=1}^{k-1} Z_{ik} y_i(z)
\]

\[
CL_k(z) = \frac{-Z_{km}CL_m}{1-Z_{mm}}
\]

\[
Z_{km} = Z\left(L^{-1}(HDF_{km})|nT_s\right)
\]
A case study: A 12-bit@20MHz, 4-b, 2-1-1 CT ΣΔM for VDSL [Tort06]

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>$R_{in}$</td>
<td>1kΩ</td>
</tr>
<tr>
<td>$R_s$</td>
<td>2.5kΩ</td>
</tr>
<tr>
<td>$k_{f2}$</td>
<td>50µA/V</td>
</tr>
<tr>
<td>$k_{f1}$</td>
<td>500µA/V</td>
</tr>
<tr>
<td>$k_f$</td>
<td>120µA/V</td>
</tr>
<tr>
<td>$k_{n1}$</td>
<td>450µA/V</td>
</tr>
<tr>
<td>$C_4$</td>
<td>7.5pF</td>
</tr>
<tr>
<td>$C_2$</td>
<td>4.075pF</td>
</tr>
</tbody>
</table>

CT-ΣΔMs: Synthesis Methods

Direct synthesis method

General References


