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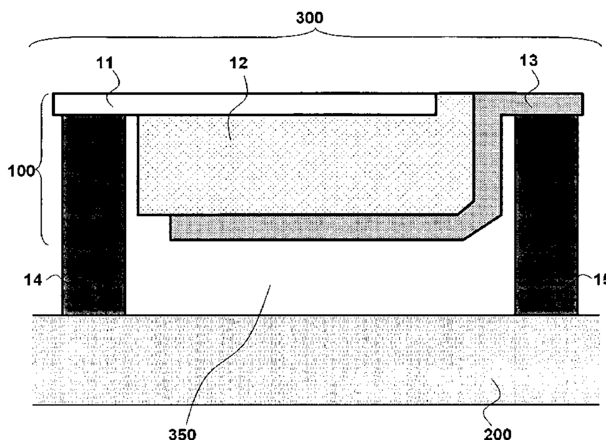

FIG. 1B

(57) Abstract: The invention relates to a method of performing heterogeneous integration of thin-film bulk acoustic wave resonator, FBAR, with complementary-metal-oxide-semiconductor integrated-circuit, CMOS, technologies. According to the invention, the method comprising the following steps, namely: i) forming a first device wafer including said FBAR, a sacrificial layer and substrate, with said FBAR devices defined on a first face; ii) forming a second device wafer including circuit elements fabricated on a CMOS technology, with CMOS integrated-circuits defined on a first face; iii) wafer-level-transferring and integration of the first device wafer including FBAR, a sacrificial layer and substrate, into the second device wafer including circuit elements fabricated on a CMOS substrate; iv) wafer-level-releasing of FBAR devices from their supporting substrate to provide mechanical isolation of FBAR devices. The invention further comprises a heterogeneous-technology semiconductor assembly, radio-frequency system and a sensing system.

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THIN-FILM BULK ACOUSTIC WAVE RESONATOR AND METHOD FOR PERFORMING HETEROGENEOUS INTEGRATION OF THE SAME WITH COMPLEMENTARY-METAL-OXIDE-SEMICONDUCTOR INTEGRATED CIRCUIT

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TECHNICAL FIELD OF THE INVENTION

The present invention relates to acoustic resonators and its fabrication, to integrated circuits and its fabrication; and more particularly to the combination of the
10 above techniques and methods for performing heterogeneous integration of thin-film bulk acoustic wave resonators (FBAR) with complementary-metal-oxide-semiconductor (CMOS) integrated circuit (IC).

15

BACKGROUND OF THE INVENTION

The integration and process compatibility of micro-electromechanical systems (MEMS) to CMOS-integrated circuit technologies is one of the most demanding areas at both technology and application levels. Several issues like manufacturing
20 temperature, packaging, and post-processing of MEMS; integrity of CMOS; and reliability and modeling of the MEMS-to-CMOS interface are just some examples that can be mentioned. The references presented in [1-3] describe some of the commented issues.

25 As a micro-machined resonant system, thin-film bulk acoustic wave resonators (FBAR) have also attracted the attention of RF integrated-circuit and sensor-application designers, being capable of achieving high performance in radio-frequency (RF) and sensor applications, as well. The first FBAR was presented by Lakin and Wang in 1981 [4] and, since then, RF filters and duplexers [5], mass and
30 chemical sensors [6-8], and other acoustic-based sensors have been investigated and manufactured.

In considering the popularity and good response of FBAR, recent interest and latest developments in FBAR-to-CMOS integration have stimulated the conception
35 of integrated applications in which FBAR is key component and whose IC integration

is a requirement to proper functionality of the system. Different integration strategies have been investigated, being hybrid and monolithic integration the most relevant. By means of hybrid integration, two systems located in separated substrates are typically integrated by wire-bonding of the involved devices. In the case of FBAR-to-CMOS integration, the FBAR terminals are the bonding points of the first system to be connected, while the corresponding circuit nets do for the second system, in this case the IC. Examples of this integration approach are the oscillators presented in [9-11], where the FBAR performs the crystal-like functionality in the system. Second approach for FBAR-to-CMOS is to monolithically integrate FBAR with CMOS circuitry. In the typical conception, FBAR is placed above the circuit, in order to save die area. This approach was disclosed in late 1993 [12], even a system integrating FBAR and radio circuitry was conceived in 2001 [13]. However, it was not as late as 2005 when the first monolithic FBAR-above-IC systems were demonstrated [14-16]. The interest for monolithic integration of FBAR has not limited to full-active ICs, but also for passive components like CMOS inductors [17]. Other MEMS, NEMS and SAW integrated resonators have been demonstrated, as well [18-20].

At the date, hybrid or monolithic approaches are main-stream integration strategies. Now, a third integration approach introduced by the present invention is wafer-level-transfer of FBAR into CMOS substrate or, vice versa, CMOS substrate may be transferred to FBAR substrate. For this purpose, this approach implements various techniques additional to standard CMOS and FBAR fabrication, including flip-chip, multi-chip-module, surface micromachining and packaging. Implemented in this invention, some of these techniques are utilized in a different way to the standard application. For example, packaging of MEMS or FBAR has traditionally been implemented as a protective means of device [21-24], where caps and protective structures are provided to enclose the device. Also, in [25], a method for packaging FBAR is presented, where a device chip having circuit elements and a cap is fabricated. To complete the process, the cap is placed on the device chip to connect a first contact point with a second contact point using the connector on the cap. On the other hand, a reduced substrate MEMS device and system for producing the same is disclosed in [26]. Here, a process in accordance with embodiments of the invention may include bonding a first packaging part to a MEMS device including a support substrate, removing the support substrate, and bonding a second packaging part to the MEMS device. Also related with reducing losses due

to substrate coupling, a method for fabricating a floating FBAR structure has been disclosed in [27]. In that work, the thin film resonator includes a supporting means, a first electrode, a dielectric layer, and a second electrode. The FBAR supporting layer has posts and a supporting layer formed on the posts, yet comprising a three
5 dimensional, floating construction. The supporting layer and posts are fabricated by means of surface micro-machining of a sacrificial layer. The overall structure is still supported on isolating substrate material such as silicon, glass or ceramic.

As it will be disclosed from the following description, in the present invention the
10 FBAR is a three-dimensional, floating structure. As a difference to conventional two-dimensional FBAR or the floating structure presented in [27], the whole FBAR structure of the present invention is completely transferred to a supporting substrate, with no presence of sacrificial layer in the target substrate. Hence, no etching of the FBAR supporting substrate is needed. In one embodiment of the present invention,
15 the FBAR is exclusively supported by two or more posts. This reduces the number of steps and time involved in the fabrication of the FBAR. At the same time, the supporting posts may be connecting points to a CMOS substrate, allowing for heterogeneous integration of FBAR-to-CMOS, being the FBAR placed above the integrated circuit. This means that die area may be reduced, compared to hybrid or
20 even to FBAR-on-side-of-IC monolithic integration. This implies that no specific technology development is needed in order to provide with technologic compatibility to both FBAR and CMOS fabrication processes.

According to the previous paragraph, the present invention describes a method
25 for performing heterogeneous integration of FBAR devices with integrated circuits fabricated according to standard CMOS technologies. In this sense, the fabrication technologies of both FBAR and CMOS devices are, in general, different. In this way, they are referred as heterogeneous technologies.

30 Another feature is that, as a difference to hybrid-integrated devices, integration is prioritized to dicing, i.e. the FBAR devices are integrated prior to chip dicing.

A third feature of the heterogeneous integration approach reported by the present invention is that the FBAR devices are transferred to the CMOS wafer, and at the
35 same time, said FBAR devices are released from their original supporting substrate

by means of surface micromachining of a sacrificial layer. This approach is different from the one disclosed by Wong *et al.* in [28], because they integrate a micro-electromechanical switch with an FBAR which already exhibits an air cavity, defined by an independent FBAR fabrication process. Also, the carrying substrates of both
5 the switch and the FBAR devices are still present after packaging and integration of them. In our approach, the air cavity is the result of the wafer-level-transfer process of the FBAR into a CMOS device wafer. On the other hand, the original carrying substrate of the FBAR devices is discarded after the wafer-level-transferring, because it is released when surface micromachining of a sacrificial layer present on
10 the FBAR wafer is performed. Said sacrificial layer is located between the FBAR devices and the substrate and occupies a volume which has no pattern. As a difference to conventional FBAR fabrication processes based on surface micromachining in which a sacrificial layer is deposited and patterned according to photolithography processes, the etching of the sacrificial layer described by the
15 present invention is performed on the whole surface of the wafer. Since no patterning of the sacrificial layer is performed on the FBAR wafer prior to the FBAR-to-CMOS integration, the whole volume of the material composing the sacrificial layer is etched once both the FBAR and the CMOS wafers are interconnected, thus releasing the FBAR devices and separating them from their original carrying
20 substrate (although they are now attached to the second CMOS substrate, once the assembly and wafer-level-transfer is completed).

Broadly, it is an object of the present invention to provide a thin-film bulk acoustic wave resonator (FBAR) heterogeneously integrated with CMOS integrated-circuit in
25 order to implement RF and sensor applications as well, and a method for manufacturing the thin-film resonator and the FBAR-to-CMOS integration.

It is another object of the present invention to provide a thin-film bulk acoustic wave resonator (FBAR) that may be fabricated by transferring of said FBAR on top
30 of a supporting substrate, and a method for manufacturing the thin-film resonator.

It is still another object of the present invention to provide a thin-film bulk acoustic wave resonator (FBAR) that may be fabricated by transferring of said FBAR on top of an on-substrate CMOS integrated circuit, and a method for manufacturing the
35 thin-film resonator and for design of the CMOS integrated-circuit.

It is still another object of the present invention to provide a thin-film bulk acoustic wave resonator (FBAR) having a three-dimensional, floating construction to minimize power loss due to acoustical and electric coupling to the substrate, and a method for manufacturing the thin-film resonator.

It is still another object of the present invention to reduce the fabrication time of a thin-film bulk acoustic wave resonator (FBAR) by transferring the same into a CMOS substrate with no need of etching of said substrate, and a method for manufacturing the thin-film resonator.

It is still another object of the present invention to provide fabrication compatibility for both thin-film bulk acoustic wave resonator (FBAR) and CMOS integrated circuit in order to integrate them into a compact RF or sensor application, and a method for achieving said compatibility.

It is still another object of the present invention to provide fabrication flexibility and versatility for the FBAR-to-CMOS interconnection technology, in order to integrate both thin-film bulk acoustic wave resonator (FBAR) and CMOS integrated circuit, and a method for achieving said flexibility and versatility.

It is a further object of the present invention to reduce die area for fabrication of FBAR-to-CMOS integrated RF and sensor applications as well, and a method for achieving said die area reduction.

These and other objects of the present invention will become apparent to those skilled in the art from the following detailed, description of the invention and the accompanying drawings.

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BRIEF DESCRIPTION OF THE INVENTION

A method for fabricating a thin-film bulk acoustic wave resonator (FBAR) and, at
5 the same time, performing heterogeneous integration of said FBAR with complementary-metal-oxide-semiconductor (CMOS) integrated circuit (IC). Integration of FBAR to CMOS-IC is performed with independence of FBAR or IC fabrication technologies. Wafer-level or chip-level integration is performed under decision of the designer, being possible to implement wafer-to-wafer, wafer-to-chip
10 or chip-to-chip transfer processes. In the preferred embodiment of this invention, wafer-level-transfer is carried-out, being said FBAR suspended above the IC substrate and connected to the IC by at least two electrical-connecting points. Said connecting points provide the FBAR-to-IC integration and may be implemented as soldering bumps, thru-hole or via-hole-fabricated supporting posts, or electro-plating
15 deposition. This invention is understood to not be limited to FBAR devices, and its principles may be applied to other suitable MEMS devices.

BRIEF DESCRIPTION OF THE DRAWINGS

20 **FIG. 1A** is top view showing the integrated FBAR-to-CMOS ensemble according to one preferred embodiment of this invention.

FIG. 1B is cross-sectional cutaway view of the device of **FIG.1A** cut along line A-A'.

25 **FIGS. 2A** to **2D** are cross-sectional cutaway views illustrating a method for manufacturing a thin-film bulk acoustic resonator according to one embodiment of this invention.

FIG. 3 is cross-sectional cutaway view showing a CMOS process according to one
30 embodiment of this invention.

FIGS. 4A to **4D** are cross-sectional cutaway view of the heterogeneous integration process of FBAR to CMOS substrate, according to one embodiment of this invention.

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DETAILED DESCRIPTION OF THE INVENTION

Although the present invention is not limited in this regard, the term "MEMS device" as used herein may be understood to include, inter alia, any suitable micro-electromechanical system device, for example, a thin-film bulk acoustic resonator (FBAR), an FBAR filter, and FBAR RF filter, a RF switch, a varactor, a tunable capacitor, or any other MEMS device where it may be relevant to apply the principles of the present invention. Although an exemplary embodiment of the present invention may include a single FBAR device, it is presented herein only as an example of applying the principles of the present invention to a MEMS device; the present invention is not limited in this regard, and its principles may be applied to other suitable MEMS devices.

Hereinafter, preferred embodiments of the present invention will be described in more detail with reference to the accompanying drawings, but it is understood that the present invention should not be limited to the following embodiments.

In one embodiment of the present invention, an FBAR is placed on and connected to a CMOS substrate, thus configuring a floating structure on the substrate. Also in one embodiment of the present invention, the CMOS substrate may carry integrated circuitry, although this is not strictly necessary, being enough a CMOS substrate carrying connecting interfaces to the FBAR. **FIG. 1A** and **FIG. 1B** are schematics illustrating top and cross-sectional views of the integrated FBAR-to-CMOS **300**, where FBAR **100** is placed on CMOS substrate **200**. In this way, the only supporting means, making the FBAR **100** a three-dimensional, floating structure, are the posts **14** and **15**. At the same time, posts **14** and **15** serve as connecting points, providing electrical contact between FBAR **100** and CMOS substrate **200**. It will be appreciated by persons skilled in the art that, in embodiments of the present invention, supporting substrate **200** may be a CMOS substrate carrying passive devices, dummy interconnections, test structures, integrated circuitry, or combinations of one or more of these. Also, it will be appreciated to those skilled in the art that the present invention is not limited to CMOS technologies, being possible to apply the present invention to other integrated circuit technologies. Thus, an exemplary embodiment of the present

invention includes CMOS technology as substrate **200** for providing support to FBAR **100**. On the other hand, it will become apparent to those skilled in the art that, since the floating configuration of FBAR **100** provides it with acoustical and mechanical isolation to substrate **200**, the same principles may be applied to other
5 micro-machined movable structures, for example, MEMS devices including FBAR filters, FBAR RF filters, RF switches, varactors, tunable capacitors, or any other suitable MEMS device. Referring to **FIG. 1A** and **FIG. 1B**, FBAR **100** is conformed by metal electrodes **11** and **13**, and acoustic material thin-film **12**. In **FIG. 1B** the air interface **350** between FBAR **100** and substrate **200** provides acoustical and
10 mechanical isolation between FBAR and substrate, in order to guarantee a high quality factor. This air interface is the result of one of the fabrication processes described following.

Referring to **FIGs. 2A** to **2D**, schematic description of the fabrication process of
15 FBAR **100** is given, according to one embodiment of the present invention. In **FIG. 2A** a sacrificial layer **110** is deposited on top of the silicon substrate **119**. Said sacrificial layer **110** will be released when FBAR **100** and substrate **200** are to be integrated. The next step of the fabrication process of FBAR **100** is illustrated in FIG. **2B**, where a metal electrode **111** is deposited on top of sacrificial layer **110**. In one
20 embodiment of the present invention, the material composing the metal electrode may be selected from the group of platinum, molybdenum, aluminum, gold, tungsten, tantalum, or any other having good electrical conductivity properties. At the same time, this material is to provide crystallographic compatibility with the piezoelectric material to be used for implementation of the acoustic thin-film layer
25 **112** in **FIG.2C** and **2D**. For the purpose of obtaining good crystallographic orientation and piezoelectric properties, acoustic material is deposited on top of the first metal electrode **111**, which is made of one of the materials yet mentioned, or others with similar properties. In one embodiment of the present invention, the thin-film acoustic layer is deposited by means of RF sputtering, with no prejudice of other
30 deposition or growing techniques, for example, epitaxial, or plasma-assisted deposition. In the same way, compatibility issues with CMOS technologies are not relevant to choose the thin-film acoustic layer, since FBAR **100** and substrate **200** are independent processes, being integrated just at the final step of the whole manufacturing process of the FBAR-to-CMOS integrated system. In one
35 embodiment of the present invention, the material composing the thin-film acoustic

layer may be selected from the group of aluminum nitride (AlN), zinc-oxide (ZnO), lead zirconate titanate (PZT), lead tantalum zirconate titanate (PLZT), or any other material exhibiting good piezoelectric properties. In **FIG. 2D**, it is illustrated the last step of the FBAR 100 fabrication process, before integration to CMOS substrate, 5 which is deposition of the second metal electrode **113**. In one embodiment of the present invention, the material composing the metal electrode may be selected from the group of platinum, molybdenum, aluminum, gold, tungsten, tantalum, or any other having good electrical conductivity properties. Metal electrode **113** is deposited on top of the thin-film acoustical layer **112**, and may be manufactured by 10 the same processes carried-out to fabricate the first electrode. In the preferred embodiment of the present invention, and as a difference to conventional FBAR devices, the FBAR **100** is provided with no air-interface or reflecting-mirror stack underneath the first metal electrode **111**. Since air interface **350** will be provided in successive steps of the integration process, no additional steps are required for the 15 FBAR **100** manufacturing process.

FIG. 3 illustrates schematic of the cross-sectional view of an exemplary integrated-circuit process **211** fabricated on carrying substrate **210**. In one embodiment of the present invention, the integrated-circuit process **211** may be, but 20 not restricted to, CMOS, being possible alternative implementations in bipolar, BiCMOS, SOI, or other integrated-circuit technologies. In the preferred embodiment of this invention the integrated-circuit process may include a protective layer **212** on top of the upper layers of the process. At its time, said protective layer **212** is provided with at least two opening windows **213** and **214** just above the top 25 electrical conducting layer, or above of any other electrical conducting layer provided by the integrated-circuit technology. The opening windows **213** and **214** will serve as landing pads **215** and **216** to FBAR-to-CMOS interconnection. According to the present invention, alternative configurations of the integrated-circuit process may not include protective layer or opening windows on the latter. In these cases, 30 additional post-processing steps will be required in the integrated-circuit, in order to provide opening windows and protective layer on top of the integrated-circuit layers. Among these steps it may be implemented, inter alia, protective layer deposition and photolithography. Additional steps conducting to provide protective layer and opening windows on top of the integrated-circuit process will become apparent to 35 those skilled in the art of integrated-circuit manufacturing.

Referring to **FIGs. 4A** to **4D**, schematic of the FBAR-to-CMOS heterogeneous integration process is illustrated for one embodiment of the present invention. In **FIG. 4A**, deposition and etching of an alloy or stack of metals suitable for soldering
5 or electro-platting is carried-out, thus defining landing pads **310** and **320**. This step is required if metal electrodes **111** and **113** of FBAR **100** are not made of materials suitable to adherence for soldering or electro-platting purposes. In one embodiment of the present invention, the materials composing the landing pads **310** and **320** may be selected from the group of nickel, gold, titanium, among others. **FIG.4B**
10 illustrates how connecting posts **330** and **340** are placed on top of landing pads **310** and **320**. Connecting posts **330** and **340** will provide support and electrical connection to FBAR **100**, giving to it the suspended configuration described in the preferred embodiment of the preferred invention. The techniques and methods required to implement posts **330** and **340** are diverse and include, inter alia, mask-
15 driven deposition of soldering paste, metal deposition, and electro-platting assisted deposition. **FIG. 4C** is schematic describing the interconnection between FBAR and CMOS substrates. First, vertical orientation of substrate **119** carrying FBAR **100** is swapped and aligned to integrated-circuit substrate **200**. This is done to provide alignment between connecting post **330** and opening window **213**, and between
20 connecting post **340** and opening window **214**. The swapping and alignment procedures may be implemented by manual or automatic means. It is to be noticed that the whole FBAR structure is swapped during this step, with respect to the vertical direction, being now the former top electrode **113** the one to be closest to the integrated circuit. At its time, the FBAR-carrying substrate **119** is now the most
25 top layer of the suspending structure. It is also to be noticed that, due to bigger size of connecting posts **330** and **340**, compared to thickness of FBAR **100**, an air interface is now provided between FBAR **100** and substrate **200**. Mechanical interconnection of connecting posts **330** and **340** to pads **215** and **216** depends on the integration process. For example, in one embodiment of the present invention,
30 connecting posts **330** and **340** are soldering bumps that are heated and soldered to integrated-circuit pads **215** and **216**, in one side, and to FBAR pads **310** and **320**, in the other side. In other embodiments of the present invention, soldering may be replaced by electro-platting or deposition techniques, in order to achieve the interconnection described in **FIG. 4C**. Referring to **FIG. 4D**, final release of FBAR is
35 performed by wet etching of sacrificial layer **110**, thus achieving complete integration

between the FBAR **100** and the substrate **200**. Since sacrificial layer **110** isolates FBAR **100** of substrate **119**, the latter is also released when complete etching is achieved, separating both FBAR **100** and substrate **119**. At this point substrate **119** is of no interest and is discarded for manufacturing purposes. In one embodiment of
5 the present invention, wet etching is performed by means of fluorhydric acid (HF). At its time, FBAR **100** is fully released and connected to substrate **200**, which may be an only supporting substrate, or may carry passive or active devices, or both. In the preferred embodiment of the present invention, the substrate carries integrated-circuit devices, thus providing fully-integrated FBAR-to-CMOS application system
10 **300**. It is to be noticed that after the releasing process of sacrificial layer **110**, FBAR **100** exhibits two air interfaces, **350** and **360**, respectively. Hence, FBAR **100** has mechanical freedom to vibrate since no acoustical coupling exists between it and any substrate. This fact is necessary condition to guarantee good quality factors.

15 Various modifications to the present invention will become apparent to those skilled in the art from the foregoing description and accompanying drawings.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENT

Referring to **FIG. 2A to 2D**, FBAR configuration may be as follows: a 1μm-thick phosphor silicate glass (PSG) layer **110** is deposited on a 550μm-thick silicon wafer. Next, an 180nm-thick Cr/Pt layer –30nm of Cr for Pt-adhering purposes– is deposited on top of PSG and the first electrode **111** defined by lift-off. Afterwards, the acoustic layer **112** is composed of a 1μm-thick aluminum nitride (AlN) layer, being the resonator's shape defined by wet-etching. Finally, the second electrode **113** is made according to the same configuration of first electrode **111**.

Referring to **FIG. 3**, CMOS substrate **200** may be fabricated according to the typical structure of a CMOS technology, i.e. a top metal layer **217** for interconnecting covered by a dielectric protective layer **212**. This layer may be, for example, a 500nm-thick PECVD silicon oxide layer, with photolithography-defined openings **215** and **216** for pad connection. Metal layer **217** may be manufactured by implementing one or more of the following configurations: platinum over chromium, aluminum over chromium, aluminum over titanium, among others. Possible metal configurations are mainly determined by the etchant solution implemented for subsequent FBAR-to-CMOS integration.

Referring to **FIG. 4A** to **4D**, FBAR-to-CMOS integration may be performed as follows: first, landing pads **310** and **320** may be selected from the group of nickel (Ni), gold (Au), titanium (Ti), or combination of two or all of them. For example, thicknesses for Ni, Au and Ti may be 30nm, 20nm and 50nm, respectively. If the top metal of CMOS technology is not provided with adhesive metals for interconnection to soldering bumps, similar procedure should also be practiced on top metal **217** of CMOS substrate to guarantee proper adherence of soldering bumps. Next step is to place contacting posts **330** and **340** on top of landing pads **310** and **320**. These posts may be soldering bumps, made of an alloy of nickel and lead (Pb). In this case, soldering paste is applied to wafer by means of masking-aided appliance and alignment system. Once deposited the paste, manual or automatic pick-and-place system may be used to position, align and soft contact FBAR and CMOS wafers in proper location. Once both wafers are positioned in such a way that soldering paste contacts both FBAR and corresponding CMOS pads, the ensemble is introduced in

oven or heating machine, in order the soldering paste to be liquefied and subsequently cooled for soldering of landing pads, allowing for hard interconnection between both FBAR and CMOS substrates. Finally, PSG layer **110** is attacked by means of HF-etching, releasing silicon substrate layer **119**. At this point, FBAR
5 exhibits full acoustic isolation by means of two air interfaces up and down of electrodes and, at the same time, full interconnection with the CMOS substrate.

CLAIMS

1. Method of performing heterogeneous integration of thin-film bulk acoustic wave resonator (FBAR) with complementary-metal-oxide-semiconductor integrated-circuit (CMOS) technologies, the method comprising:

forming a first device wafer including said FBAR, a sacrificial layer and substrate, with said FBAR devices defined on a first face;

forming a second device wafer including circuit elements fabricated on a CMOS technology, with said CMOS integrated-circuits defined on a first face;

wafer-level-transferring and integration of the first device wafer including said FBAR, a sacrificial layer and substrate, into the second device wafer including circuit elements fabricated on a CMOS substrate;

wafer-level-releasing of said FBAR devices from their supporting substrate to provide mechanical isolation of said FBAR devices

2. Method of performing heterogeneous integration of thin-film bulk acoustic wave resonator (FBAR) with complementary-metal-oxide-semiconductor integrated-circuit (CMOS) technologies according to claim 1, wherein the first device wafer and the second device wafer are fabricated, in general, according to heterogeneous integrated-circuit technologies.

3. Method of performing heterogeneous integration of thin-film bulk acoustic wave resonator (FBAR) with complementary-metal-oxide-semiconductor integrated-circuit (CMOS) technologies according to claim 1, wherein said sacrificial layer is located all over the top surface of the substrate of the first device wafer, said sacrificial layer being distributed along the whole surface of the wafer and not limited to specific regions as it is performed in photolithography-processed, mask-based sacrificial layers.

4. Method of performing heterogeneous integration of thin-film bulk acoustic wave resonator (FBAR) with complementary-metal-oxide-semiconductor integrated-circuit (CMOS) technologies according to claim 1, wherein the wafer-level-transferring of said FBAR devices located on the first device wafer into the second device wafer is performed, among other processes, by means of surface micromachining of the sacrificial layer included on the first device wafer.

5. Method of performing heterogeneous integration of thin-film bulk acoustic wave resonator (FBAR) with complementary-metal-oxide-semiconductor integrated-circuit (CMOS) technologies according to claim 1, wherein no patterning of said sacrificial layer is performed prior to wafer-level-transferring of said FBAR devices into the second device wafer.

6. Method of performing heterogeneous integration of thin-film bulk acoustic wave resonator (FBAR) with complementary-metal-oxide-semiconductor integrated-circuit (CMOS) technologies according to claim 1 and claim 3, wherein the complete volume of the substrate of the first device wafer is released after etching of said sacrificial layer.

7. Method of performing heterogeneous integration of thin-film bulk acoustic wave resonator (FBAR) with complementary-metal-oxide-semiconductor integrated-circuit (CMOS) technologies according to claim 1 wherein said etching of said sacrificial layer of said first device chip including said FBAR provides full acoustic and mechanical releasing of said FBAR, being said FBAR located on top of said second device chip including circuit elements.

8. Method of performing heterogeneous integration of thin-film bulk acoustic wave resonator (FBAR) with complementary-metal-oxide-semiconductor integrated-circuit (CMOS) technologies according to claim 1 wherein said etching of said sacrificial layer of said first device chip including said FBAR provides full integration and interconnection of said FBAR with said second device chip including circuit elements.

9. Method of performing heterogeneous integration of thin-film bulk acoustic wave resonator (FBAR) with complementary-metal-oxide-semiconductor integrated-circuit (CMOS) technologies according to claim 1, wherein said method may be implemented at the chip-level or at the wafer-level, as well.

10. Heterogeneous-technology semiconductor assembly comprising:

thin-film bulk acoustic wave resonator (FBAR) devices;

a second device wafer including circuit elements fabricated on a CMOS technology, with said CMOS integrated-circuits defined on a first face;

said FBAR devices being wafer-level-transferred into the second device wafer in first face-to-first face alignment according to flip-chip, multi-chip-module and surface micromachining technologies and processes.

11. Heterogeneous-technology semiconductor assembly according to claim 10, wherein said FBAR devices are located above said second device wafer including circuit elements fabricated on a CMOS technology.

12. Heterogeneous-technology semiconductor assembly according to claim 10, wherein a first air cavity is formed in between the top surface of said second device wafer and said FBAR devices.

13. Heterogeneous-technology semiconductor assembly according to claim 10, wherein a second air interface is formed above the top surface said FBAR devices.

14. Heterogeneous-technology semiconductor assembly according to claim 10, wherein the assembly including a conductive contact between said second device wafer and said FBAR devices to make contact electrically with said FBAR.

15. Radio-frequency (RF) system or device according to claim 10, comprising ensemble of one or more thin-film bulk acoustic wave resonator (FBAR) and integrated-circuit in which at least one of the resonators is connected to the integrated-circuit in order to provide radio-frequency functionality such as band selection filter, pre-selection filter, band-rejection filter, duplexer, oscillator, mixer, tuned low-noise amplifier, power-amplifier, or similar RF system in which said FBAR is fundamental technology to provide the system with proper functionality.

16. Sensing system or device according to claim 10, comprising ensemble of one or more thin-film bulk acoustic wave resonator (FBAR) and integrated-circuit in which at least one of the resonators is connected to the integrated-circuit in order to provide read-out or processing functionality to said sensing system such as pull-in amplifier, read-out amplifier, zero-crossing detector, or similar sensing system in which said FBAR is fundamental technology to provide the system with proper functionality.

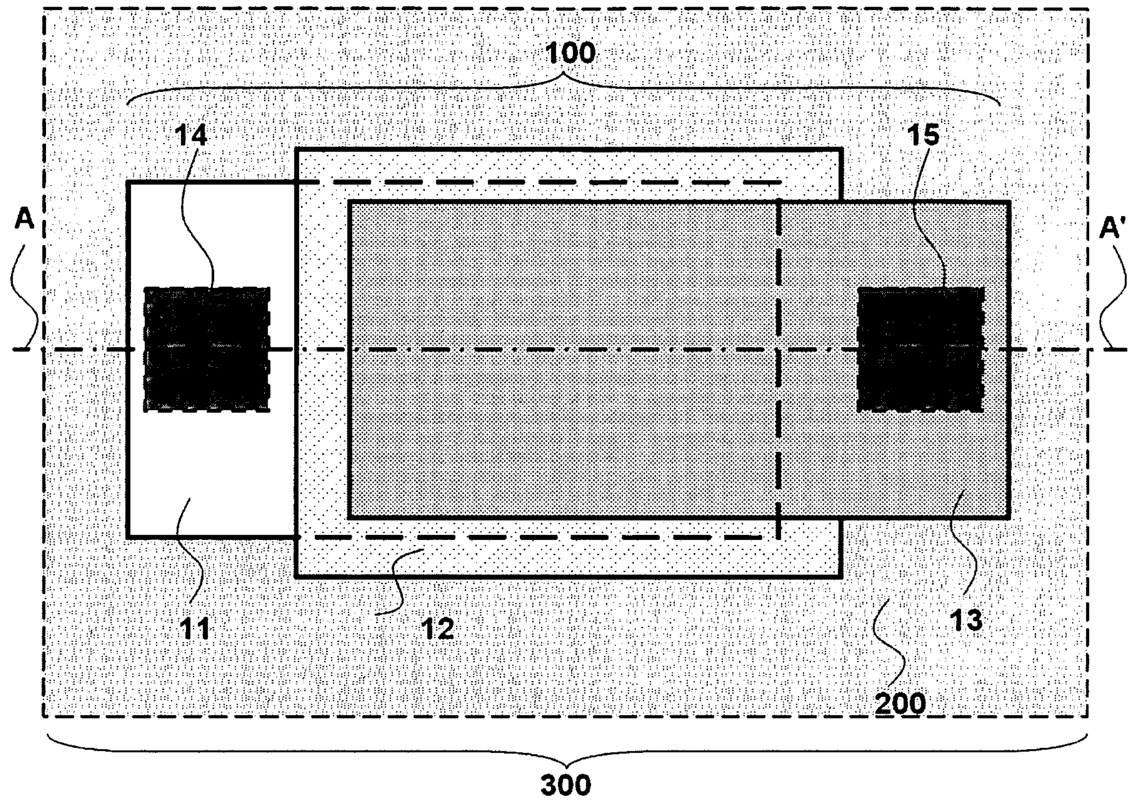

FIG. 1A

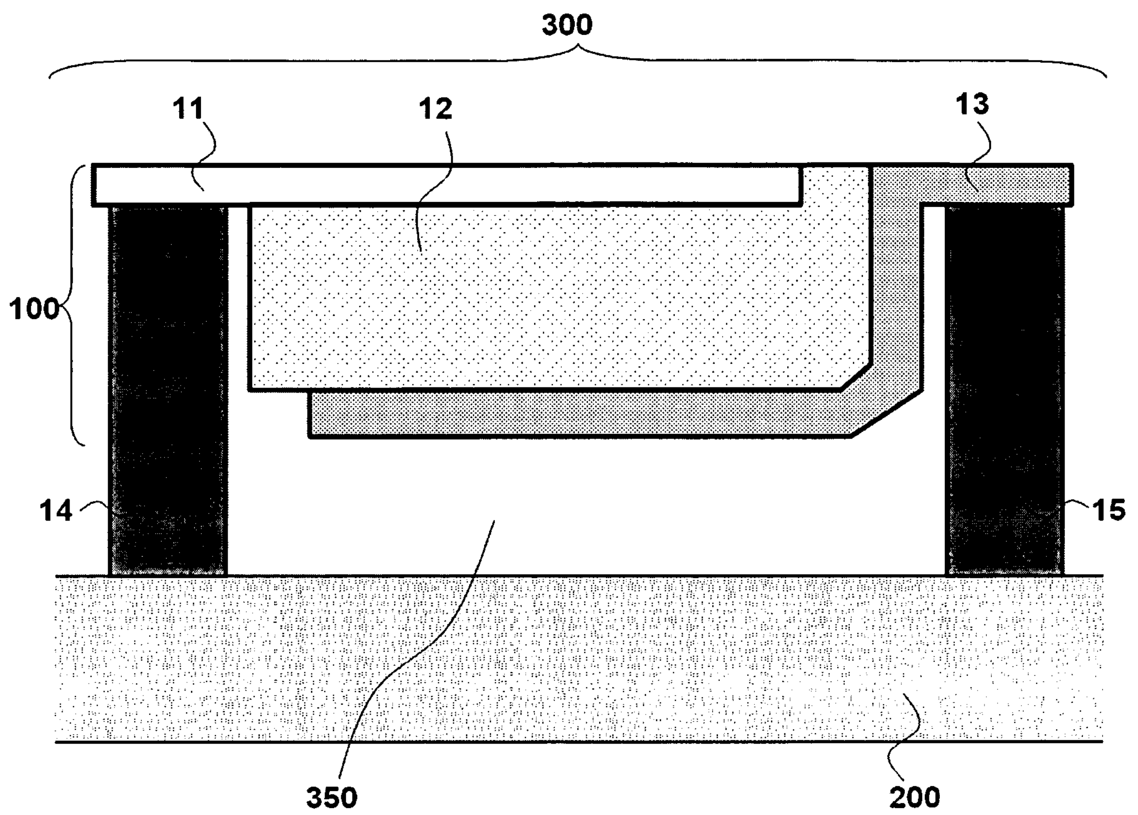

FIG. 1B

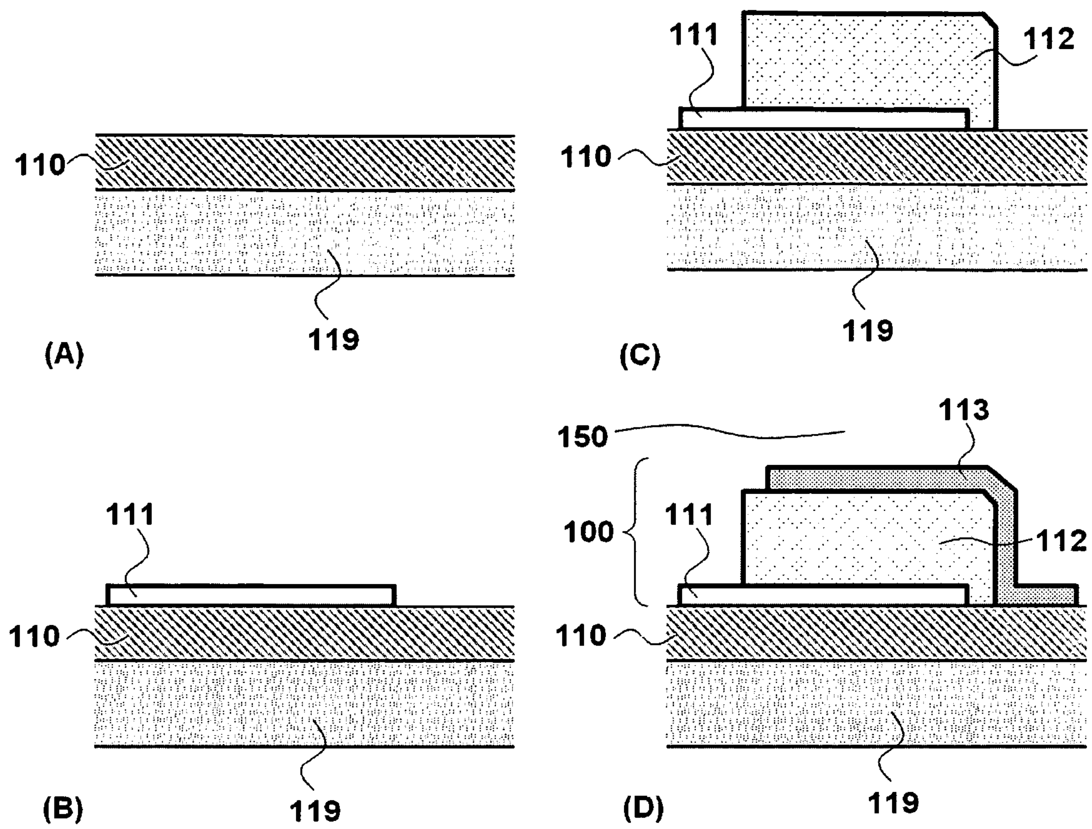

FIG. 2A to 2D

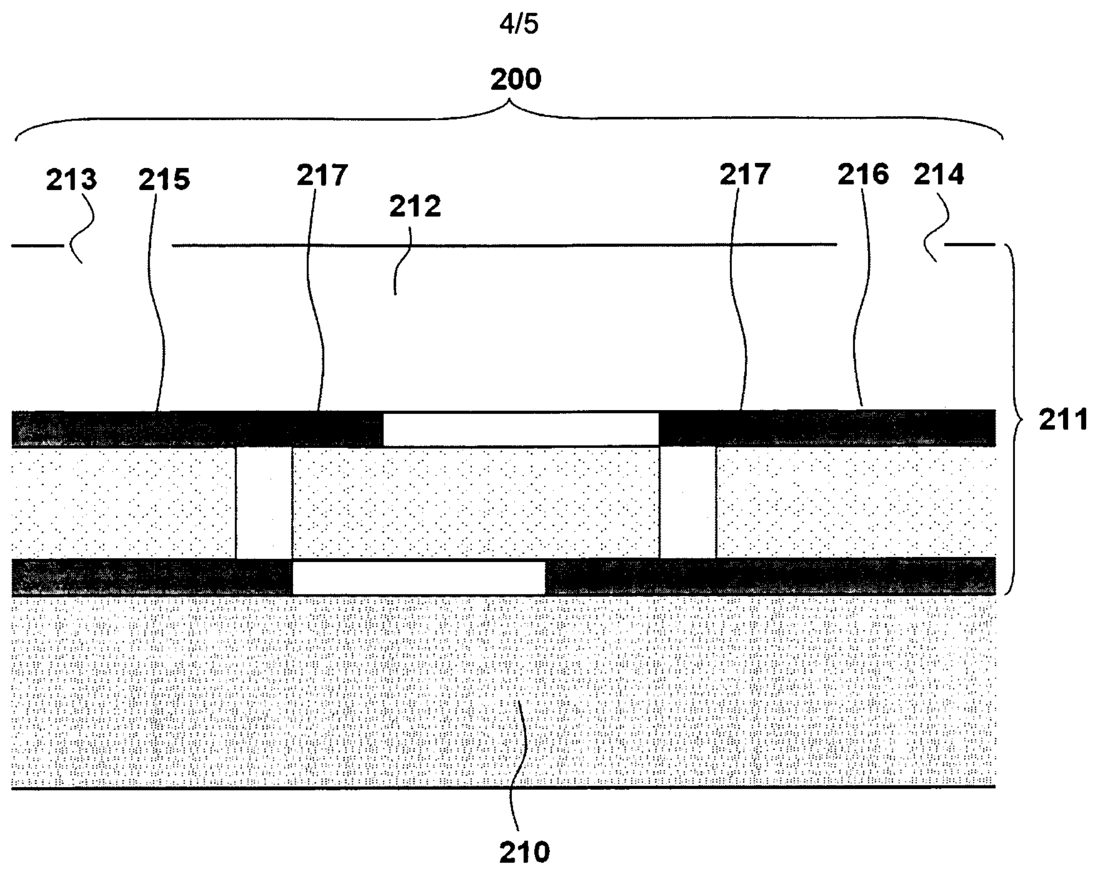

FIG. 3

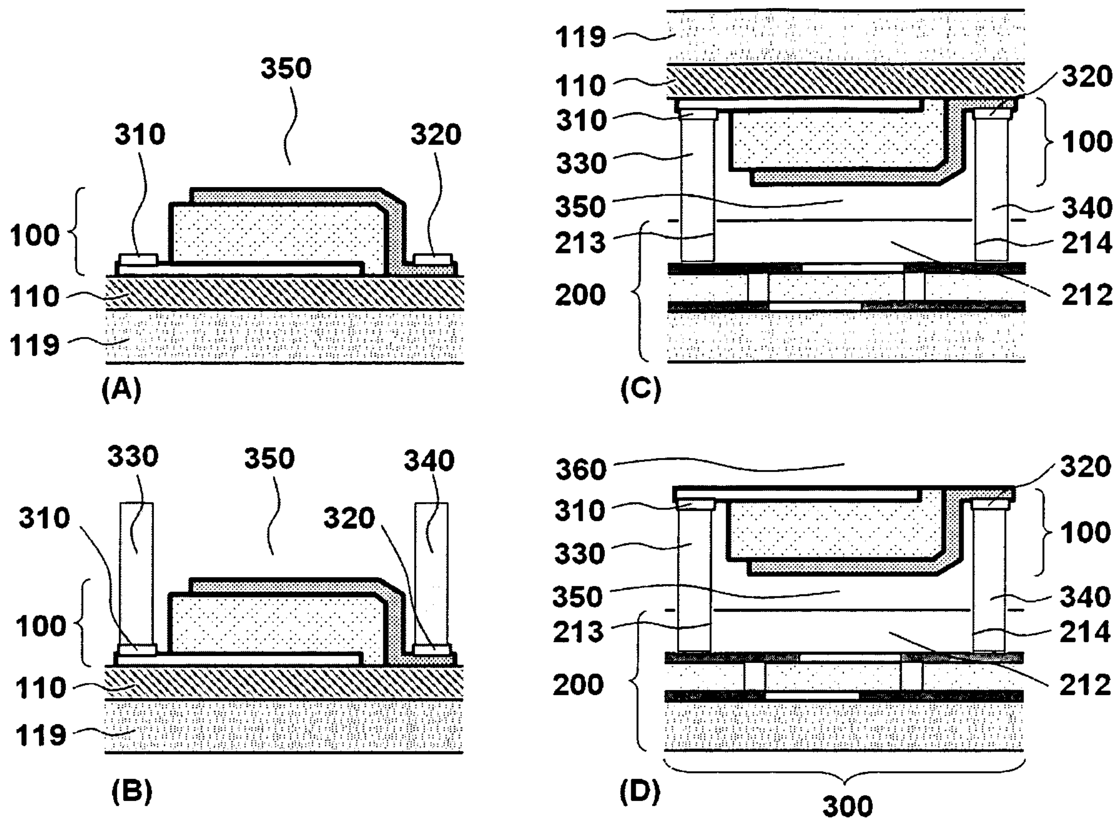

FIG. 4A to 4D

INTERNATIONAL SEARCH REPORT

International application No
PCT/EP2008/001226

A. CLASSIFICATION OF SUBJECT MATTER
INV. H03H9/17 H03H9/05

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
H03H

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practical, search terms used)

EPO-Internal, WPI Data, INSPEC, COMPENDEX

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	US 2006/125084 A1 (FAZZIO RONALD S [US] ET AL) 15 June 2006 (2006-06-15) the whole document	1-16
A	US 2006/128058 A1 (DUNGAN THOMAS E [US] ET AL) 15 June 2006 (2006-06-15) the whole document	1-16
A	US 2004/032012 A1 (WONG DANIEL M [US] ET AL) 19 February 2004 (2004-02-19) paragraph [0013] - paragraph [0016]; figure 3	1-16

☐ Further documents are listed in the continuation of Box C.

☒ See patent family annex.

* Special categories of cited documents :

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"O" document referring to an oral disclosure, use, exhibition or other means

"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

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"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art.

"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
23 July 2008	01/08/2008

Name and mailing address of the ISA/	Authorized officer
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INTERNATIONAL SEARCH REPORT

Information on patent family members

International application No
PCT/EP2008/001226

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