A Smart Noise- and RTN-Removal Method for Parameter Extraction of CMOS Aging Compact Models

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***Abstract*—In modern nanometer-scale CMOS technologies, time-zero and time-dependent variability (TDV) effects, the latter coming from aging mechanisms like Bias Temperature Instability (BTI), Hot Carrier Injection (HCI) or Random Telegraph Noise (RTN), have re-emerged as a serious threat affecting the performance of analog and digital integrated circuits. Variability induced by the aging phenomena can lead circuits to a progressive malfunction or failure. In order to understand the effects of the mentioned variability sources, a precise and sound statistical characterization and modeling of these effects should be done. Typically, transistor TDV characterization entails long, and typically prohibitive, testing times, as well as huge amounts of data, which are complex to post-process. In order to face these limitations, this work presents a new method to statistically characterize the emission times and threshold voltage shifts (ΔV_{th}) related to oxide defects in nanometer CMOS transistors during aging tests. At the same time, the aging testing methodology significantly reduces testing times by parallelizing the stress. The method identifies the V_{th} drops associated to oxide trap emissions during BTI and HCI aging recovery traces while removing RTN and background noise contributions, to avoid artifacts during data analysis.**

Keywords—CMOS; BTI; HCI; parameters; extraction; method; RTN; defects; aging;

I. INTRODUCTION

With nowadays CMOS technology downscaling, BTI [1][2] and HCI [3][4] aging effects, as well as RTN [5][6] transient effects, have re-emerged as important time-dependent variability (TDV) phenomena that must be taken into account in the design of digital and analog integrated circuits (ICs). During circuit operation, the variability effects related to the trapping/detrapping in/from oxide defects could result in circuit malfunction due to the shift of key transistor parameters, such as the threshold voltage (V_{th}) [7]. Thus, it is critical for IC designers to take into account TDV effects to implement reliability-aware circuits [8]. To this end, appropriate TDV compact models, like the Probabilistic Defect Occupancy (PDO) model [3], are essential. These models need to account for and clearly distinguish the 'slow' defects, responsible for aging-induced degradation, from the 'fast' defects causing the RTN transient variations. As shown in this paper, isolating the impact of the different types of defects within the experimental data is not straightforward.

Another important aspect is that an accurate extraction method of the defect parameters requires a sound statistical characterization of the transistor response to accelerated stress conditions [9]. Conventional BTI/HCI aging characterization techniques are based on the application of serialized stress-measurement (SM) sequences to one or more transistors simultaneously by using probe stations. The SM characterization technique consists of a stress phase, which accelerates the device degradation through the application of overvoltage to the device terminals, and a measurement phase, where the effects of the induced aging can be measured in reasonable testing times [10]. However, to get sufficient statistical data, a 'massive' aging test, with hundreds of transistors subjected to the same stress and measurement pattern, must be performed. Doing so serially (one device at a time) may, however, take several months. In our work, we use our previously designed 65-nm array-based IC ENDURANCE chip [11] in combination with a custom-designed characterization setup [12] that allows to execute BTI/HCI aging tests over hundreds of CMOS transistors with a stress parallelization technique that significantly reduces the total aging test time.

The impact of aging can be modeled through the analysis of the emission time (τ_e) and the corresponding impact on the variation of the threshold voltage (η) of each defect in the transistor. This analysis is carried out during the measurement phases, after the application of an overvoltage stress, where a 'recovery' (back to the fresh, un-stressed value) of the device threshold voltage V_{th} can be observed [13]. Fig. 1 shows experimental recovery traces attained after the execution of a massive BTI test, where charge detrapping from oxide defects [1] can be clearly seen during recovery as positive abrupt current jumps (i.e., V_{th} drops). Fig. 2 provides a zoom-in of some of the traces in Fig. 1. Note here that the simultaneous presence of RTN in the traces could mask or significantly increase the current increments, so it is critical to distinguish between those current levels that are linked to fast transients and slow defect discharges.

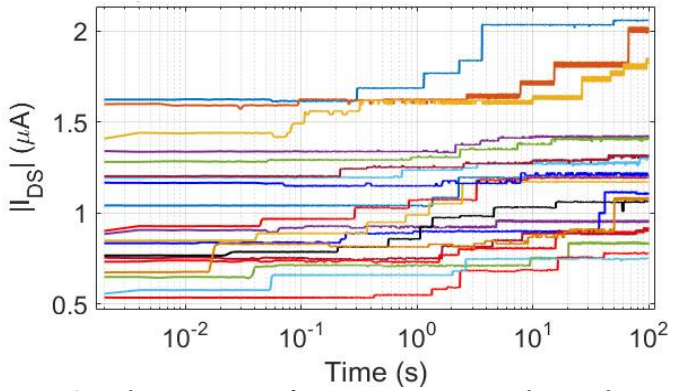

Fig. 1. Several recovery traces from a massive BTI test showing discrete current increments.

In this work, we introduce a novel and smart method of defect parameters extraction that identifies the defect-related τ_e and η values from a large number of experimental transistor recovery traces, where fast defect capture/emissions (i.e., RTN) and background noise are present. To model the effect of aging without noise-masking issues, the defect parameters extraction method removes the RTN and background noise from the measured BTI/HCI recovery traces and evaluates the $\{\tau_e, \eta\}$ tuple of each slow defect discharge found.

II. Description of the Method

The extraction method of the defect parameters follows the flow diagram shown in Fig. 3. For each device involved in the aging test, the method treats each recovery trace individually. First, it converts the I_{DS} vs. time traces measured after the stress period into the equivalent ΔV_{th} vs. time trace (the difference between the instantaneous threshold voltage and the fresh threshold voltage). By using the Weighted Time Lag Plot (WTLP) method [5][6], all ΔV_{th} levels of the trace are obtained. In order to remove the background noise from the recovery traces, each experimental ΔV_{th} sample is assigned to one of the ΔV_{th} levels previously found with the WTLP method, quantizing the trace and removing the background noise. Then, all RTN fast defect transitions (if any) are removed from the trace through the analysis of each transition between the i-th and the (i+1)-th recovery sample. The last step consists in the extraction of τ_e and η parameters associated to each of the identified defect discharges. This 5-step procedure is described in detail in the following.

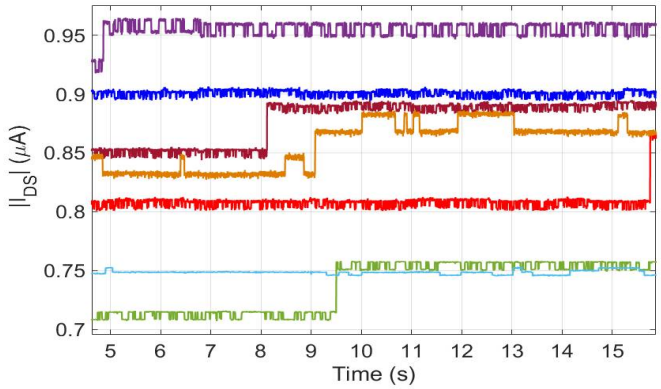

Fig. 2. Zoom-in of some traces in Fig. 1 showing fast defect transitions (RTN) mixed with slow defect discharges that result in I_{DS} abrupt jumps.

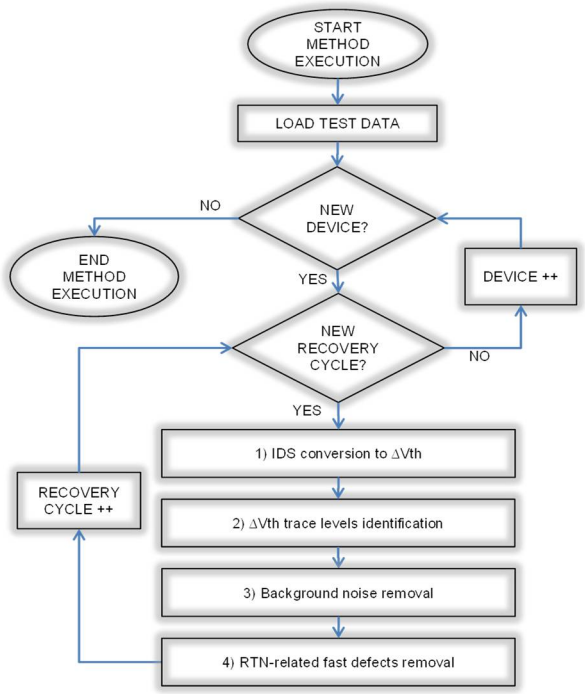

Fig. 3. Diagram flow for the extraction method of $\{\tau e, \eta\}$.

1) **I_{DS} conversion to ΔV_{th}.** For each tested device, the I_{DS} recovery traces measured as a function of time during the aging test is converted into the equivalent ΔV_{th} vs. time trace by means of the pre-stress I_{DS}-V_{GS} curve, i.e., the I_{DS}-V_{GS} curve of the fresh device [14]. For instance, Fig. 4 shows the results of the conversion from a measured I_{DS} trace, like the ones represented in Fig. 1, to its equivalent ΔV_{th} waveform, where 3 charge emissions (denoted with green arrows) can be clearly located during the measurement time window of 100s. Moreover, as can be observed in the recovery trace, fast transitions associated to RTN are present during the entire characterization experiment. The inset of Fig. 4 exposes one of those fast defect transitions between two separated ΔV_{th} levels

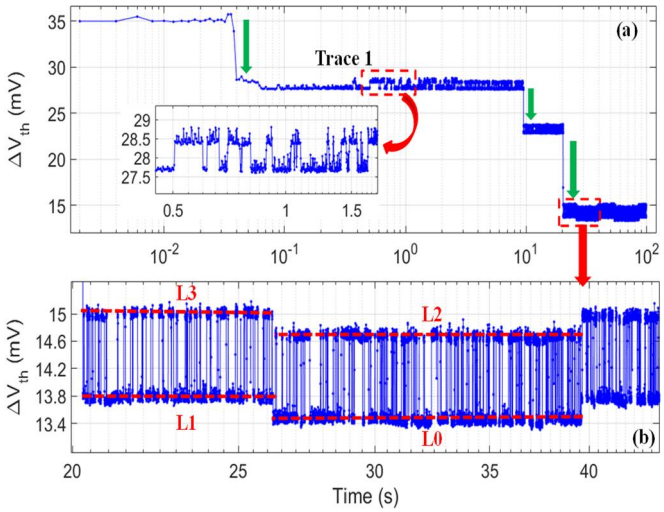

Fig. 4. (a) Example of a ΔV_{th} trace constructed from the measured I_{DS} recovery data, showing three clear slow defect discharges labeled with green arrows. (b) Zoom-in of (a) showing the combination of two fast defects and background noise on top of a ΔV_{th} level.

superimposed to a temporaly constant ΔV_{th} level. Fig. 4 (b) reveals fast capture/emission transitions, switching between 4 different ΔV_{th} levels (i.e., L0 to L3) and mixed with background noise. A visual inspection of Fig. 4 (b) reveals the joint contribution of two individual RTN signals, one switching between ΔV_{th} levels L0-L1 and the other one switching with lower capture/emission times between L1-L3 and between L0-L2.

2) **Identification of ΔV_{th} trace levels.** The next step consists in the application of the WTLP method [5][15] to each recovery trace to identify the number and magnitude of the ΔV_{th} levels present in the trace. The basic principle of the WTLP technique is the Time Lag-Plot (TLP) method [16], in which the i-th data sample of an experimental signal is represented versus the (i+1)-th data sample as shown in Fig. 5 (a). The plot diagonal shows populated data regions corresponding to different data levels (i.e., I_{DS} or ΔV_{th}) while transitions between different levels and background noise are located outside the diagonal.

The TLP methodology can be used as long as the background noise level is low enough, so that the ΔV_{th} levels and/or transitions can be clearly distinguished. However, if the background noise is so relevant that masks the capture/emission transitions, the resulting TLP of the ΔV_{th} levels are overlapped with the background noise making impossible to accurately locate them. Thus, the improved WTLP [5] is used instead of the TLP to clearly separate the background noise present in the recovery traces from the capture/emission defect transitions. The WTLP represents the probability that a $(\Delta V_{th\text{-}i} - \Delta V_{th\text{-}(i+1)})$ data sample in a recovery trace corresponds to one of the levels present in the trace. This probability is calculated by the normal bivariate distribution function (1.1) for each data sample. The weigthed time lag function defined in equation (1.2) reveals the contribution of all samples in the recovery trace, weighted by its distance to the analyzed $\Delta V_{th\text{-}i}$ data sample:

$$\varphi_i(x,y) = \frac{1}{2\pi\alpha^2}\exp\left(\frac{-\left[(I_i - x)\right] + \left[(I_{i+1} - y)^2\right]}{2\alpha^2}\right) \quad (1.1)$$

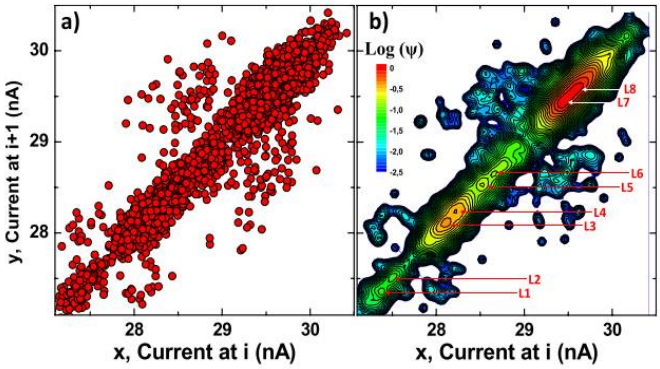

Fig. 5. Representation of a conventional TLP in an arbitrary example (a) and the corresponding WTLP in (b) [5].

$$\Psi(x,y) = K\sum_{i=1}^{N-1}\Phi_i \quad (1.2)$$

As shown in (b), where the function Ψ has been plotted against all data samples of the TLP (a), the Ψ function gets higher values in the most populated regions of the TLP. Moreover, those populated regions are located across the main diagonal of the WTLP where each local maximum corresponds to an individual current level present in the recovery trace.

For instance, Fig. 6 (a) shows the WTLP resulting from the analysis of trace 1 in Fig. 4 (a). In this case, the corresponding ΔV_{th} variations have been calculated from the comparison between the fresh I_{DS}-V_{GS} and the I_{DS} current measured after the BTI stress, as explained in step 1. By analyzing the diagonal of the WTLP, four groups of populated data regions, separated in the figure by green dashed arrows, can be distinguished. Each one of the data groups corresponds to a different ΔV_{th} level present in the recovery trace. Transitions from one data group to the next one are considered as slow defect emissions at a specific τ_e and the difference between two ΔV_{th} levels corresponds to the η of the discharged defect.

Furthermore, when present, fast capture/emissions on top of each ΔV_{th} level can also be clearly distinguished, as red-colored regions in the diagonal (i.e., in the ΔV_{th} levels L0 to L9) from other less populated regions located perpendicularly to the diagonal (i.e., ΔV_{th} level transitions). Moreover, the ten red

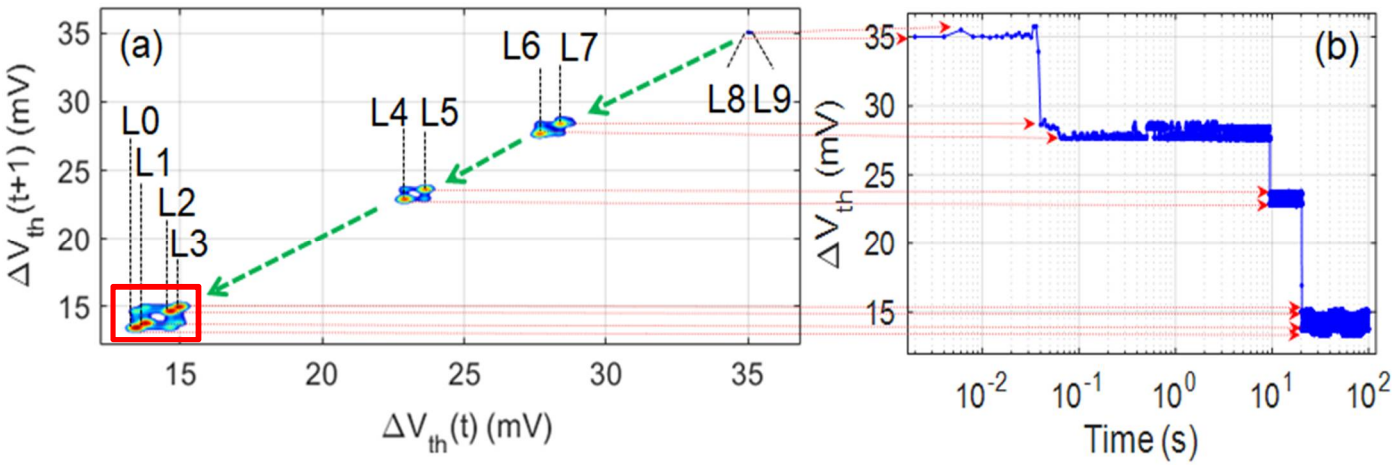

Fig. 6. (a) WTLP resulting from the analysis of Trace #1 in Fig. 4(a). (b) Corresponding ΔV_{th} level in the recovery trace for each red-colored zone in the WTLP in (a).

populated regions in the WTLP in Fig. 6 (a), i.e., from LO to L9, can be associated with each ΔV_{th} level present in the recovery trace in Fig. 6 (b) (pointed out with red arrows).

In order to clearly see the ΔV_{th} values associated to the RTN transitions detected in Fig. 4 (b), a zoom-in of the WTLP (red square in Fig. 6 (a)) is plotted in Fig. 7. The zoom clearly shows the 4 red regions across the diagonal, which correspond to the four different ΔV_{th} levels (i.e., L0, L1, L2 and L3). The blue regions out of the diagonal in the WTLP indicate the transitions between levels (e.g., L1 → L3). For instance, at t~25s, the signal switches between levels L1 and L3 and later, at t~30s, the signal switches between L0 and L2. These levels result from the joint combination of the two individual RTN signals shown in Fig. 4 (b) and coming from the fast charges/discharges of two oxide defects. The results in Fig. 7 clearly demonstrate that the application of the WTLP to the ΔV_{th} recovery trace allows an accurate location of all ΔV_{th} levels while distinguishing between RTN and BTI contributions.

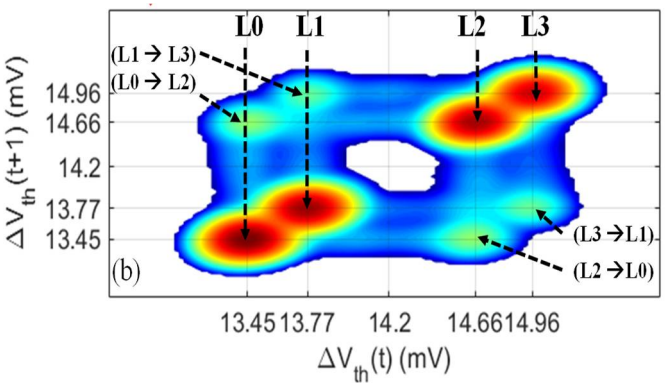

Fig. 7. Zoom-in of the WTLP in Fig. 6(a) showing, for the two RTN signals in Fig. 4(b), the ΔVth levels in the diagonal of the WTLP and the corresponding transitions between ΔVth levels outside the diagonal.

3) **Background noise removal.** Once the ΔV_{th} levels have been identified with the WTLP method, the procedure assigns the closest ΔV_{th} level to each sample in the ΔV_{th} trace. This step quantizes the ΔV_{th} recovery trace, removing the background noise and keeping only ΔV_{th} levels associated to captures/emissions of RTN and BTI contributions. For instance, Fig. 8 (a)-(c) displays three ΔV_{th} traces (in blue), showing high ΔV_{th} degradation due to the previous stress, and also the ΔV_{th} trace reconstruction (in red) with the background noise removed. During the recovery period (in this example, from 2ms to 100s), different ΔV_{th} levels can be observed because of defect emissions mixed with RTN phenomena, as shown in detail in the zoom-in plots in Fig. 8 (b) and (c).

4) **Removal of RTN-related transients.** In order to distinguish between RTN and BTI contributions, the Transition Matrix (TM), a square matrix that stores the transitions between different ΔV_{th} levels in the recovery trace, is defined. The dimention of the TM is the total number of ΔV_{th} levels found (ten in the example used in this Section), and each ΔV_{th} level is denoted as L*N* where *N* accounts for the number of levels (e.g., *N* goes from 0 to 9 in the example). The rows of the TM are defined as the initial ΔV_{th} levels (i.e., i-th ΔV_{th} level) while the columns are defined as the final ones

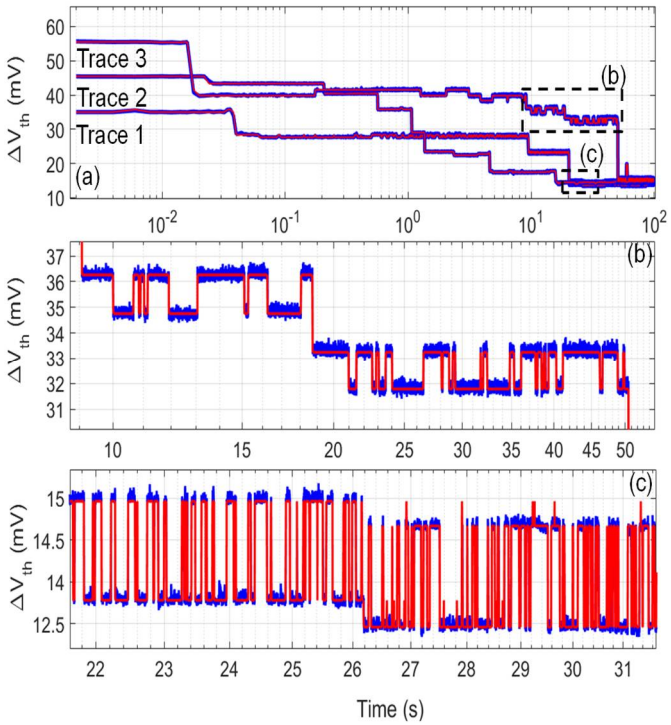

Fig. 8. (a) Recovery traces (blue) with the reconstructed trace without noise (red). (b), (c) Zoom-in of the traces showing RTN (in blue) and the trace reconstruction without background noise (in red).

(i.e., (i+1)-th ΔV_{th} level). During the ΔV_{th} trace analysis, three different ΔV_{th} level transitions can be distinguished:

- Case (i): No change of the ΔV_{th} level. The ΔV_{th} level of the i-th data sample equals the (i+1)-th ΔVth level. For instance, two consecutive ΔV_{th} samples staying at level L1.
- Case (ii): Defect charging. The (i+1)-th ΔV_{th} level is larger than the i-th ΔV_{th} level. For instance, two consecutive ΔV_{th} samples switching from level L1 to L3.
- Case (iii): Defect discharging. The (i-th)+1 ΔV_{th} level is smaller than the i-th ΔV_{th} level. For instance, two consecutive ΔV_{th} samples switching from level L3 to L1.

To construct the TM, the ΔV_{th} recovery trace is swept by its (i_i, i_{i+1}) elements and the transition location counter of the TM initial-final ΔV_{th} level is incremented when needed. Case-(i) transitions will lay in the main diagonal of the TM while case-(ii) and case-(iii) transitions will be located above and below the TM main diagonal, respectively. For instance, in Trace 1 of Fig. 8 (a), which is actually the same trace in Fig. 4 (a), ten ΔV_{th} levels have been detected by the WTLP method (Fig. 6 (a)). The resulting 10x10 TM is formed with all ΔV_{th} transitions identified during the ΔV_{th} recovery trace sweep as shown in Fig. 9 (a). In order to remove fast RTN transitions from the traces, the method analyzes the data in the TM, distinguishing the following two cases:

- *Slow emission recognition*: This type of defect emissions is characterized by a unique defect discharge to a lower ΔV_{th} level. In the TM, this appears as a '1' in the corresponding element below the TM main diagonal, and a '0' in the TM symmetric position. Analyzing the TM in Fig. 9 (a), three

different emissions, without any further capture, can be found marked with blue circles: from initial to final ΔV_{th} levels L4-L3, L6-L4 and L8-L7.

- *Transients recognition*: the method identifies multiple and consecutive transitions between two distinct ΔV_{th} levels. For instance, all transitions of the combined RTN signals in Fig. 4 (b), uncoupled by the WTLP method in Fig. 7 (b), are marked in the TM of Fig. 9 (a) with a green dashed square, which correspond to transitions from/to levels L0 to L3. A clear example of a transient in the TM is highlighted with a solid red square box, which corresponds to the RTN signal shown in the inset of Fig. 4 (a). The main diagonal (of the red square box) indicates the number of samples at the same ΔV_{th} level (i.e., initial and final ΔV_{th} levels L6 or L7) while hundred ten defect discharges (i.e., initial L7 to final L6) and 109 defect charges (i.e., initial L6 to final L7) take place in the RTN signal.

Fig. 10 displays the resulting 3 traces after the application of the methodology showing a total of 3, 8 and 4 slow emissions, respectively, without artifacts coming from fast defect transitions and background noise.

5) **Defect parameters extraction.** The last step is the obtention of the τ_e and η parameters of the slow defect emissions. This is done by locating the elements below the TM main diagonal showing single discharge that have a symmetrical zero above the TM main diagonal. The η value of each detected defect is obtained by the obtention of the size of the ΔV_{th} drop To allow the evaluation of the τ_e associated to

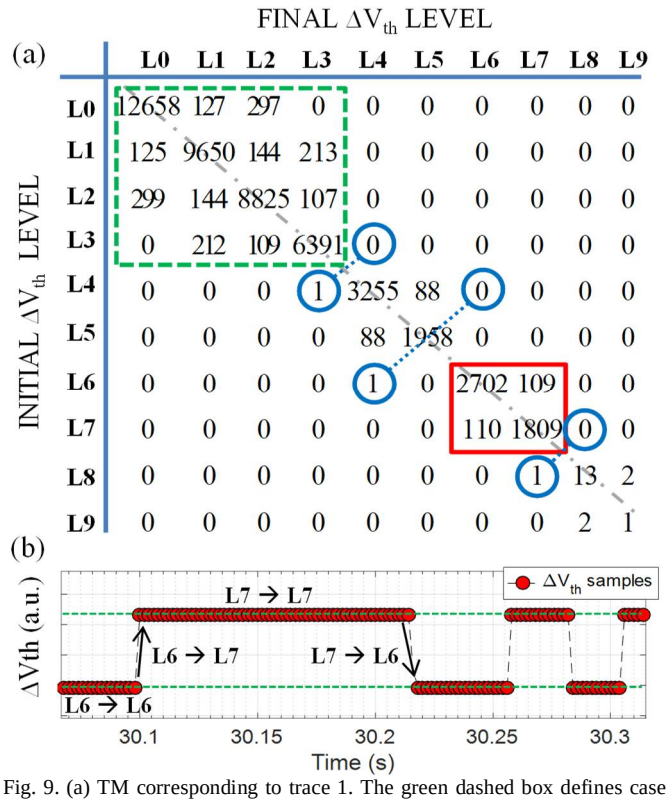

Fig. 9. (a) TM corresponding to trace 1. The green dashed box defines case (i), (ii) and (iii) transitions of the joint RTN in (b) while the red solid box defines the transitions of the fast defect switching shown in the inset in (a). Blue circles indicate the location of slow defect emissions and the main diagonal is highlighted with a grey dashed line. (b) Illustrative example of the two ΔV_{th} level transitions in the RTN signal in the inset in (a).

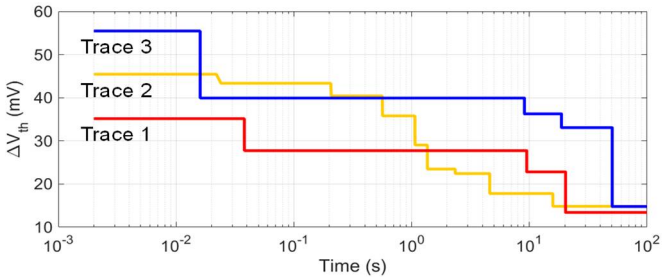

Fig. 10. Filtered recovery traces without noise and RTN ready for defect parameter extraction.

the defect, when the TM is constructed, also the times at which (i_i, i_{i+1}) transitions occur are saved. When a slow discharge is encountered, the τ_e is assigned to the computed η value so it the defect is characterized by the tuple $\{\tau_e, \eta\}$.

III. Experimental Results

In order to evaluate the validity of the described method, either BTI or HCI recovery data could be used. Here, four individual BTI tests, each one involving 248 CMOS transistors with 8 different channel sizes: 80nm/60nm, 200nm/60nm, 600nm/60nm, 800nm/60nm, 1000nm/60nm, 1000nm/100nm, 1000nm/500nm and 1000nm/1000nm. Fig. 11 shows a schematic representation of the measurement setup [12] used for the characterization of the transistors in the ENDURANCE IC chip with the following list of items:

- A full-custom printed circuit board (PCB), where the ENDURANCE IC chip is inserted for DUT measurements.
- The Keysight Semiconductor Parameter Analyzer (SPA) model B1500A.
- The Agilent E3631A power supply for PCB and IC biasing.
- The T-2650BV Thermonics precision temperature system.
- An USB Digital Acquisition System (DAQ), model USB-6501 from National Instruments.
- A personal computer (PC) equipped with Microsoft Windows® and Matlab®, both using a 64-bits architecture.

The Agilent E3631A power supply, the Keysight B1500A SPA and the Thermonics temperature system T-2650BV instruments are connected using an IEEE 488 General Purpose Interface Bus (GPIB), in order to send and receive data during tests executions. For the communication with the USB-6501 DAQ, a USB 3.0 connection is used.

During the BTI experiments, conducted at room temperature, each device has been tested using a 6-cycle SM scheme, in which the duration of the stress phases is increased exponentially (i.e., 1s, 10s, 100s, 1000s 10,000s and 100,000s), while the measurement (i.e., recovery) phase time is always 100s. During the stress period, a gate-source voltage V_{GS} has been applied maintaining the drain-source voltage V_{DS} at 0V (four different V_{GS} voltages have been considered), while for measurements $V_{GS} \approx V_{th}$ and V_{DS} = 100mV. The total test time required for a 6-cycle SM test on a single device takes 111,111s + (6·100s) = 111,711s ≈ 31 hours. Thus, for the four BTI tests involving 992 devices, the total test time, with

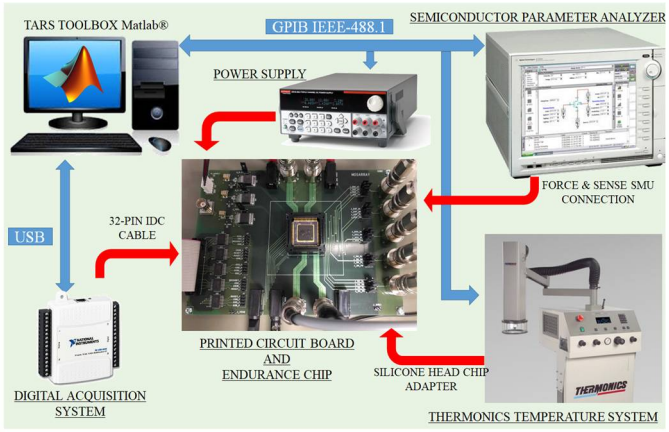

Fig. 11. Schematic representation of the instrumentation and their interconnections of the measurement setup.

conventional serial testing procedures, would be ≈ 3.5 years, a considerably large and rather prohibitive test time. In this work, and thanks to the array-based IC chip design, the stress phases of each BTI test have been parallelized, without overlapping the measurement phases of any device, thus significantly reducing the total testing time. The parallel stress technique follows the approach reported in [12] and aims at keeping minimum and equal time gaps in the transition from stress phases to measurement phases. In addition, stand-by periods (drain-source and gate-source voltages are kept at 0V) are introduced between the measurement and stress phases to make the necessary room to accommodate any number of DUTs in the tests. In this way, the efficiency of the test procedure is maximized. In this case, the testing time is reduced to only sixty-four hours per BTI test, resulting in a 4-BTI test that only lasts ten days, a significant test time reduction when compared to conventional serial testing.

From the automated analysis of the data, a total of 10,582 slow emissions have been identified. Fig. 12 shows the histogram plots of the extracted τ_e from the defects found during the recovery traces showing that charges are emitted

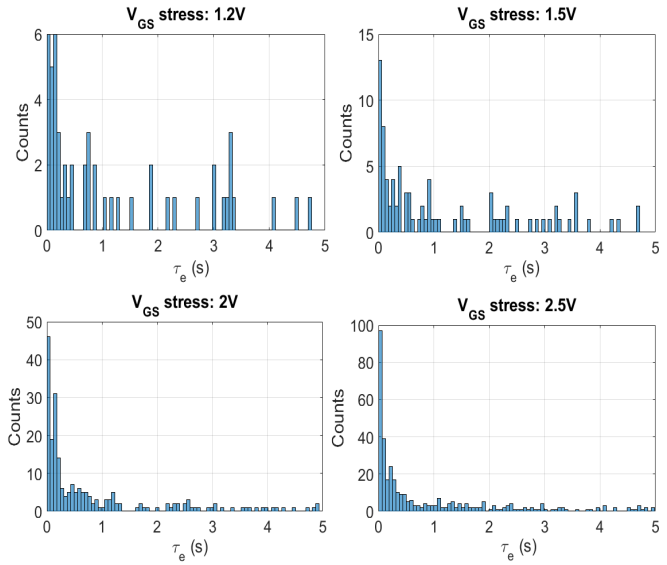

Fig. 12. τ_e histogram plots found during recovery analysis for the 80nm/60nm transistor geometry after 10,000s of BTI stress at four different V_{GS} stress voltages.

during the very first moments of the recovery phase utilizing the data extracted from the 80nm/60nm transistors, the smallest geometry. Fig. 12 also indicates an increasing V_{GS} voltage during the stress results in an increasing number of slow emissions.

Fig. 13 shows the statistical results obtained from the analysis of all $\{\tau_e, \eta\}$ tuples extracted by using the method detailed in this work. Fig. 13 (a) shows the dependence of the $\langle\eta\rangle$ value with the transistor area. The results demonstrate that $\langle\eta\rangle$ decreases with the transistor area. If the RTN related transients were not removed from the recovery traces before the slow emissions identification, a large number of 'false' events (with equal ΔV_{th} value as the RTN amplitude) would have been mistakenly considered during the $\langle\eta\rangle$ calculation. Therefore, the resulting $\langle\eta\rangle$ value, for all tested geometries, would have been closer to the ΔV_{th} of the fastest RTN, masking the actual $\langle\eta\rangle$ of the BTI-related defects. Fig. 13 (b) also shows that η is exponentially distributed. The results are in agreement with those in the literature [1], which supports the validity of the methodology.

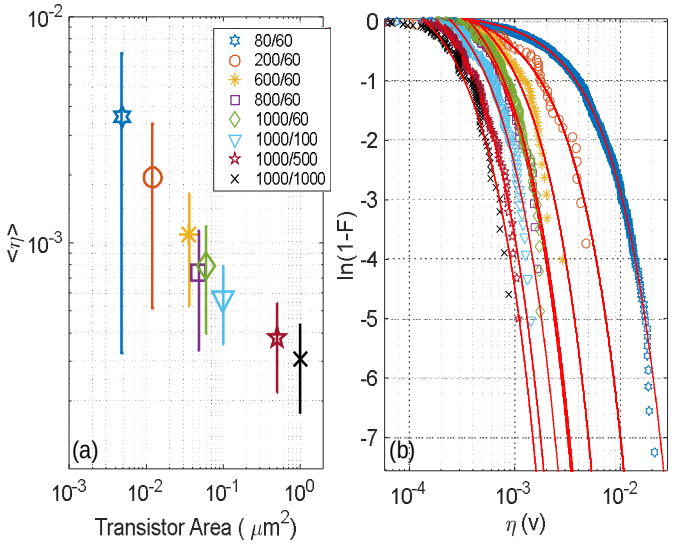

Fig. 13. (a) Distribution of the $\langle\eta\rangle$ values of the slow emissions as a function of the transistor area. (b) Exponential distribution of the η values, with exponential fitting extracted from the four 6-cycle BTI tests for each tested geometry.

CONCLUSION

In this paper, a smart method for the massive extraction of CMOS aging parameters has been presented. Our method analyzes the BTI/HCI aging recovery traces and looks for ΔV_{th} voltage drops related to slow emissions after the application of accelerated stress patterns. The method identifies and removes the fast transient capture/emissions (RTN) and the background noise in the recovery traces to avoid artifacts during the CMOS defect parameters extraction. In the application example, the described method has allowed to extract the $\{\tau_e, \eta\}$ tuples of more than 10,000 defects emissions that can be used as input parameters to stochastic aging compact models. Moreover, in order to reduce the testing time required for the massive analysis of the aging of nanometer MOSFETS (from years to days), our fabricated array-based IC chip in combination with a stress parallelization technique have been used.

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REFERENCES

[1] Kaczer B, Grasser T, Roussel PJ, Franco J, Degraeve R, Ragnarsson LA, et al. Origin of NBTI variability in deeply scaled pFETs. IEEE Int Reliab Phys Symp Proc 2010:26–32. doi:10.1109/IRPS.2010.5488856.

[2] Gao R, Manut AB, Ji Z, Ma J, Duan M, Zhang JF, et al. Reliable Time Exponents for Long Term Prediction of Negative Bias Temperature Instability by Extrapolation. IEEE Trans Electron Devices 2017;64:1467–73. doi:10.1109/TED.2017.2669644.

[3] Martín-Martínez J, Gerardin S, Amat E, Rodríguez R, Nafría M, Aymerich X, et al. Channel-hot-carrier degradation and bias temperature instabilities in CMOS inverters. IEEE Trans Electron Devices 2009;56:2155–9. doi:10.1109/TED.2009.2026206.

[4] Duan M, Zhang JF, Ji Z, Zhang WD, Kaczer B, Asenov A. Key Issues and Solutions for Characterizing Hot Carrier Aging of Nanometer Scale nMOSFETs. IEEE Trans Electron Devices 2017;64:2478–84. doi:10.1109/TED.2017.2691008.

[5] Martin-Martinez J, Diaz J, Rodriguez R, Nafria M, Aymerich X. New Weighted Time Lag Method for the Analysis of Random Telegraph Signals. IEEE Electron Device Lett 2014;35:479–81. doi:10.1109/LED.2014.2304673.

[6] Maestro M, Diaz J, Crespo-Yepes A, Gonzalez MB, Martin-Martinez J, Rodriguez R, et al. A new high resolution Random Telegraph Noise (RTN) characterization method for resistive RAM. EUROSOI-ULIS 2015 2015 Jt. Int. EUROSOI Work. Int. Conf. Ultim. Integr. Silicon, vol. 115, IEEE; 2015, p. 133–6. doi:10.1109/ULIS.2015.7063791.

[7] Mahapatra S, Parihar N. A review of NBTI mechanisms and models. Microelectronics Reliability 2018;81:127–35. doi:10.1016/j.microrel.2017.12.027.

[8] Toro-Frias A, Martin-Lloret P, Martin-Martinez J, Castro-Lopez R, Roca E, Rodriguez R, et al. Reliability simulation for analog ICs: Goals, solutions, and challenges. Integr VLSI J 2016;55:341–8. doi:10.1016/j.vlsi.2016.05.002.

[9] Kaczer B, Grasser T, Roussel J, Martin-Martinez J, O'Connor R, O'Sullivan BJ, et al. Ubiquitous relaxation in BTI stressing-new evaluation and insights. Proc. Int. Reliab. Phys. Symp., IEEE; 2008, p. 20–7. doi:10.1109/RELPHY.2008.4558858.

[10] Maricau E, Gielen G. Analog IC Reliability in Nanometer CMOS. New York, NY: Springer New York; 2013. doi:10.1007/978-1-4614-6163-0.

[11] Diaz-Fortuny J, Martin-Martinez J, Rodriguez R, Nafria M, Castro-Lopez R, Roca E, et al. A transistor array chip for the statistical characterization of process variability, RTN and BTI/CHC aging. Proc. 14th Int. Conf. Synth. Model. Anal. Simul. Methods Appl. to Circuit Des., 2017. doi:10.1109/SMACD.2017.7981600.

[12] Diaz-Fortuny J, Martin-Martinez J, Rodriguez R, Nafria M, Castro-Lopez R, Roca E, et al. TARS: A toolbox for statistical reliability modeling of CMOS devices. Proc. 14th Int. Conf. Synth. Model. Anal. Simul. Methods Appl. to Circuit Des., 2017. doi:10.1109/SMACD.2017.7981601.

[13] Grasser T, Reisinger H, Wagner P-J, Schanovsky F, Goes W, Kaczer B. The time dependent defect spectroscopy (TDDS) for the characterization of the bias temperature instability. Proc. IEEE Int. Reliab. Phys. Symp (IRPS)., 2010, p. 16–25. doi:10.1109/IRPS.2010.5488859.

[14] Kaczer B, Grasser T, Roussel PJ, Martin-Martinez J, O'Connor R, O'Sullivan BJ, et al. Ubiquitous relaxation in BTI stressing-new evaluation and insights. Proc Int Reliab Phys Symp 2008:20–7. doi:10.1109/RELPHY.2008.4558858.

[15] Maestro M, Diaz J, Crespo-Yepes A, Gonzalez MB, Martin-Martinez J, Rodriguez R, et al. New high resolution Random Telegraph Noise (RTN) characterization method for resistive RAM. Solid State Electron 2016;115:140–5. doi:10.1016/j.sse.2015.08.010.

[16] Nagumo T, Takeuchi K, Yokogawa S, Imai K, Hayashi Y. New analysis methods for comprehensive understanding of Random Telegraph Noise. 2009 IEEE Int Electron Devices Meet 2009:1–4. doi:10.1109/IEDM.2009.5424230.