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Two-Step RF IC Block Synthesis with Pre-Optimized Inductors and Full Layout Generation In-the-loop

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***Abstract*—In this paper, an analysis of the methodologies proposed in the past years to automate the synthesis of radio-frequency (RF) integrated circuit blocks is presented. In the light of this analysis, and to avoid non-systematic iterations between sizing and layout design steps, a multi-objective optimization-based layout-aware sizing approach with pre-optimized integrated inductor(s) design space is proposed. An automatic layout generation from netlist to ready-to-fabricate prototype is carried in-the-loop for each tentative sizing solution using an RF-specific module generator, template-based placer and evolutionary multi-net router with pre-optimized interconnect widths. The proposed approach exploits the full capabilities of the most established computer-aided design tools for RF design available nowadays, i.e., RF circuit simulator as performance evaluator, electromagnetic simulator for inductor characterization, and layout extractor to determine the complete circuit layout parasitics. Experiments are conducted over a widely-used circuit in the RF context, showing the advantages of performing complete layout-aware sizing optimization from the very initial stages of the design process.**

***Index Terms*—Automatic layout generation, electronic design automation, integrated inductors, layout-aware sizing, multi-objective optimization, radio-frequency integrated circuits.**

I. Introduction

Nowadays, radio-frequency (RF) integrated circuit (IC) design must be fulfilled at minimal costs under severe time-to-market constraints due to the high demand for wireless data communication systems, where these circuits play a major role. Avoiding costly re-design cycles and minimizing post-fabrication tuning and compensation work for first-pass fabrication success have become important objectives in circuit design [1]. However, RF circuits are among the most difficult ones to design not only due to the extremely wide range of frequencies and dynamic ranges involved, but also due to their dependence from non-reliable models of passive devices, e.g., integrated inductors, which are still the most critical integrated components, and to the catastrophic impact of layout parasitics at gigahertz frequencies.

Regarding integrated inductors, equivalent analytical models have been developed to avoid the usage of computationally-expensive electromagnetic (EM) simulators during the initial stages of the design process. However, these models fail to accurately predict performances of the complete inductor design space, ultimately leading to design errors. Moreover, to account for layout parasitics during manual design, RF designers must at least draw a first-cut layout for a satisfactory sizing solution, and then, the parasitics extracted from that solution are used as an estimation for the subsequent re-sizing process, until all design specifications are met. This manual methodology leads to undesired and time-consuming re-design iterations between electrical and physical design steps, since the parasitics of only one layout are considered for different active and passive device sizes, and, in addition, the results of this process remain ultimately unpredictable. One viable way to deal with these bottlenecks is to develop and adopt RF-specific electronic design automation tools.

In this paper, an automatic synthesis methodology targeted at RF IC blocks is proposed to tackle the abovementioned problems. The methodology combines EM-characterized integrated inductors and, for the first time in this research field, in-the-loop and accurate parasitic extraction from ready-to-fabricate layout prototypes during a sizing optimization procedure. Unlike previous solutions, where approximated/ custom solutions are taken for inductors and/or circuit layout parasitics, this methodology exploits the full capabilities of established off-the-shelf tools for RF IC design, i.e., EM simulator, RF circuit simulator and layout parasitic extractor. By doing so, the methodology introduces automation at the block-level design flow, providing robust solutions by automatically exploring the layout-aware design space, without driving designers away from their current workspace and traditional tools.

This paper is organized as follows. In section II, the state-of-the-art is reviewed and the innovative contributions of this work discussed. In section III, the architecture of the two-step layout-aware flow for RF IC blocks is described, and, in section IV, the automatic in-the-loop layout generation is

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discussed. In section V, implementation results are presented, and, finally, in section VI, the conclusions are drawn.

II. State-of-the-Art Review and Discussion

Nowadays, the automation of analog, mixed-signal and RF IC sizing by means of optimization-based techniques is an established concept, where either circuit simulators or analytical models are used to accurately evaluate or estimate, respectively, the performances of the tentative solutions, as referred in [2]. These optimization-based design methodologies overcome the drawbacks of knowledge-based design approaches by using search algorithms that efficiently explore the design space, whereas knowledge-based methodologies apply an iterative procedures to size each device from user-defined analytical equations [3]. Still, to achieve robust circuit designs, complete layout parasitic effects must be considered during the optimization flow. In order to develop a successful RF IC layout-aware synthesis methodology, four key aspects must be considered that will help us to classify and compare existing approaches: (1) how the circuit performances are evaluated; (2) how the integrated inductors are modeled, since they play a fundamental role; (3) how the full circuit layout parasitics are extracted; and, finally, (4) how the in-the-loop layout generation is carried out.

In the next sub-sections, how inductor modelling can be considered into the optimization-based methodologies is first reviewed, and afterwards, the methodologies to include a wider set of circuit layout parasitics and complete layout-aware tools are overviewed. Finally, the innovative contributions of this work are discussed.

A. Integrated Inductor Modeling

Inductors have a high impact on the performances of the vast majority of RF circuits and systems. For this reason, several authors have discussed the accurate evaluation of their performances during circuit optimization. One possibility is to use limitative foundry-provided inductor libraries, as performed in [4–6], which reduces the possibility of finding an optimal inductor for a given application. In [7], a compact model is used to incorporate some inductor parasitics during the simulated-annealing-based optimization of RF power amplifiers. Other approaches use approximate inductor analytical models, π-models [8–11] or 2–π-models [12], and have been applied to different circuit classes. In a different direction, Liu et al. [13] proposed a simulation-based optimization approach for RF amplifiers, where machine learning techniques are used to build an inductor surrogate model. The accuracy of such model is iteratively improved by refining the model with EM simulation results of promising inductors, instead of performing EM simulation of each candidate inductor, as in [14]. Finally, to avoid in-the-loop EM simulations, in [15, 16], a Pareto-optimal front (POF) of EM-simulated inductors is obtained priorly to any circuit optimization, and, then, the POF is used as inductor design space (IDS) during circuit sizing. This constitutes, essentially, a two-step solution. These approaches, schematized in Figs. 1(a) and (b), still require, however, a subsequent design stage to handle the circuit layout parasitics.

B. Parasitic-Inclusive Methodologies

Attempting to shorten the gap between circuit and layout design steps, a parameterized layout generator and full parasitic extraction are used in [17] to sample the effects of critical interconnect parasitics and on-chip inductors. Their impact is embedded into symbolic models, which are then used to estimate the circuit performances. More recently, in [18], a hybrid scheme of geometric programming and a many-objective evolutionary algorithm is used with performance models (PMs) derived for different analog and RF circuits. Device and interconnect parasitics are modeled into symbolic models, using foundry-provided equations and analytical models, respectively.

Following the manual process that is carried out by designers, in [19], a set of parasitic corners are identified with statistical analysis over earlier/rough placement solutions. Then, the circuit is re-optimized using linear correlations between parasitics and performances. The layout is generated *a posteriori* using a performance-driven methodology, where performance macro models constrain the layout generation. Similar approaches are taken in [20], where the parasitic

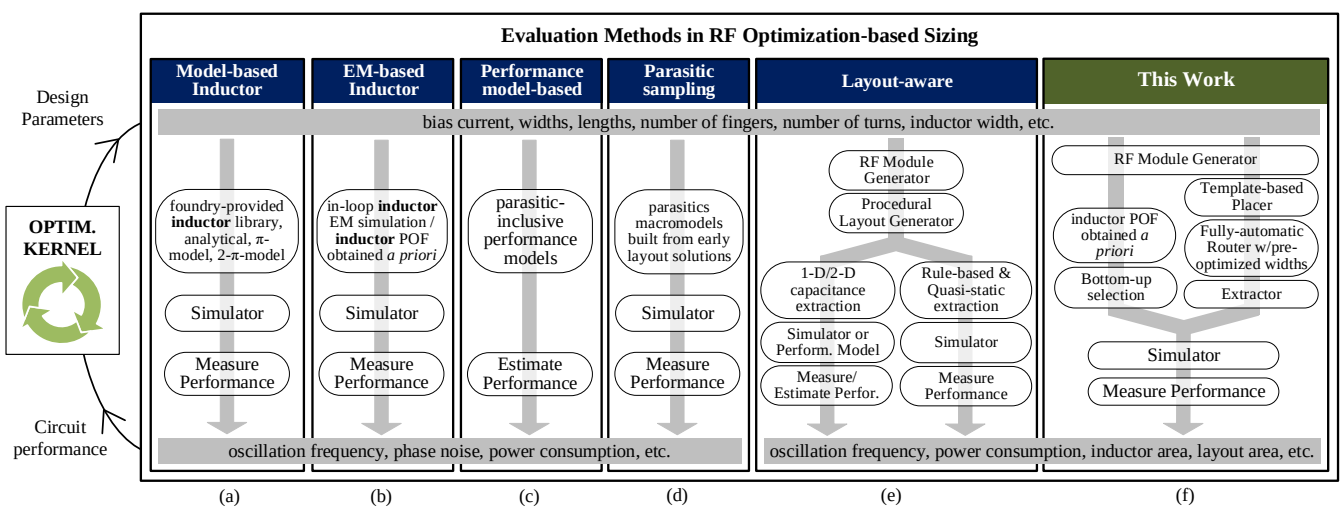

Fig. 1. (a) Model-based inductor [4–12], (b) EM-based inductor [13–16], (c) Performance-model-based [17, 18], (d) Parasitic sampling [19–21], (e) Procedural layout generation & custom parasitic extraction [22, 23] evaluations performed in RF sizing optimization; (f) Proposed RF layout-aware sizing optimization.

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bounds are estimated only within a feasible region firstly identified, and, in [21], where the optimization is carried over a parasitic-parameterized netlist instead. These approaches are schematized in Figs. 1(c) and (d).

C. Layout-aware Sizing

The first RF-specific methodology to incorporate full layout generation into a sizing optimization loop was proposed in [22]. There, a specific module generator with RF building blocks embedded in a procedural layout generator was used to create the layout of each tentative sizing, and then, the parasitics of the critical nets were extracted using 1-D/2-D capacitance models and back-annotated in the netlist. The solutions were evaluated by a circuit simulator or, alternatively, estimated in manually derived PMs to speed up the optimization. Still, no results with integrated inductors are reported. In [23], an RF-specific procedural layout generator is also used, and, a more extensive set of parasitics are obtained using standard rule-based and quasi-static inductance extraction techniques, as illustrated in Fig. 1(e).

Layout-aware sizing approaches for baseband analog IC design with explicit layout generation in-the-loop have been reported in recent literature. The most successful approaches discarded the procedural layout generators and adopted template-based approaches [24–27] or complete enumeration of the hierarchical floorplan [28], improving the compactness of the floorplan for broader variations on devices' sizes. The solutions reported in [26, 27] consider multiple floorplan templates to simultaneously pack every sizing solution, and discard the template-based router in favor of an automatic electromigration-aware approach. Moreover, custom 2-D/2.5-D extraction of parasitic capacitances and resistances of all devices and interconnections is performed.

D. Discussion & Contributions

Table I summarizes the characteristics of each work overviewed above and the contributions of the proposed approach. Regarding the first key aspect (circuit performance evaluator) listed above for a layout-aware synthesis methodology, PMs for circuit evaluation are error-prone, inaccurate, must be specifically derived for each circuit topology and have unexpected behavior in several regions of the design space. Off-the-shelf circuit simulators are probably the most established CAD tool in the RF design flow, being used to verify the circuit performances from the early design stages until post-layout validations. Therefore, this is a mandatory requirement for high accuracy, while simultaneously easing the inclusion of automation in the design flow. In terms of inductor modeling and simulation (criterion (2) above), EM simulators are the most accurate performance evaluators available to predict all parasitic effects of integrated inductors. This, however, comes at the expense of a high computational time. Physical/analytical models for inductor modeling lie at the opposite end of the accuracy-efficiency trade-off: short synthesis times but with the lowest accuracy. Therefore, they should be avoided during automatic approaches to calculate an accurate parameter set for the inductors, as shown in [29].

For parasitic consideration (criterion (3)), there are two distinct approaches to include a broader set of circuit layout effects: prior layout sampling or layout generation in-the-loop. Methodologies with accurate integrated inductor modeling of section II.A fail to consider other layout parasitics, while the ones in section II.B estimate them, but still do not perform an explicit layout generation in-the-loop for each tentative sizing. In prior layout sampling, the parasitic information associated with a single layout design or the statistical analysis over several early layout designs do not capture all parasitic variations that could be found during re-sizing, and several promising solutions may be lost. While layout generation in-the-loop represents an overhead during optimization, having the layout readily available allows computing the precise parasitics for each specific solution without approximations, as well as readily providing a layout for fabrication.

TABLE I
COMPARISON BETWEEN STATE-OF-THE-ART WORKS ON RF IC SIZING OPTIMIZATION

Work	Performance Evaluator/Estimator	Inductor Modeling	Circuit Layout Parasitics		In-Loop Layout Generation	
			Extraction Method	Parasitic Included	Placement	Routing
Vancoreland [8], 2001	Circuit simulator & performance models	not included	Foundry & 1/2-D analytical models	Device and interconnect C and CC	Procedural generator	
Gupta [7], 2001	Parametric equations	Parasitic-incl. compact model	not included		not included	
Ranter [14], 2002	Circuit simulator	In-the-loop EM simulation	not included		not included	
Zhang [19], 2004	Performance models	Linear behavior into PMs	Custom analytical models	not specified	not included	
Ranjan [17], 2004	Symbolic models	Custom quasi-static extraction	Mixed rule-based & quasi-static	Full device and interconnect	not included	
Bhaduri [23], 2004	Circuit Simulator				Procedural generator	
Agarwal [20], 2005	Performance models	Sampling and extraction embedded into PMs	Off-the-shelf extractor	Inter-module not specified	not included	
Nieuwoudt [9], 2007	Analytical models	π models	π models	Other passive components	not included	
Liu [13], 2012	Circuit Simulator	EM-based Surrogate model built in-the-loop	not included		not included	
Póvoa [6], 2014	Circuit Simulator	Foundry-provided libraries	not included		not included	
Afacan [12], 2016	Circuit simulator	2-π models	2-π models	Other passive components	not included	
González [16], 2017	Circuit simulator	EM-simulated POF obtained *a priori* (two-step approach)	not included		not included	
Liao [18], 2017	Performance models	Linear behavior into PMs	Foundry & custom analytical models	Device and interconnect C, CC and R	not included	
This work	Circuit simulator	POF from EM-based Surrogate model (two-step)	Off-the-shelf extractor	Full device & interconnect (IDS previously set)	Template-based	Multi-net automatic

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The only RF-specific methodologies of section II.C eligible for criterion (4) adopt limitative and hard-to-define procedural layout generators, and, therefore, the paradigm must be changed. For parasitic extraction, the analytical/geometrical 1-D/2-D/2.5-D and rule-based methods overviewed in literature present satisfactory results for baseband design [30], however, the accuracy of such extraction is inferior when compared to the accuracy of commercial extractors. Regarding the parasitic estimation, the traditional benchmark verification tool for RF designers is EM simulation. To fully validate a given layout, the entire circuit (without its active part) must be EM simulated to fully consider its parasitic capacitances, resistances and inductances. Therefore, the full parasitics of the circuit should be accounted for in the earlier phases of the design process to shorten this gap.

As a final note, beyond all the approximations that may be made in the field of RF IC synthesis, the designers' confidence will always and ultimately rely on established CAD verification tools. Therefore, for the first time in the literature, the proposed RF layout-aware design methodology combines: (1) a circuit simulator for accurate performance evaluation; (2) an integrated inductor characterization using EM-based surrogate modeling to set the optimal IDS, and, a weighted nearest P-neighborhood with tail technique to map it during the circuit optimization; (3) an approach for computing the complete set of circuit layout parasitics with an accurate off-the-shelf extractor from ready-to-fabricate layout prototypes, which are fully generated in-the-loop. This step is performed aware that all layout structures added during prototyping, e.g., inductors' shielding, pads, buffers, etc., and associated routing, have a drastic impact on the circuit performance; and finally, and for the first time reported in RF layout automation, (4), an RF-specific module generator, template-based placement and evolutionary multi-net automatic routing with pre-optimized interconnect widths, thus avoiding the limitations of procedural generators.

III. Proposed Layout-Aware Flow for RF IC Blocks

The general description of the methodology is illustrated in Fig. 1(f), and the detailed flow is shown in Fig. 2. The two-step bottom-up design methodology is divided into: construction of a surrogate model for the inductors to determine the optimal IDSs, and, layout-aware sizing optimization, the latter encompassing several other complex tasks. Following a bottom-up approach, the two distinct phases communicate through the generated integrated inductor POF(s).

A. Integrated Inductor Design

A Gaussian-process surrogate inductor modeling technique is adopted to avoid inaccurate physical/analytical models and the inefficiency of EM simulations. Surrogate modelling is an engineering technique used when the most accurate performances of a given system cannot be easily (or cheaply) measured. The model is built from (expensive) accurate evaluations of the system behavior at a limited number of training data samples that cover the design space evenly. The samples can be selected using different techniques, e.g., classical Monte Carlo, quasi Monte Carlo or Latin Hypercube Sampling. In the results reported in this paper, quasi Monte Carlo sampling was used. In our approach, EM simulations of the parameterized cell of the desired topology, e.g., the octagonal symmetric spiral inductor with shielding of Fig. 3(a), using the geometric parameters of the data samples, i.e., inner diameter, number of turns and turn width, are performed. Afterwards, the EM simulation results are used to train the surrogate structure that models the complete inductor search space using the setup proposed in [31], and illustrated in Fig. 2(a). The surrogate model is able to cheaply predict the system

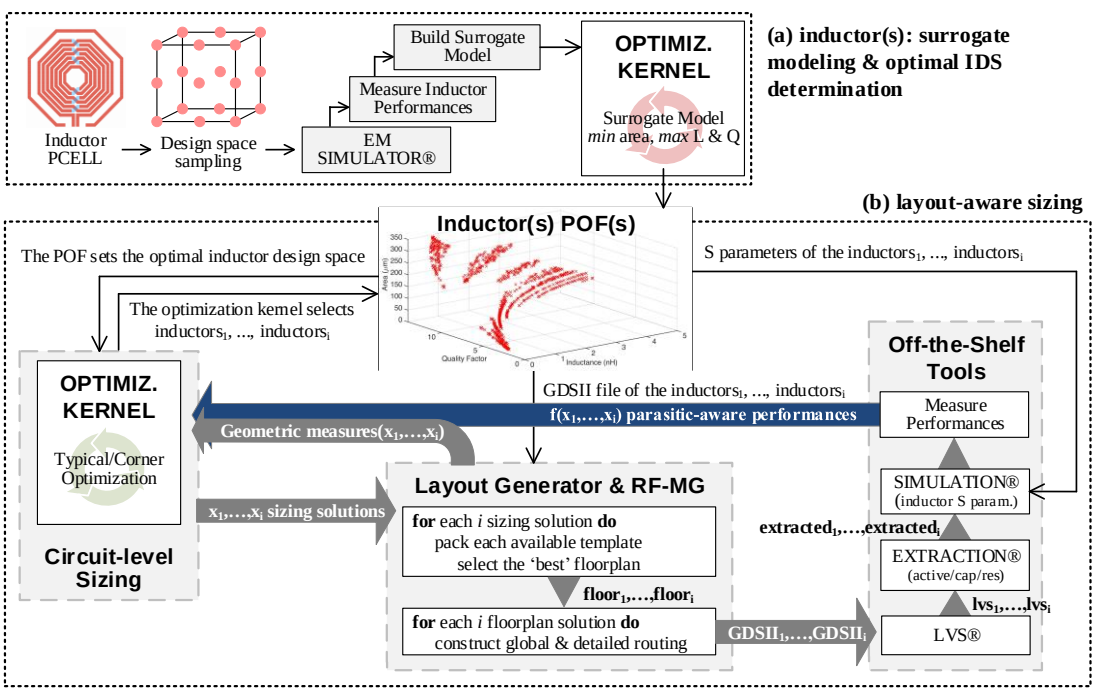

Fig. 2. Proposed two-step RF-specific layout-aware synthesis flow: (a) Integrated inductor design using Gaussian-process surrogate modeling and optimal IDS determination, and, (b) Layout-aware circuit sizing loop.

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performances for non-sampled points. A set of EM-simulated inductor samples, not used in the model training, can also be used to validate the model in different regions of the search space, and eventually increase the number of training samples. The surrogate model offers less than 1% error when compared to EM simulations for non-sampled inductor designs, while the simulation time is reduced by several orders of magnitude after the training period. This accuracy level is obtained with a few hundred samples of the inductor geometries (800 samples in the experiments shown in this paper). This number of samples is sufficient to reach this prediction accuracy while their EM simulation (using ADS Momentum®) is still manageable (a few days of CPU time). It must be taken into account that this procedure is performed *a priori* and only once for each new inductor topology added and technology process used. The generated information can be reused for as many surrogate models as desired for any frequency of operation.

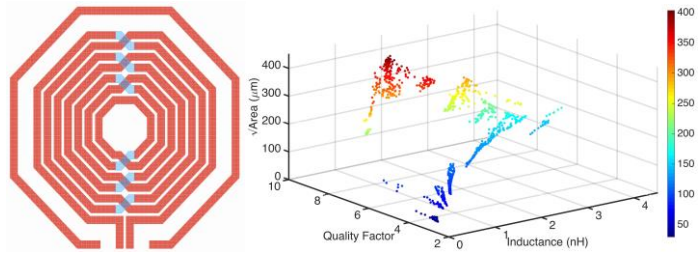
Afterwards, a bottom-up synthesis approach is adopted, where the optimal IDS is determined first, and then, composed up the hierarchy. The concept of using POFs for electronic design was introduced in [32], and later successfully applied by several authors to hierarchical bottom-up sizing of analog, mixed-signal [33, 34] and RF circuit classes [16]. For this purpose, a NSGA-II-based [35] multi-objective optimization is performed, using the surrogate model as an inductor performance evaluator, to readily obtain a POF of inductors, as illustrated in Fig. 2(a). The kernel was designed to solve the general constrained multi-objective problem defined as:

$$\begin{aligned} &\text{find } x \text{ that minimize } f_m(x) && m = 1,2,...M \\ &\text{subject to } g_j(x) \geq 0 && j = 1,2,...J \\ &x_i^L \leq x_i \leq x_i^U && i = 1,2,...N \end{aligned} \tag{1}$$

where, x is the vector of N design variables, $g(x)$ the J constraint functions (performances, or analytic functions of the performances, that should be made larger than a specified value) and $f(x)$ the M objective functions (performances, or analytic functions of the performances, that should be minimized). The objective functions are set to minimize the inductor area, and maximize both the quality factor (Q) and the inductance (L). Optimization constraints are added to ensure that the inductance value is sufficiently flat from DC to slightly above the operating frequency, and that the self-resonance frequency is sufficiently above this frequency. The result of this optimization is the POF of Fig. 3(b), which shows the best tradeoffs among area, Q and L. The POF is then used as input of the layout-aware flow and define the IDS, providing the S-parameter files that accurately describe its behavior for circuit simulation.

B. Layout-aware Sizing Loop

In this section, the generic netlist of the voltage-controlled oscillator (VCO) of Fig. 4 is used to illustrate the methods adopted in the layout-aware sizing loop of Fig. 2(b), which are also sketched on Algorithms 1 and 2. The major steps are briefly overviewed in order:



(a) (b)

Fig. 3. (a) Instance of the octagonal symmetric inductor with shielding; (b) POF of 1000 points with the tradeoff √Area (μm) vs. Quality factor vs. Inductance (nH) of the octagonal symmetric inductor with shielding that sets the optimal IDS for bottom-up layout-aware sizing.

```
1.  .SUBCKT VCO
2.  Ind I=Vout+   O=Vout- PARAM=[inductor from the POF of Fig. 3(b)]
3.  Cvar1 A=netvar C=Vout-  B=Gnd PARAM=[width length nrows ncolumns]
4.  Cvar2 A=netvar C=Vout+ B=Gnd PARAM=[width length nrows ncolumns]
5.  Cpoly1 A=Vtune  C=Vout-  B=Gnd PARAM=[width length]
6.  Cpoly2 A=Vtune  C=Vout+ B=Gnd PARAM=[width length]
7.  nmos1  D=Vout-  G=Vout+ S=Gnd   B=Gnd PARAM=[width length nfingers]
8.  nmos2  D=Vout+ G=Vout-  S=Gnd   B=Gnd PARAM=[width length nfingers]
9.  pmos1  D=Vout+ G=Vout-  S=net12 B=Vdd PARAM=[width length nfingers]
10. pmos2  D=Vout-  G=Vout+ S=net12 B=Vdd PARAM=[width length nfingers]
11. pmos3  D=IBp    G=IBp   S=Vdd   B=Vdd PARAM=[width length nfingers]
12. pmos4  D=net12  G=IBp   S=Vdd   B=Vdd PARAM=[width length nfingers]
13. .ENDS
```

Fig. 4. Generic netlist of a VCO. Values inside PARAM can be changed by the optimization kernel.

1) Optimization Kernel (lines 2-8 of Algorithm 1)

The circuit optimization is also carried out by the NSGA-II kernel, that selects different sizing solutions, each one with a new set of design variables x (e.g., width, length or number of finger of the transistors' $nmos_{1,2}$ or $pmos_{1,2,3,4}$, number of fingers per row and number of fingers per column of the varactors C_{var1} and C_{var2}, etc.). The number of design variables defines the space order, while the variable ranges will define the size of the search space. The kernel is set to solve the multi-objective problem of equation (1). However, circuit design specifications are traditionally formulated as:

$$\begin{aligned} g_j^L &= p_k(x) \geq P_j^L && j = 1,2,...,LB, k \in \{1,2,...A\} \\ g_j^U &= p_k(x) \leq P_j^U && j = 1,2,...,UB, k \in \{1,2,...A\} \end{aligned} \tag{2}$$

where a set of LB lower bounds, P^L_j, and UB upper bounds, P^U_j, for some of the A measured circuit characteristics, $p_k(x)$, are imposed during optimization, e.g., oscillation frequency equal or above 2.45 GHz (lower bound) and oscillation frequency equal or below 2.55 GHz (upper bound). Therefore, the general problem formulation of equation (1) is transformed and treated in compliance with:

$$f_m(x) = \begin{cases} p_m(x) \text{ when minimizing } p_m(x) \\ -p_m(x) \text{ when maximizing } p_m(x) \end{cases}$$

$$g_j(x) = \begin{cases} \dfrac{p_k(x) - P_j^L}{|P_j^L|} \text{ when the design specification is } p_k(x) \geq P_j^L \\ p_k(x) \text{ when the design specification is } p_k(x) \geq 0 \\ -p_k(x) \text{ when the design specification is } p_k(x) \leq 0 \\ \dfrac{P_j^U - p_k(x)}{|P_j^U|} \text{ when the design specification is } p_k(x) \leq P_j^U \end{cases} \tag{3}$$

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where $p_m(x)$ are the circuit's performance metrics being optimized, e.g., power consumption or phase noise at 10 MHz offset from central oscillation frequency. The optimization of electronic circuits using genetic algorithms, and particularly, the application of genetic operators to devices' dimensions or bias voltages/currents, is a widely acknowledged concept. However, the use of POFs from lower hierarchical levels to optimize higher levels in the hierarchy poses additional problems to these evolutionary algorithms. This is the case of inductors (line 2 of the netlist of Fig. 4), where a tuple of performances (i.e., area, Q and L) cannot be efficiently used as design variables as their values are not regularly distributed. Therefore, to effectively explore the set of N_{IND} solutions at the inductor POF when optimizing the complete circuit, the inductors must be mapped and organized in such a way that the mutation operator most probably make "small changes" to the currently selected solution (as mutation is expected to operate). In this work, the weighted nearest P-neighborhood with tail mapping, proposed in [36], is adopted to map the pre-optimized inductors during the circuit optimization. Unlike mapping methods based on sorting only [16], here the distance between inductors in their performance space determines the behavior of the mutation operator applied.

Formally, the probability $s_b(x)$ of the inductor b being selected when the evolutionary mutation operator is applied to a solution whose inductor is a, is given by:

$$s_b(x) = \begin{cases} \dfrac{\left(\dfrac{1}{d_{a,b}}\right)}{\sum_{c\in\theta_a}\left(\dfrac{1}{d_{a,c}}\right)+2\left(\dfrac{1}{d_{a,d}}\right)} & \forall b \in \theta_a \\ \dfrac{\left(\dfrac{2}{(N_{IND}-P-1)\,d_{a,d}}\right)}{\sum_{c\in\theta_a}\left(\dfrac{1}{d_{a,c}}\right)+2\left(\dfrac{1}{d_{a,d}}\right)} & \forall b \notin \theta_a \end{cases} \quad (4)$$

where P is the number of points in the neighborhood of each inductor; θ_a is the neighborhood of inductor a, i.e., the set of the P inductors closest to a in their Euclidean performance space; subscript d refers to the inductor which is closest to a and is not in θ_a, and $d_{a,x}$ is the Euclidean distance from inductor a to any other inductor x. The size limit of θ_a ensures scalability by limiting the amount of probability values stored, and inductors in θ_a are selectable with a probability that grows inversely with the distance. Inductors not in θ_a are selectable as well, all with the same, small, probability. This tail accounts for the existence of clusters in the IDS (which may appear due to the constraints imposed in the inductors and the discrete nature of search space), as illustrated in Fig. 5, where some solutions would become inaccessible from others. Such mapping strategy proved to outperform other strategies such as matrix mapping, nearest neighbor ordering or nearest P-neighborhood without tail for several experiments [36].

2) *Layout Generator & RF module generator (Algorithm 2)*

The inductors from the inductor POF are imported as GDSII files, and the remaining modules generated using an internal RF module generator. Afterwards, the available placement templates are packed for each sizing. Since any geometrical requirement from the layout can be imposed as a constraint or an objective for the optimization problem, the floorplan that suits most of those requirements, for each sizing, is passed to the Router. Here, a wiring topology, global routing and detailed routing solutions with wiring symmetry are devised for each floorplan. Further details on the layout generator are described in section IV.

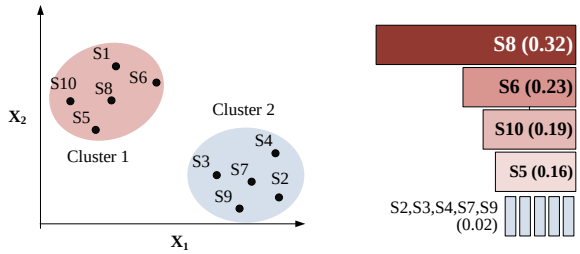

Fig. 5. Illustration of the weighted nearest P-neighborhood with tail mapping and corresponding probability of being selected by the mutation operator on a set of 10 solutions (S1-S10) for the 4-neighborhood of S1.

Algorithm 1 Layout-aware Sizing

input: **List**<**Ind**<**S-Param** s-param**, GdsII** lay>> *IDS // inductor design space*
Circuit<**Netlist** netlist, **List**<**Testbench**> tb> C *//netlist and testbench(es)*
Requirements<**List**<**f(x)**>, **List**<**g(x)**>> *R //set of objectives and constraints*
List<**Template**> *T //list of high level guidelines for placement*
output: **List**<**Sizing**<**Variables** x**, Performance** px>> *Layout-Aware-POF*

1. #define **List**<**Sizing**<**Variables** x**, Performance** px>> *Parents, Offspring*
2. *Parents:*= New random sizing solutions
3. Evaluate(*Parents*)
4. **while** generation++ < G_{max} **do**
5. *Offspring:*= Apply mutation and crossover to *Parents*
6. Evaluate(*Offspring*)
7. *Parents:*= Select top half of {*Parents, Offspring*} sorted according to dominance and crowding distance using *R*
8. **return** *Parents*
9. **function** Evaluate(**List**<**Sizing**<**Variables** x**, Performance** px>> *S*) **do**
10. **for** each **sizing** s_i in *S* **do**
11. *GDSII* := LayoutGenerator(s_i<***x***>, *C*<**netlist**>, *T, R, IDS*) *//Alg. 2*
12. *LVS* := Run Calibre® nmLVS(*C*<**netlist**>, s_i<***x***>, *GDSII*)
13. *GDSII* := Remove inductors from layout
14. *PEX* := Run Calibre® xRC(*LVS, GDSII*)
15. *PEX* := *PEX* + back-annotate the S-parameters from *IDS*<**s-param**> into the extracted netlist
16. *FX* := Run Eldo® RF(*N*<**tb**>>, *PEX*)
17. s_i<***px***> := Store {*FX*<***pnoise, fosc, …***>, *GDSII*<***area, width, ...***>} the electrical and geometrical performance measures

3) *Off-the-Shelf Tools (lines 12-16 of Algorithm 1)*

The automatically generated layouts are saved as GDSII files and passed to the external tools. In a first phase, Mentor Graphics' Calibre nmLVS® (layout-versus schematic) is used to ensure compliance of the automatically generated GDSII file with the circuit netlist (Fig. 4). Afterwards, the Calibre nmLVS® report is used in Mentor Graphics' Calibre xRC® tool to extract all parasitic structures from the complete set of active, capacitive and resistive devices of the circuit. Nonetheless, the support of a different external layout-versus schematic tool or extractor is only dependent of executing different calls during this phase, i.e., if the input/output SPICE-like netlist format files hold, any tool can be easily

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integrated in the flow. Integrated inductors are ignored at the previous extraction, since a more accurate extraction is already included in the EM-based surrogate model. Therefore, the corresponding S-parameters from the inductors are back-annotated into all the extracted netlists as *Fblock* devices (used specifically to simulate devices whose description is based on S-parameters). The parasitic-aware performances from the entire circuit (extracted netlist and *Fblock*(s)) are measured from a set of testbenches (DC, steady-state analysis, steady-state noise, etc.) using Mentor Graphics' Eldo RF®, and used in the optimization process together with the accurate geometrical properties of the circuit measured by the Layout Generator.

The proposed approach is flexible to any RF circuit class, e.g., VCOs, low-noise amplifiers, mixers, etc., and the inputs required from the designer are the parameterized circuit and testbench(es) with corresponding analyses and measures. The ranges of the design variables and design specifications can be specified using a graphical interface developed for the framework. For the layout generation, only the floorplan template(s) must be specified.

IV. In-The-Loop Automatic Generation of the Ready-to-Fabricate Layout Prototype

This section provides further details on the layout generation that is carried in-the-loop: first, the template-based Placer, followed by the fully-automatic Router.

A. Template-based Placer (lines 4-9 of Algorithm 2)

The proposed Placer is built over the template-based approach for analog and mixed-signal IC blocks introduced in [37], where the designer is responsible for providing a high-level floorplan description, and then, all the instantiation and packing procedures are performed automatically given any set of device sizes. Similarly, the RF module generator is an extension to other RF devices and constructs, e.g., double-poly capacitors, varactors, RF MIMs, RF MOSFETs, guard-rings, options to extend the inductors' shielding to surround other parts of the circuit, etc., of the technology-independent module generator. Inductors are imported as GDSII files. Also, the same can be performed for other fixed layout structures (e.g., pads).

The high-level floorplan guidelines are provided in a XML form, using simple structures that capture the matching, proximity and topological relations that the designer wishes to impose. A template description for the VCO netlist of Fig. 4 is illustrated in Fig. 6. As it is shown, the template hierarchy should be refreshed every time that additional constructs are needed, e.g., N-type/P-type guard-ring around PMOS/NMOS devices and inductor shielding around the complete block. This set of guidelines is then mapped routinely to non-slicing layout representations, which are later used to generate the floorplan for each tentative sizing solution. Furthermore, inductors are kept at consistent distances in all four directions during automatic placement, attempting to minimize not only the magnetic coupling to other inductors, but also, to the rest of the circuit.

Algorithm 2 Layout Generator & RF module generator

input: V**ariables** x
Netlist<**cell_list**, **netlist**> *N //parameterized netlist*
List<**template**> *T //set of template hierarchies that code placement guidelines*
Requirements<**List**<**f(*x*)**>, **List**<**g(*x*)**>> *R //set of objectives and constraints*
List<**Ind**<**S-Param** s-param**, GdsII** lay>> *IDS // inductor design space*
output: **GdsII** *GDSII*

1. *//Placer*
2. #define **List**<**Shape**> *bestLayout*:= none
3. #define **List**<**Cell**<**Shape**>> *library*
4. **for** each **cell** c_i in the **cell_list** of *N* **do**
5. *library*:= generate c_i using the RF module generator and the **variables** x_i **or** import the **gdsii** file of the **cell** and add it to the library
6. **for** each **template** hierachy t_i in *T* **do**
7. **List**<**shape**> *currentLayout*:= pack t_i hierarchy using the cells in *library*
8. **if** *currentLayout* dominates *bestLayout* in terms of *R* **do**
9. *bestLayout*:= *currentLayout*
10. *//Wiring Planner*
11. #define **List<Net<List<Wire<List<Node>>>>>** *Networks*
12. **for** each net_i in the **Netlist** *N* **do**
13. **List<Wire<terminal**$_a$, **terminal**$_b$>> *spanningTree*:= create the minimum area tree that connects all terminals of net_i in *bestLayout*
14. *Networks*<net_i<**List**<**Wire**>>>:= put the new *spanningTree*
15. **for** each **wire** *p* in the *NetworkGraph* of each net_i in the **Netlist** *n* **do**
16. **for** each **wire** *q* in the *NetworkGraph* of each net_j in the **Netlist** *n* **do**
17. with *p*!=*q* evaluate symmetry information from *bestLayout* and **if** a wiring symmetry heuristic matches for **wires** *p* and *q* **do**
18. **set wires** *p* and *q* as a symmetric pair
20. *//Single-net Global Router*
21. **for** each net_i in the **Netlist** *N* **do**
22. **List**<node> *grid*:= construct a multilayer multiport rectilinear grid
23. **for** each **wire** *p* in the *NetworkGraph* of net_i **do**
24. *Networks*<net_i<$wire_p$<**List**<**node**>>>:= assign symmetric path **or** put the shortest path from **terminal**$_a$ to **terminal**$_b$ of **wire** *p* using the path-finding algorithm A*
25. *//Multi-net Detailed Router*
26. **List**<**shape**> *DetailedRoutingPaths*:= use the evolutionary detailed optimization over *NetworksGraphs* and *bestLayout* to obtain a design-rule- and LVS-correct routing
27. **return** *bestLayout* and *DetailedRoutingPaths as* **GdsII** stream

B. Fully-automatic Router

While the placement is controlled by the circuit designer in a high-level fashion using the technology- and specification-independent template, all routing setup and execution is kept independent from placement. That is, as solutions vary in a multitude of different devices' sizes/shapes and performances, regardless of the template(s) and subsequent placement obtained, the Router presents a design-rule- and LVS-correct layout solution without additional effort for the designer. To accomplish this, a three-step Router is adopted.

1) Wiring Planner (lines 10-18 of Algorithm 2)

The first block parses the netlist of the RF block under optimization, and, together with the obtained floorplan, derives the wiring topology that connects all the terminals and provides the optimal terminal-to-terminal connectivity. The problem is formulated as: given a set of *t* terminals $\{T_1, T_2, \ldots, T_t\}$, construct the tree that is strongly-connected (i.e., all terminals are interconnected) and that minimizes the total wiring area of the tree given by:

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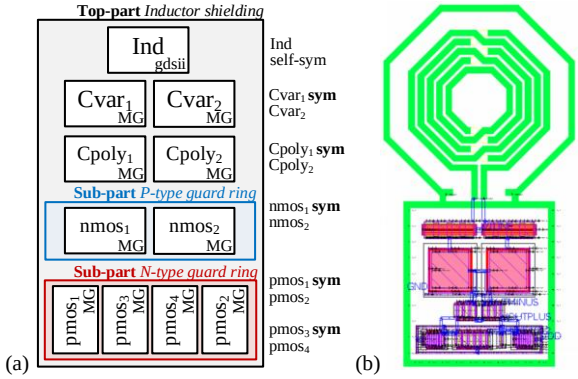

Fig. 6. (a) Graphical representation of the template hierarchy used for the layout generation. Devices are generated using the custom module generator or imported as a GDSII file (gdsii); (b) a possible layout after template-based Placer and single-net global Router.

$$\sum_{i=1}^{t}\sum_{j=1}^{t} l_{i,j} \times w_{i,j},\ i \neq j \tag{5}$$

where $l_{i,j}$ is the rectilinear distance between the two terminals and $w_{i,j}$ is the wire width. This problem is solved with the method proposed in [38]. When all wiring topologies are obtained, the symmetry information of the high-level floorplan guidelines is used to identify symmetries between terminal-to-terminal instances. Each terminal-to-terminal connection from each topology (i.e., each net) is tested with all other connections from the same and other topologies. Different heuristics can be used for wire symmetry pattern identification, as detailed in [39].

2) *Single-net Global Router (lines 20-24 of Algorithm 2)*

Each terminal of each cell may contain multiple electrically-equivalent locations where the connection can be made. Therefore, in the second block, each terminal-to-terminal connection is transformed into a rectilinear path where the ports that minimize the wire area, while implementing the detected symmetries, are selected from the multiple available ports of their corresponding terminals. To achieve this, first, a multilayer rectilinear grid for the problem is constructed, which consists of a directed graph considering 3-dimensional vertices and obstacles. Then, to select the best ports to be connected and the corresponding path, a variation of the A* path-finding algorithm [38] operating over the sparse non-uniform multilayer grid is taken. A possible layout solution for a given sizing after the single-net global Router is illustrated in Fig. 6(b).

3) *Multi-net Detailed Router (lines 26-27 of Algorithm 2)*

In the last step, routing paths are allowed to go off the global routing grid, while kept in the manufacturing grid of the technology process. Previously determined terminal-to-terminal connections, global routing solution, and symmetry information are used as the starting point for an optimization process. This optimization-based routing follows the principles introduced in [37], where an evolutionary algorithm performs slight structural and layer changes in the physical representation of a population of different and independent detailed routing solutions. This allows optimizing all wires of all nets simultaneously. The different routing solutions are evaluated by built-in algorithms that are basically lightweight design-rule- and LVS-check procedures, which provide the constraints at each generation of the optimization problem. Solutions should converge to feasible ones, i.e., feasibility is attained when no design rule or LVS rule is violated, while keeping the minimum wire length as objective. The adopted optimization kernel is a genetic algorithm, designed to solve the single-objective optimization problem:

$$\text{find } x \text{ that minimize } \sum_{i=1}^{N_{net}}\left[\sum_{j=1}^{n_i}\left(\sum_{k=1}^{K_j}\left(l_{ijk} \times w_{ijk} \times z_{ijk}\right)\right)\right] \tag{6}$$
$$\text{subject to } g_{\text{design - rule - error}}(x) = 0$$
$$\text{and } g_{\text{lvs - error}}(x) = 0$$

where, N_{net} is the number of nets, n_i the number of terminal-to-terminal instances in the net i, and K_j stands for the fixed number of rectilinear segments in wire j. Parameters l_{ijk} and w_{ijk} are the length and width, respectively, of the segment k of wire j of net i, and z_{ijk} the tabled cost of a given conductor (preferred conductors should be associated with the lower costs). The dimension of the design variables' space for a routing solution, x^d, can be computed with:

$$x^d = \sum_{i=1}^{N_{net}}\left[\sum_{j=1}^{n_i}\left(\sum_{k=1}^{K_j}\left(l_{ijk} + layer_{ijk}\right) + Src + Sink\right)\right] \tag{7}$$

with $layer_{ijk}$ being the index of a different available conductor, and, *Src* and *Sink* the different electrically-equivalent locations available within the start or end terminals, respectively, of a wire to establish the connection.

C. *Pre-Optimized Interconnect Widths*

While every layout designer agrees that routing should be minimized as much as possible, the selection of interconnect widths is usually performed by rules-of-thumb. These rules-of-thumb are technology-dependent and a lot of experimentation is still required to achieve the desired post-layout circuit performances. While increasing interconnect widths reduces the parasitic resistances, it also results in larger parasitic area capacitances as well as parasitic coupling between nets. Therefore, the determination of the interconnect widths (and the number of vias proportional to those widths) is a delicate tradeoff on RF circuit layout design. From the point of view of an automatic layout-aware sizing methodology, leaving the convergence of the process dependent of randomly selected wire widths may cause the optimization process to fail.

Table II presents the nominal performances of the VCO from Fig. 4 for a given sizing. Using the same floorplan, wiring planner and global Router, four different multi-net detailed routings were performed by varying the interconnect widths (and consequently the number of vias). The obtained layouts were extracted, the post-layout performances measured, and the results annotated on columns L1 to L4 of

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Table II. As observed, even though the floorplan and global routing solutions are the same for all cases, the post-layout performance figures of the VCO are extremely sensitive to the interconnect widths and the number of vias adopted.

TABLE II
VCO POST-LAYOUT PERFORMANCES FOR DIFFERENT INTERCONNECT WIDTHS VERSUS THE NOMINAL PERFORMANCE VALUES (0.35µm CMOS PROCESS)

Performances	Units	Nominal	Post-layout				
			L1[1]	L2[2]	L3[3]	L4[4]	Opt.[5]
f_{OSC}	GHz	2.485	2.478	2.459	2.451	2.423	2.449
PN@10KHz	dBc/Hz	-74.5	-62.7	-68.5	-69.5	-68.5	-72.6
PN@100KHz	dBc/Hz	-102.1	-91.6	-96.9	-97.6	-96.9	-100.5
PN@1MHz	dBc/Hz	-124.6	-116.3	-120.9	-121.3	-120.9	-123.6
PN@10MHz	dBc/Hz	-145.0	-137.2	-141.6	-142.0	-141.7	-144.1
P_{DC}	mW	19.22	18.93	18.99	18.96	18.96	18.93
Largest parasitic resistance (Ω)			8.58	5.79	5.70	4.23	5.79
Largest parasitic coupling cap. (fF)			1.73	3.13	4.65	7.08	2.25
Normalized Euclidean distance $f(x^w)$			207e-3	103e-3	89e-3	105e-3	38e-3

All nets assigned with: [1]the minimum width (from 0.5µm to 0.6µm) allowed by the technology process; [2]three times the minimum width; [3]five times the minimum width; [4]eight times the minimum width.
[5]Optimized case: **net name** [**multiplier width**] Vdd [5], Gnd [5], Vout+ [6], Vout- [5], IBp [4], net12 [5], netvar [6], Vtune [5].

To determine the optimal interconnect widths, a simulated-annealing algorithm [40] is here used to independently vary the width multiplier used within each net. In this optimization, each combination of design variables is evaluated by running the detailed routing, extracting the layouts in Calibre xRC®, and, using $c(x)$, the normalized Euclidean distance between pre- and post-layout relevant performances figures, as cost function:

$$c(x) = \sqrt{\sum_{i=1}^{Pf}\left(\frac{\left|pf_i^{\text{postlayout}}\right| - \left|pf_i^{\text{prelayout}}\right|}{\left|pf_i^{\text{prelayout}}\right|}\right)^2} \tag{8}$$

$$x^d = \sum_{i=1}^{N_{net}}\left[w_i\right], \quad w_i \in [1,10], v_i \propto w_i$$

where Pf are the number of relevant performance figures, i.e., oscillation frequency (f_{OSC}), phase noise (PN)@10KHz, PN@100KHz, PN@1MHz, PN@10MHz and power consumption (P_{DC}) for the current example. x^d computes the dimension of the design variables' space, i.e., multiplier width w_i for each net $\underline{i}$ and number of vias v_i proportional to w_i. The results obtained with this simulated-annealing optimization are shown in the last column of Table II, which balanced both the parasitic resistances and parasitic coupling capacitances for post-layout performance figures closer to the nominal values.

While this procedure is performed *a priori* for a representative sizing solution, the interconnect widths can still become outdated as the layout-aware flow evolves. In a future version of the proposed methodology, the objective is to incorporate this feature within the layout-aware optimization loop in a similar scheme to the one performed in [41], where placement templates were automatically generated on-the-fly.

V. EXPERIMENTAL RESULTS

In this section, the results obtained using the proposed methodology are presented. To show its potential, a widely used RF circuit block is considered for a 0.35-µm CMOS technology, namely a VCO. Note that all process-dependent simulations and extractions are carried out with off-the-shelf tools, therefore, the accuracy of the methodology itself is completely independent of the technology adopted. The use of the 0.35-µm CMOS technology is motivated by the fact that a reliable description of the technology process layer stack was available, allowing accurate EM simulations.

A. Optimization Setup

From the VCO topologies available, the cross-coupled double-differential topology with current biasing technique [3], whose schematic is illustrated in Fig. 7, is adopted. This type of LC VCO shows good phase noise performances as well as low power. The VCO is connected to output buffers to fix the output capacitance and ease the experimental measurement. Usually, the most important VCO performances are the oscillation frequency f_{OSC}, the phase noise (PN), the frequency tuning range f_{TUNE}, the power consumption P_{DC}, the output swing V_{OUT}, and, the circuit area, being the latter directly related to the manufacturing cost in IC technologies. Taking the previous aspects into consideration, the design variables and the optimization objectives and constraints are shown in Tables III and IV, respectively. This circuit operates at V_{dd} = 2.5V.

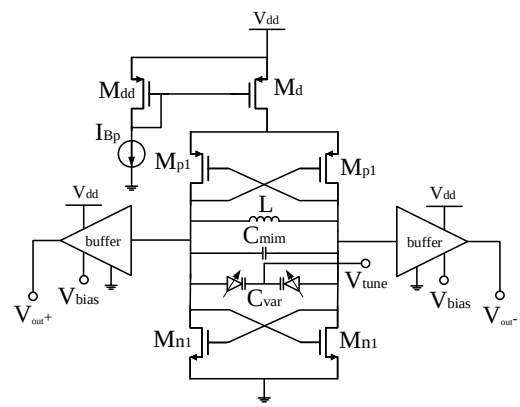

Fig. 7. Cross-coupled double-differential VCO schematic.

TABLE III
DESIGN VARIABLES AND RANGES

Variable	Units	Minimum	Grid	Maximum
$\mathbf{nf_{n1}}$	-	1	1	20
$\mathbf{nf_{p1}, nf_d, nf_{dd}}$	-	1	1	15
$\mathbf{w_{Cmim}}$	µm	9	1	29
$\mathbf{row_{Cvar}, col_{Cvar}}$	-	4	1	12
$\mathbf{I_{Bp}}$	mA	0.1	0.1	5
Inductor index	-	1	1	1000
Sizes fixed in the Process Design Kit				
$\mathbf{l_{n1}, l_{p1}, l_d, l_{dd}}$	µm	0.35		
$\mathbf{w_{n1}, w_{p1}, W_d, W_{dd}}$	µm	10		
$\mathbf{l_{Cvar}}$	µm	0.65		
$\mathbf{w_{Cvar}}$	µm	6.6		

The variables l_{n1}, w_{n1} and nf_{n1} are the length, width per finger and number of fingers of transistors M_{n1}; l_{p1}, w_{p1}, and nf_{p1} of transistors M_{p1}; l_d, w_d, and nf_d of transistor M_d; l_{dd}, w_{dd}, and nf_{dd} of transistor M_{dd}; row_{Cvar}, col_{Cvar}, w_{Cvar} and l_{Cvar} are the number of fingers per row, fingers per column, width per finger and length per finger of the varactors C_{var}; w_{Cmim} is the width and length of the MIM capacitor C_{mim}; Inductor index is used to explore the pre-optimized POF of inductors. It is not treated as a continuous design variable in the genetic operators, but instead, with the mapping strategy introduced in section III.B.

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TABLE IV
VCO SPECIFICATIONS: OBJECTIVES AND CONSTRAINTS

Specifications	Measure	Target	Units	Description
Objectives	PN@1MHz	minimize	dBc/Hz	Phase Noise @ 1MHz
	P_{DC}	minimize	mW	Power Consumption
	Area	minimize	mm^2	Layout Area
Constraints	*f*osc@0V V_{tune}	≥ 2.55	GHz	Oscillation frequency
	*f*osc@2.5V V_{tune}	≤ 2.45	GHz	Oscillation frequency
	PN@10KHz	< -65	dBc/Hz	Phase Noise @ 10KHz
	PN@100KHz	< -92	dBc/Hz	Phase Noise @ 100KHz
	PN@1MHz	< -113	dBc/Hz	Phase Noise @ 1MHz
	PN@10MHz	< -134	dBc/Hz	Phase Noise @ 10MHz
	Vout	≥ 0.15	V	Output swing
	P_{DC}	< 40	mW	Power Consumption

The inductor topology chosen for this circuit is the octagonal symmetric inductor with shielding, and the design variables of the inductor used to generate the POF are shown in Table V. This allowed obtaining the POF previously presented on Fig. 3(b), which sets the optimal IDS with 1,000 points for bottom-up synthesis.

TABLE V
DESIGN VARIABLES FOR THE POF GENERATION OF THE OCTAGONAL SYMMETRIC INDUCTOR WITH SHIELDING

n		D_{in} (µm)		*w* (µm)		*s* (µm)
Min-Max	**Grid**	**Min-Max**	**Grid**	**Min-Max**	**Grid**	**Fixed**
1–8	1	10–300	1	5–25	0.05	2.5

n – number of turns; D_{in} – inner diameter; *w* – conductor width; *s* – spacing between conductors.

B. Sizing Optimizations

To first study the need for a layout-aware flow, 10 runs of the sizing optimization for the proposed setup were performed. In these optimizations, only the sizing of the devices as well as the EM-characterized inductors were considered, but disregarding full parasitic extraction. It is important to note that the foundry models of the devices already contemplate layout parasitic estimations; therefore, the pre- to post-layout gap is already shortened. Each optimization was performed with a population of 256 individuals (solutions) for 200 generations from random initial solutions. Since no layout is available yet, the minimization of the device areas summation of the devices (including buffers and pads) is adopted instead of the real placement area. A summary of the results of these 10 runs is presented on Table VI, and the POF obtained in run_{VCOS2}, is illustrated on Fig. 8.

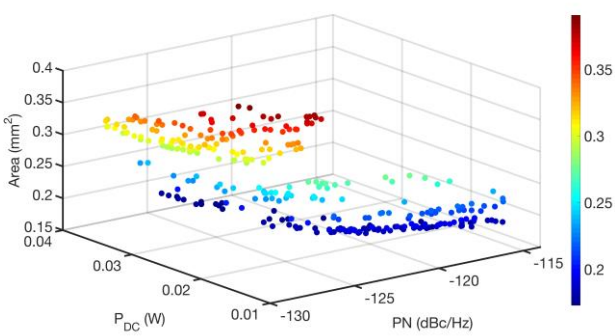

Fig. 8. VCO sizing optimization: Pareto front with the tradeoff area (mm^2) vs. PN@1MHz (dBc/Hz) vs. P_{DC} (W) of RUN_{VCOS2}.

C. Post-layout Simulation

After the solutions were obtained, the placement template hierarchy of Fig. 9 was defined by an experienced RF designer, capitalizing the provided expertise, e.g., aligned current/signal-flows, minimal wiring topology, mismatch, guard-rings, shielding, dummies, pad placement, etc. The layouts of the designs from the 10 previous runs (i.e., 2560 designs) were automatically generated with the procedures proposed in section IV.A and IV.B, with the interconnect widths pre-defined using the optimization method of section IV.C. Each automatically generated layout was extracted with Mentor Graphics' Calibre® and the full post-layout performances were simulated. From the original 2560 designs, in approximately 86% of the points the steady-state analysis failed convergence due to the presence of layout parasitic devices (in most cases, the extracted layout parasitics make the design stop oscillation and, hence, the simulator is unable to converge to the guessed oscillation frequency), while 11% actually got simulated but failed to meet at least one performance constraint post-layout, and only a small set verify all performance constraints, results also highlighted on Table VI.

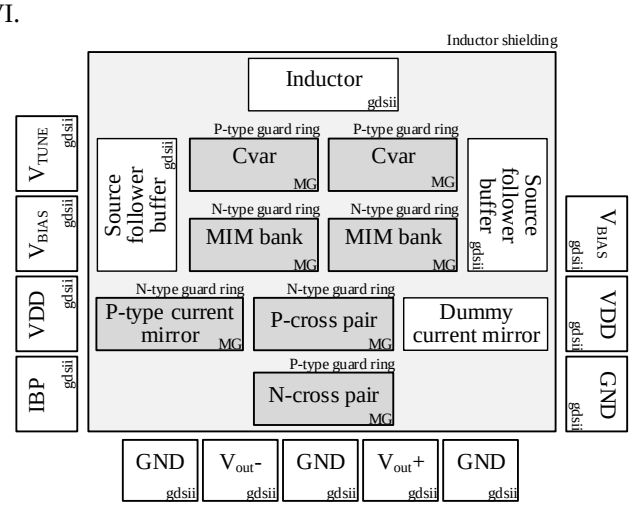

Fig. 9. Placement template hierarchy for the VCO. Shaded boxes refer to sub-partitions. Devices, blocks or sub-partitions are either generated using the custom module generator or imported as a GSDII file (gdsii).

Particularly for run_{VCOS2}, the post-layout front is illustrated on Fig. 10 and pre- and post-layout performances of some sample points of this front are presented in Table VII. As it is clearly observable, disregarding a full parasitic extraction from ready-to-fabricate layout prototypes leads to some of the performances being over-estimated in a pre-layout stage (e.g., P_{DC}), others being mostly under-estimated (e.g., PN, V_{OUT}), and, the oscillation frequency always deviating from pre-layout values. All of this is also allied to unrealistic layout area estimation. In the traditional flow, the layout of each design failing post-layout validation would be re-iterated manually until the impact of layout parasitics is negligible and all design specifications are fully met. However, this may not always be achievable as manually finding the culprit parasitics would be like finding a needle in the haystack of nets of a complex circuit. The layout of point S_2 (which refers to sizing-only optimization) is illustrated on Fig. 11(a).

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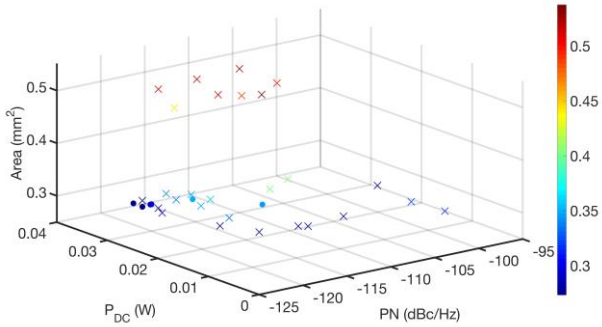


Fig. 10. Post-layout simulation of RUN_{VCOS2}. Post-layout feasible points are represented with circles (6 of 256) and unfeasible points (#fail) are represented with crosses (27 of 256). The steady-state analysis failed convergence (#n/c) in 223 points.

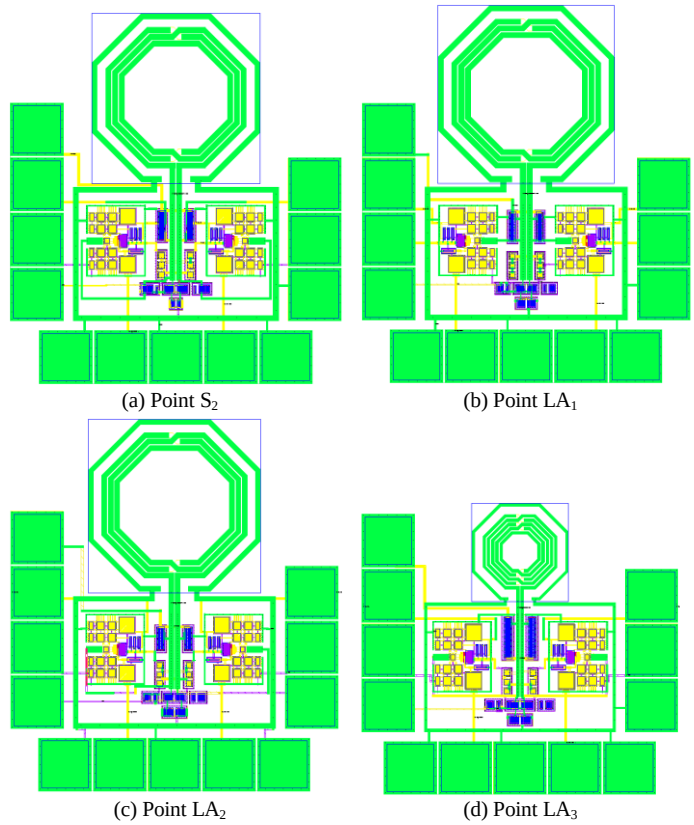
D. Layout-aware Optimizations

The previous results clearly justify the need for a layout-aware approach. Therefore, a batch of 10 runs of the layout-aware sizing optimization for the proposed setup were performed following the strategy presented in section III. In contrast to the runs from Table VI, all device and interconnect parasitics are fully accounted for. Each optimization was conducted with a population of 64 individuals for 50 generations, from random initial solutions. Each layout-aware point took on average 264 seconds to be evaluated on an Intel® Core™ i7-3770 @ 3.4GHz workstation with 32GB of RAM, including complete layout generation, extraction and simulation of the extracted netlist, which represents a significant overhead in terms of computational effort when comparing to the 7 seconds required on average for pre-layout simulation only.

A summary of the results of these 10 runs is presented on Table VIII, and, the POF obtained in run_{VCOLA4} shown in Fig. 12. In Table IX, a more detailed analysis of some sample points is presented, and, the corresponding device sizes of those solutions are in Table X. All the designs in these layout-aware POFs comply with the complete set of specifications, and therefore, are more trustworthy than the optimizations not considering full layout parasitics. Moreover, the inclusion of all required layout structures for manufacturing during optimization brings the designer closer to a first-pass fabrication success. The layout of points LA_1, LA_2 and LA_3 are illustrated in Figs. 11(b)-(d), and the point LA_4 in Fig. 13.

E. Comparison Against Electromagnetic Simulation

Even though all stages of the proposed methodology were built over established CAD tools for RF IC design, in this section an accuracy comparison is carried out between the proposed approach and the benchmark used in RF design, i.e., the EM simulation. To do so, the GDSII data from the layout point LA_4 was imported in ADS Momentum. An EM simulation was performed to consider all the parasitic components of the routing and circuit shielding. The S-parameters obtained from the EM simulation were then back-annotated in the netlist as a *Fblock* device, as performed for the back-annotation of inductors, and, the entire circuit simulated in Eldo RF®. The results of this simulation are shown in the last column of Table IX. Despite some minor differences between the measured post-layout performances resultant from the Calibre xRC® extraction and the EM simulation, it is possible to observe that the post-layout simulation is very similar to the EM-extracted simulation, endorsing, therefore, the proposed approach.



(a) Point S_2 (b) Point LA_1

(c) Point LA_2 (d) Point LA_3

Fig. 11. Automatically generated layouts. All layouts are placed at the same scale. Areas: (a) Point S_2, 0.348 mm^2; (b) Point LA_1, 0.357 mm^2; (c) Point LA_2, 0.351 mm^2; and, (d) Point LA_3, 0.273 mm^2.

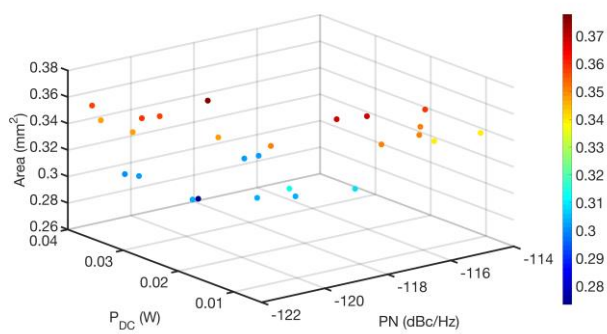


Fig. 12. VCO layout-aware optimization: Pareto front with the tradeoff circuit area (mm^2) vs. PN@1MHz (dBc/Hz) vs. P_{DC} (W) of RUN_{VCOLA4}.

As previously said, the EM simulation of the routing is a time-consuming process and a time-prohibitive solution to evaluate each candidate within the optimization process. In this example, the EM simulation of a single routing layout took approximately 71 hours for a setup of 700 frequency points and a mesh density of 30 cells/wavelength. An EM simulation with less frequency points and a wider mesh could be used to speed up the process, however, by using less frequency points the interpolation could no longer be passive and causal, and,

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TABLE VI
10 VCO SIZING OPTIMIZATIONS WITH EM-CHARACTERIZED INDUCTORS AND POST-LAYOUT VERIFICATION

#run	#feasible	minimum and maximum objective values of the POF						Post-layout[2]		
		Area [mm²][1]		PN@1MHz [dBc/Hz]		P_{DC} [mW]		#feasible	#fail[3]	#n/c[4]
		min	max	min	max	min	max			
run_{VCOS1}	256	0.1736	0.3809	-127.84	-115.41	12.771	37.524	6	23	228
run_{VCOS2}	256	0.1730	0.3908	-128.10	-114.76	12.598	39.835	6	27	223
run_{VCOS3}	256	0.1700	0.3909	-127.86	-114.90	12.766	39.490	5	29	222
run_{VCOS4}	256	0.1741	0.3926	-128.06	-114.96	12.720	36.903	6	19	231
run_{VCOS5}	256	0.1722	0.3819	-128.20	-114.88	12.674	39.973	3	36	217
run_{VCOS6}	256	0.1725	0.3518	-127.49	-114.75	12.496	39.771	17	30	209
run_{VCOS7}	256	0.1744	0.3876	-128.36	-114.91	12.611	39.973	6	41	209
run_{VCOS8}	256	0.1728	0.3826	-128.22	-114.81	12.545	39.952	9	25	222
run_{VCOS9}	256	0.1733	0.3803	-127.72	-115.02	12.630	39.566	8	35	213
run_{VCOS10}	256	0.1739	0.3756	-127.70	-114.94	12.927	37.182	11	22	223

area [mm²][1] the minimization of the device areas summation is used instead of the real placement area; **Post-layout[2]** layouts automatically generated using the methodology of section IV and extracted on Calibre xRC®; **#fail[3]** solutions that failed at least one constraint; **#n/c[4]** steady-state analysis not converged.

TABLE VII
PRE- AND POST-LAYOUT PERFORMANCE COMPARISON OF SAMPLE POINTS OF RUN_{VCOS2}

Specifications		Units	Point S_1		Point S_2[2]		Point S_3		Point S_4[3]	
			Netlist	Post-lay	Netlist	Post-lay	Netlist	Post-lay	Netlist	Post-lay
*f*osc@0V V_{tune}	≥ 2.55	GHz	2.556	**2.534**[‡]	2.596	2.572	2.666	2.629	2.636	2.606
*f*osc@2.5V V_{tune}	≤ 2.45	GHz	2.360	2.330	2.408	2.378	2.427	2.379	2.442	2.404
PN@10KHz	< -65	dBc/Hz	-75.61	-73.15	-76.30	-73.08	-72.26	-70.23	-73.76	-75.40
PN@100KHz	< -92	dBc/Hz	-102.50	-99.29	-103.20	-99.33	-97.76	**-90.94**[‡]	-100.80	-96.81
PN@1MHz	min < -113	dBc/Hz	-124.54	-120.90	-124.40	-121.02	-119.05	**-111.01**[‡]	-123.26	-116.98
PN@10MHz	< -134	dBc/Hz	-144.00	-141.10	-144.60	-141.20	-138.40	**-131.00**[‡]	-142.40	-137.00
P_{DC}	min < 50	mW	27.44	23.28	26.57	20.06	15.07	14.62	18.91	13.27
V_{OUT}	≥ 0.15	V	1.874	1.339	1.831	1.202	0.978	0.465	1.371	0.740
Area	min	mm²	0.2029	0.3005	0.2419	0.3483	0.1884	0.2803	0.2408	0.3472

[‡] performances that fail specifications post-layout; [2]Feasible point post-layout with smallest PN@1MHz; [3] Feasible point post-layout with smallest P_{DC};

TABLE VIII
10 VCO LAYOUT-AWARE OPTIMIZATIONS WITH EM-CHARACTERIZED INDUCTORS

#run	#feasible	minimum and maximum objective values of the POF					
		area [mm²]		PN@1MHz [dBc/Hz]		P_{DC} [mW]	
		min	max	min	max	min	max
run_{VCOLA1}	14	0.3375	0.5123	-121.18	-116.30	13.019	32.968
run_{VCOLA2}	20	0.2764	0.3541	-121.40	-115.37	12.807	36.293
run_{VCOLA3}	14	0.3028	0.3867	-121.53	-114.89	14.300	31.002
run_{VCOLA4}	26	0.2734	0.3778	-121.76	-114.17	8.089	36.987
run_{VCOLA5}	8	0.3416	0.3716	-121.27	-118.81	26.350	35.193
run_{VCOLA6}	25	0.4535	0.6038	-122.57	-115.76	11.475	31.529
run_{VCOLA7}	20	0.3367	0.3642	-121.66	-117.40	21.729	29.357
run_{VCOLA8}	34	0.2841	0.3843	-121.00	-114.41	15.030	37.160
run_{VCOLA9}	38	0.3608	0.6207	-122.29	-114.01	14.269	39.840
$run_{VCOLA10}$	28	0.3453	0.5770	-122.41	-115.55	7.697	32.303

therefore, no convergence is achieved during the circuit simulation. On the other hand, by reducing the number of cells/wavelength, the price to pay is accuracy degradation.

TABLE IX
CCDD VCO: PERFORMANCE COMPARISON OF SAMPLE POINTS OF RUN_{VCOLA4}

Specifications	Units	Point LA_1 Post-lay	Point LA_2 Post-lay	Point LA_3 Post-lay	Point LA_4 Post-lay	Point LA_4 EM[1]
*f*osc@0V V_{tune}	GHz	2.563	2.601	2.558	2.632	2.648
*f*osc@2.5V V_{tune}	GHz	2.398	2.433	2.272	2.347	2.373
PN@10KHz	dBc/Hz	-73.72	-69.42	-72.39	-73.50	-73.09
PN@100KHz	dBc/Hz	-100.00	-95.85	-97.58	-99.79	-100.28
PN@1MHz	dBc/Hz	-121.76	-117.65	-118.71	-121.50	-122.97
PN@10MHz	dBc/Hz	-142.00	-137.90	-138.80	-141.70	-142.45
P_{DC}	mW	36.99	8.090	35.19	28.35	27.34
V_{OUT}	V	1.424	0.870	1.070	1.373	1.639
Area	mm²	0.3571	0.3514	0.2734	0.3512	0.3512

EM[1] Performances with complete routing and shielding components extracted on ADS Momentum.

VI. CONCLUSION

Electronic design automation tools for reliable integrated passive devices design and with realistic circuit layout parasitic impact are mandatory to ease and speed up RF IC synthesis. This paper overviewed the major efforts proposed in the area in the last two decades, and took one step forward, by combining EM-characterized integrated inductors and full parasitic extraction from ready-to-fabricate layout prototypes during a sizing optimization. The target of this novel approach was not to drive RF designers away from their current workspace, but instead, to exploit the full capabilities of well-known and most established off-the-shelf CAD tools. Promising results over a widely used VCO were provided as a proof-of-concept, extensively validated, still, the applicability of the methodology to any other RF circuit class is straightforward. By completely exploring the ready-to-

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fabricate post-layout design space, design iterations can be successfully eliminated, bringing these RF circuit blocks closer to a first-pass fabrication success as every structure required for tape-out is considered and balanced during the optimization process.

TABLE X
DEVICE SIZES OF THE SAMPLE POINTS OF TABLE IX

Variable	Units	Point LA_1	Point LA_2	Point LA_3	Point LA_4
nf_{n1}	-	10	12	12	10
nf_{p1}, nf_d, nf_{dd}	-	11, 7, 2	11, 8, 3	14, 8, 3	10, 8, 1
w_{Cmim}	µm	10	10	10	9
row_{Cvar}, col_{Cvar}	-	5, 5	4, 6	7, 7	8, 8
I_{Bp}	mA	4.9	1.2	4.9	2.4
Inductor *n*	-	3	3	5	3
Inductor D_{in}	µm	201	198	63	185
Inductor *w*	µm	9.6	9.05	5.1	9.6

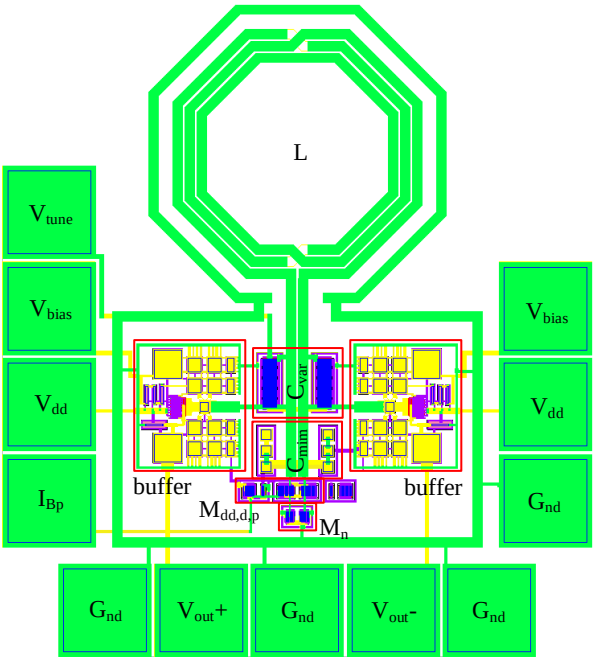

Fig. 13. Automatically generated layout of point LA_4, 0.3512 mm^2 area.

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