A 70\textmu m-Pitch 8\textmu W Self-Biased Charge-Integration Active Pixel for Digital Mammography

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Abstract—This paper presents a new low-power compact CMOS active pixel circuit specifically optimized for full-field digital mammography. The proposed digital pixel sensor (DPS) architecture includes self-bias capability at \pm 10\% accuracy, up to 15\textmu A of dark-current auto-calibration, built-in test mechanisms, selectable e\textsuperscript{-}/h\textsuperscript{+} collection, 10-bit lossless charge-integration A/D conversion, more than 1 decade of individual gain tuning for fixed pattern noise (FPN) cancellation, and a 50Mbps digital-only I/O interface. Experimental results for a 70\textmu m-pitch 8\textmu W DPS cell example are reported in 0.18\textmu m CMOS 1-polySi 6-metal technology.

Index Terms—CMOS, low-power, digital pixel sensor, DPS, imaging, X-ray, mammography.

I. INTRODUCTION

MAMMOGRAPHY has become a key tool for the diagnosis of breast cancer in women, and it is currently one of the recommended screening methods for its early detection [1]. In simple terms, a mammography machine is a low-dose X-ray imaging system adapted to the specific medical purpose depicted in Fig. 1(a). The radiology equipment includes the low-energy specific X-ray tube, positioned on top of or laterally to the breast, and the compressing device required to reduce tissue thickness and to prevent image blurring caused by the movement of the patient. On the opposite side of the breast, a sensing plate collects the X-ray particles in order to obtain the mammogram image. Over the last decade, full-field digital mammography has replaced the more classic screen-film technology as it has proven to be more efficient in terms of early cancer detection [2]. Other practical advantages of digital mammography are that it eliminates the requirement for film processing and scanning, and it enables real-time and remote evaluation of the images. Compared to classic mammography, the film plate is replaced in Fig. 1(a) by the X-ray sensing array of active pixels with practical pitch requirements in the range of 50\textmu m to 100\textmu m [3], [4]. In the case of direct conversion digital mammography, each digital pixel sensor (DPS) of the sensing array is built from the hybrid combination of the X-ray detector, which converts each incoming high-energy particle into electric charge, and the CMOS read-out circuit cell designed to collect this charge, either electrons or holes depending on the polarity of the common high-voltage bias, and to pre-process the resulting electrical signal. With respect to the X-ray detector, materials can range from low-cost Si to high-efficient CdTe compounds [5].

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Concerning the CMOS design techniques for the DPS, circuits reported in literature of other fields [6] lack the key functionalities required for X-ray mammography. In particular, the following features are usually not included in the DPS cell: dark current cancellation, biphasic current sensing for the collection of electrons (e\textsuperscript{-}) or holes (h\textsuperscript{+}), built-in test before and after the hybrid packaging, and cancellation of the fixed pattern noise (FPN) caused by the mismatching between pixels both at detector and circuit levels. Furthermore, these DPS designs are not optimized for the pulsed nature of the X-ray detector currents. In this sense, the few specific DPS circuits for X-ray imaging are based on photon-counting A/D conversion [7]–[13], so they tend to suffer from signal losses...
due to pile-up and charge-sharing between neighboring pixels. Finally, most of all these DPS architectures make extensive use of global analog biasing schemes, which are one of the main crosstalk sources between pixels in large sensing arrays.

This paper addresses all of the previous outlined issues by presenting a novel CMOS DPS circuit architecture specifically designed for digital mammography with self-bias capability, dark current auto-calibration, built-in test mechanisms, selectable $e^{-}/h^{+}$ collection, lossless charge-integration A/D conversion suitable for X-ray current patterns, and an individual pixel gain programming mechanism for FPN cancellation. The CMOS circuits proposed here exploit the subthreshold operation of the MOS transistor [14] together with the exhaustive circuit reuse inside the pixel in order to achieve a very low-power and compact DPS cell, respectively. This work is based on a preliminary proposal from the same authors [15] with improved pitch, power consumption and experimental results.

II. X-RAY PIXEL ARCHITECTURE

The functional model of the proposed DPS for digital mammography is shown in Fig. 1(b), where $V_{com}$ and $I_{sens}$ are the common high-voltage bias and the individual output current of the X-ray sensor, respectively, while $b_{in}$ and $b_{out}$ are the digital serial I/O ports of the DPS cell. The DPS can be operated in two different modes: acquisition and communication. In the acquisition mode, processing inside the active pixel starts with the auto-calibration of the input dark current ($I_{dark}$) in the absence of signal for its subsequent cancellation, as explained in Section IV. In addition, arbitrary test patterns ($I_{test}$) can be optionally added during acquisition following the procedure described in Section VI. The effective current signal:

$$I_{adc} = I_{sens} - I_{dark} + I_{test}$$

is then digitally quantified by the in-pixel charge-integration A/D converter (ADC) according to Section III. In the communication phase, the digital output of the ADC ($q_{adc}$) is serially read-out through $b_{out}$, while $b_{in}$ is used to program, at the same time and without any reduction in speed, the digital word ($q_{dac}$) to control the A/D conversion gain ($V_{th}$) individually for each pixel, as explained in Section V. This mechanism is incorporated in order to compensate for any gain FPN. Finally, all the analog references and biasing levels are locally generated inside the DPS as outlined in Section VII, so the connectivity to the rest of the sensing array is limited to digital signaling only.

III. INTEGRATING A/D CONVERSION

In order to achieve the A/D conversion inside the active pixel, the predictive architecture of Fig. 2 is selected and built from a pulse density modulator (PDM) in cascade with a digital low-pass filter.

The behavior of the proposed A/D conversion scheme is equivalent to a continuous-time first-order single-bit $\Delta \Sigma$ ADC [16] with the particularity of asynchronous operation. In this spike-counting scenario, the effective input signal in the current domain $I_{adc}$ is first integrated into $V_{int}$ and then quantified at 1-bit by the comparator according to the given threshold ($V_{th}$) and reference ($V_{ref}$) levels. The resulting asynchronous PDM pulses ($V_{pdm}$) are fed back to the reset mechanism of the analog integrator, which plays the role of a typical feedback D/A converter (DAC) used inside the $\Delta \Sigma$ loop in order to update signal prediction. As a result of the $\Delta \Sigma$ modulation, spectral noise shaping is obtained at the $V_{pdm}$ pulse stream, causing quantization errors to be pushed to high frequencies. Hence, a first-order low-pass digital filter is also included inside the pixel and implemented here by a simple lossy integrator (i.e. a counter with reset) controlled by the initialization signal ($b_{init}$). At the end of the acquisition time ($T_{acq}$), the digital output of the counter is found to be:

$$q_{adc} = \lfloor n_{adc} \rfloor \quad n_{adc} = \frac{T_{acq}}{T_{pdm}}$$

where $\lfloor x \rfloor$ stands for the base integer approximation of $x$ and $T_{pdm}$ is the PDM average period. In practice, the analog integrator of Fig. 2 is built around a capacitor ($C_{int}$), so in the ideal case:

$$n_{adcideal} = \frac{T_{acq}}{C_{int}V_{th}} I_{adc}$$

where $I_{dac}$ is the average input signal. Hence, the desired linear A/D conversion is achieved. The internal waveforms of this operation cycle are illustrated in Fig. 3(a).

Unfortunately, due to the low-power operation of both the analog integrator and the comparator blocks of each DPS cell, the $V_{pdm}$ pulse width in Fig. 3(a) cannot be null in practice. Hence, some time ($T_{res}$) is lost at each pulse generation in order to reset the analog integrator. As depicted in Fig. 3(b), this dead time causes a reduction of the PDM frequency according to:

$$n_{adcreal} = \frac{n_{adcideal}}{1 + \frac{T_{res}}{T_{acq}} n_{adcideal}}$$

In other words, the real ADC transfer curve exhibits a strong compression. This non-linear effect is particularly evident at full-scale of $I_{adc}$, where $T_{pdm}$ tends to be comparable to $T_{res}$, as illustrated in the case example of Fig. 4.

For a given unsigned integer digital output range $|q_{adc}| < 2^N$, the maximum compression error is reached at full-scale:
In order to ensure a peak deviation below half least significant bit (LSB):

$$T_{res} < \frac{T_{acq}}{2^{N}+1} \text{ for } 2^N \gg 1$$  \hspace{1cm} (6)

Using the example illustrated in Fig. 4, a reset time $T_{res} < 1ns$ should be ensured, forcing the PDM block to waste power. Furthermore, this dead time combined with the pulsed nature of the X-ray sensor current tends to introduce statistical noise far below the full-scale.

In order to overcome the reset time issues, the specific PDM topology of Fig. 5 is presented based on a previous piece of work from these authors [17]. The principle of operation is as follows: during initialization ($b_{init}$ high), the analog integrator is reset, while $C_{reset/CDS}$ remains connected to $V_{int}$; once in acquisition ($b_{init}$ low), the effective current $I_{adc}$ is integrated into $C_{int}$ while $C_{reset/CDS}$ is tracking the offset, the noise and the output signal itself of the first stage; finally, when the threshold $V_{th}$ is reached, the comparator generates a pulse ($V_{pdm}$ high), which is sent to the digital counter of Fig. 2 and it also causes $C_{reset/CDS}$ to be connected to the input of the analog integrator. Since $C_{reset/CDS}=C_{int}$, the charge accumulated in $C_{int}$ is compensated and the reset is completed. However, this novel strategy does not block the integration of $I_{adc}$ in $C_{int}$ during the reset time, as can be clearly seen in Fig. 3(c). Consequently, the PDM frequency is no longer dependent on the reset time and matches the ideal target of Fig. 3(a). In fact, a minimum reset time is required to ensure complete charge redistribution between $C_{reset/CDS}$ and $C_{int}$, but its particular value is no longer relevant. Furthermore, since $C_{reset/CDS}$ is continuously sampling the output of the analog integrator, it innerly implements a correlated double sampling (CDS) mechanism for the reduction of the low-frequency noise components at the output of this first stage.

In order to implement the PDM block, the compact CMOS circuit illustrated in Fig. 6 is proposed. The pulse modulator is mainly composed of the capacitive transimpedance amplifier (CTIA) M1-M4 and $C_{int}$, with the new reset scheme M5-M7 and $C_{reset/CDS}$, the comparator M8-M15, and a latch for generating the non-overlapping reset signals of the CTIA ($b_{res}$ and $\bar{b}_{res}$). In our X-ray context, the DPS must deal with positive (h$^+$) or negative (e$^-$) $I_{adc}$ values, depending on the selection control $b_{h/e}$. This programmability is implemented by the two switches M14-M15, which alternatively changes the sign of the comparator. Obviously, the comparison level $V_{ref} + (-1)^{b_{h/e}}V_{th}$ must be generated according to this selection, as explained in Section V.

IV. DARK CURRENT CANCELLATION

Following on from the approach outlined in Section II, auto-calibration of $I_{dark}$ is performed before each acquisition. For this purpose, the cancellation scheme of Fig. 7(a) is proposed based on current copiers. Basically, a dual NMOS (M1-M2) and PMOS (M3-M4) dynamic current mirror is introduced to compensate for positive and negative $I_{dark}$ values, according to the selection switches S1-S4. These current copiers store the equivalent dark current value in the analog memories $V_{dark1,2}$.
and are driven by the CTIA of the A/D converter itself through M5 and M6. In this way, a more compact and low-power DPS is obtained. Even more importantly, this mechanism also compensates for the effect of the input voltage offset of the CTIA during the A/D conversion.

However, two critical design points must be addressed in the dark current compensation scheme of Fig. 7(a): memory drift at $V_{dark1}$ (or $V_{dark2}$) for long acquisition times (e.g. $T_{acq}=1s$) due to the leakage current of S1 (or S2) in off state, and $I_{dark}$ offset errors caused by the charge injection at $V_{dark1}$ (or $V_{dark2}$) when opening the same switch S1 (or S2). In this regard, the CMOS circuit of Fig. 7(b) is proposed. The drift problem is solved by the the composite switching networks M9-M12 and M13-M16, which allow both a low leakage current for the off mode together with a fast settling time for the on state by changing the bulk bias of the main switch. Concerning charge injection issues, a two-step calibration procedure is implemented following Fig. 7(c): the dummy switch of the selected current mirror is not activated when changing this coarse mirror to its off state, so the systematic offset current generated by charge injection is stored in the dual current mirror, which activates its dummy switch, for the fine compensation. Hence, the final dark current error is a fraction of the coarse charge injection offset and not of the absolute $I_{dark}$ value.

V. INDIVIDUAL GAIN PROGRAMMABILITY

Again following the pixel architecture of Fig. 1(b), the remote programming mechanism of Fig. 8(a) is introduced in each DPS to compensate for pixel gain FPN. A switched-capacitor DAC is attached to the analog integrator of the PDM stage in order to control the threshold $V_{ref}$, which is equivalent to selecting different gain values for the in-pixel ADC according to (3).

The basic principle of operation is as follows: during DPS communication, and at the same time as $q_{dac}$ is read-out through the $b_{out}$ output of Fig. 1, the individual threshold code $q_{dac}$ is serially entered into each DPS through $b_{in}$ using the same daisy-chain pixel connectivity. Thanks to the charge redistribution between $C_{samp}$ and $C_{mem}$ controlled by the chronogram of Fig. 8(b), the desired threshold value is generated:

![Figure 6. CMOS circuit proposal for the PDM scheme of Fig. 5.](image)

![Figure 7. Proposed scheme (a), CMOS realization (b) and basic operation (c) for the in-pixel automatic dark current cancellation.](image)

![Figure 8. Proposed scheme (a) and operation (b) for the in-pixel gain FPN cancellation.](image)
$$V_{prog} = V_{DD} \sum_{i=0}^{B-1} \frac{q_{dac}(i)}{2^{2-i}} \quad \text{for} \quad C_{samp} = C_{mem} \quad (7)$$

where $B$ and $V_{DD}$ stand for the number of programming bits and the supply voltage, respectively. Once $V_{prog}$ is generated, the charge stored in $C_{mem}$ is transferred to $C_{int}$ using the same PDM CTIA of Fig. 5 and the polarity network controlled by $b_{h/e}$ through $\phi_2$ and $\phi_3$:

$$V_{int} = V_{ref} + (-1)^{b_{h/e}} V_{th} \quad (8)$$

$$V_{th} = \frac{C_{mem}}{C_{int}} V_{DD} \sum_{i=0}^{B-1} \frac{q_{dac}(i)}{2^{2-i}} \quad (9)$$

Hence, the absolute voltage level required in Fig. 6 is generated and copied into the MOS capacitor M1 for its storage during acquisition. Similar to the dark current cancellation proposal outlined in the previous section, the reuse of the CTIA block means important silicon area and power consumption savings per each active pixel. Even more importantly, the low output impedance of the CTIA allows a fast driving of the large M1 transistor, and it prevents charge redistribution errors at the passive DAC.

VI. BUILT-IN TEST

Due to the hybrid technology of the X-ray DPS illustrated in Fig. 1(a), a built-in mechanism for the test of the CMOS part before the expensive flip-chip process is mandatory to ensure the packaging of good dies only. Even after the hybrid packaging process is completed, injecting test signals at the individual input of each active pixel is beneficial as it can evaluate the yield of the array of X-ray sensors. For both purposes, the topology of Fig. 9(a) is proposed.

![Diagram](image)

Figure 9. Proposed scheme (a) and operation (b) for the pixel built-in test.

Basically, the switched capacitor $C_{mem}$ is operated during acquisition as a charge pump following the chronogram in Fig. 9(b). The equivalent DC test current injected at the input node is:

$$I_{test} = \frac{C_{mem}}{C_{int}} V_{test} \quad (10)$$

where $V_{test}$ is an external DC value common to all DPS cells. Since the proposed scheme is similar to the individual gain programming scheme of Fig. 8 and both functions cannot be selected at the same time, most of the devices of Fig. 9(a) are shared with the circuit referenced in Section V.

VII. LOCAL BIAS GENERATION

Last but not least, the CMOS circuit of Fig. 10 is incorporated inside each DPS to locally generate both the current biasing $I_{bias}$ and the voltage reference $V_{ref}$ levels required by all the blocks covered in previous sections. The operating principle of this circuit can be easily explained in three steps. Firstly, the circuit core M1-M4 operating in weak inversion saturation generates the proportional to absolute temperature (PTAT) voltage reference:

$$V_{bias} = U_t \ln P \quad (11)$$

where $U_t$ is the well known thermal potential. Secondly, $I_{bias}$ is obtained from the equivalent non-linear load M8-M9 attached to $V_{bias}$. Assuming strong inversion saturation and conduction for M8 and M9 devices, respectively, the resulting biasing current is proportional to the specific current ($I_S$):

$$I_{bias} = Q I_{S9} = Q 2n \beta U_t^2 \quad (12)$$

where $\beta$ and $n$ stand for the current factor and the sub-threshold slope, respectively, and $Q$ is a function of the scaling factors $M$, $N$ and $P$ [18]. Thirdly, $I_{bias}$ is driven to the active load M12, also operating in strong inversion saturation. As a result:

$$V_{ref} = 2n \sqrt{\frac{Q X}{Y}} U_t + V_{TO} \quad (13)$$

where $V_{TO}$ is the MOSFET threshold voltage. As $V_{TO}$ exhibits, in general, a negative coefficient with temperature [19], the final thermal compensation in $V_{ref}$ can be obtained through a suitable scaling between $Q$, $X$, and $Y$ in (13).

VIII. CMOS INTEGRATION

Based on the low-power and compact circuits proposed in the previous sections, a 70µm-pitch DPS CMOS cell is developed as the basic building block for sensing arrays in full-field digital X-ray mammography. The main design parameters are listed in Table I, while the resulting CMOS layout is shown in Fig. 11 for a 0.18µm 1-polySi 6-metal triple-well bulk CMOS technology. As can be seen from the pixel floorplan, more than half of the Silicon area is dominated by the analog and mixed blocks of the DPS. Concerning metal usage, the top metal structures are the metal-in-metal (MIM) capacitors for the analog integrator and the DAC blocks, the bump pad for the hybrid connection to the X-ray sensor, and the supply rails. Apart from the $V_{test}$ input that is used in test mode
only, all the I/O connectivity of the active pixel is restricted to the digital domain. In this sense, the 10-bit output word is complemented by an overflow flag.

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Value</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>$I_{\text{bias}}$</td>
<td>450</td>
<td>nA</td>
</tr>
<tr>
<td>$V_{\text{ref}}$</td>
<td>760</td>
<td>mV</td>
</tr>
<tr>
<td>$C_{\text{out}}$</td>
<td>85</td>
<td>fF</td>
</tr>
<tr>
<td>$C_{\text{reset/CDS}}$</td>
<td>85</td>
<td>fF</td>
</tr>
<tr>
<td>$C_{\text{mem}}$</td>
<td>85</td>
<td>fF</td>
</tr>
<tr>
<td>$C_{\text{samp}}$</td>
<td>85</td>
<td>fF</td>
</tr>
<tr>
<td>$V_{\text{th}}$</td>
<td>40 to 400</td>
<td>mV</td>
</tr>
<tr>
<td>$T_{\text{res}}$</td>
<td>$\sim 0.5$</td>
<td>$\mu$s</td>
</tr>
<tr>
<td>$N$</td>
<td>10</td>
<td>bit</td>
</tr>
</tbody>
</table>

In order to verify experimentally the proposed DPS CMOS circuit, a test chip is integrated as shown in Fig. 12. This integrated circuit contains several DPS cell replicas with specific experiments for the extraction of internal pixel performance parameters. In this regard, a custom current DAC is integrated in the same chip shown in Fig. 12 to digitally control the signal amplitude stimulated at the input of each pixel under test, which would be difficult to generate externally due to its low value (typ. pA to nA range). Finally, a tiny array of DPS cells is also included in the test chip for the exhaustive study of possible inter-pixel crosstalk effects.

**IX. EXPERIMENTAL RESULTS**

An exhaustive series of electrical tests have been performed on the integrated DPS circuits in Fig. 12, returning the results shown in Fig. 13 to Fig. 17 and summarized in Table II. All the graphical data presented here is for $h^+$ collection, although similar performance is obtained in case of selecting $e^-$ collection.

The first block to be verified based on the DPS scheme proposed in Fig. 1(b) is the core ADC itself, which is in charge of converting the effective input current signal $I_{\text{adc}}$ into the pixel output $q_{\text{adc}}$ already in the digital domain, as detailed in Section III. Fig. 13 shows an example of the ADC transfer function measured for a given pixel gain and set of acquisition window conditions. In all the programmed cases, the in-pixel ADC exhibits low compression losses compared to the classical behavior of Fig. 4, which will result in improved brightness linearity in the final digital mammography.

According to Fig. 2, brightness non-linearity at pixel level can occur due to two different phenomena: the overflow of the
digital counter, and the dead times at the PDM stage. While the former usually constrains the hard limit or saturation level of the pixel digital read-out, the latter is responsible for the gradual compression of the brightness scale. In order to test this second effect, the general expression (2) of the in-pixel ADC is presented here as:

\[ q_{adc} = \left\lfloor T_{acq} f_{pdm} \right\rfloor \]
\[ f_{pdm} = \frac{I_{adc}}{C_{int} V_{th}} \]  

(14)

where \( f_{pdm} \) stands for the PDM frequency at the output of the modulator of Fig. 2. From a simple review of (14), it is now clear that the linearity of the A/D conversion is dependent not only on the digital counter (\( q_{adc} \)) but also on the PDM stage itself (\( f_{pdm} \)). In this sense, and thanks to the new analog integrator scheme of Fig. 5, the experimental PDM transfer curves measured in the test chip show a remarkable linear response up to \( f_{pdm} \) values very close to \( 1/T_{res} \), similar to Fig. 14. From the mammography viewpoint, the linear response will minimize pixel brightness distortion under high-gain configurations (e.g. low-dose or high-speed applications).

With respect to the ADC gain, Fig. 15 shows more than one decade of programmability through the control of the threshold voltage of the PDM stage, as described in Section V. Experimental results also show a high level of consistency with the theoretical \( 1/V_{th} \) dependency from (14). This individual pixel brightness control range is wide enough to equalize by calibration the practical levels of gain FPN present in large size mammography panel sensors. Furthermore, this pixel-by-pixel gain digital tuning also opens the possibility of performing in-situ image preprocessing, such as highlighting a specific area without saturating the rest of the mammography image.

Additionally, with regard to the ADC block, the sensitivity of the overall pixel is obtained from the equivalent noise charge:

\[ ENC = C_{int} V_{intn} \]  

(15)

where \( V_{intn} \) is the integrated noise voltage at the output of the charge integrating amplifier in Fig. 6. Compared to classical topologies, it is important to note here that the inherent CDS mechanism supplied by the proposed reset scheme implements the following OpAmp noise transfer function in the discrete time \( Z \)-domain:

\[ \text{NTF}(Z) = 1 - Z^{-1} \]  

(16)

Hence, the low-frequency noise components generated by the OpAmp are attenuated before reaching the comparator by this differentiating NTZ. However, the corner frequency of the high-pass NTF is dependent on the input signal itself due to the asynchronous nature of the PDM stage of Fig. 5. In this sense, the ENC range reported in Table II is obtained from the circuit simulation of Fig. 6 under CMOS technology, acquisition window and signal corner cases.

Concerning the automatic dark current cancellation circuit
of Fig. 7, its performance in terms of residual offset is shown in Fig. 16 with DC error levels below 5% for $I_{\text{dark}}>1\text{nA}$. Hence, the proposed dark cancellation scheme is shown to be accurate enough to protect the pixel brightness dynamic range against the practical offset FPN of X-ray sensing planes. Moreover, this dynamic dark cancellation circuit can be operated for a wide range of $T_{\text{acq}}$ values in order to extend digital X-ray imaging from single shot mammography [20] to real-time video for stereotactic breast biopsy [21].

Figure 16. Experimental in-pixel offset cancellation results for DC (i.e. dark current) sensor input.

In terms of pixel built-in test, the experimental results of Fig. 17 show the digital read-out obtained under different injection input test amplitudes. The linearity of the equivalent test transfer curve validates the use of the circuit of Fig. 9 for the screening of the CMOS integrated imagers both before and after the expensive hybrid packaging with the corresponding X-ray sensor arrays.

Finally, crosstalk between the pixels of the tiny DPS matrix inside the test chip of Fig. 12 has been studied by stimulating the input of a given pixel at full-scale and observing the output of neighbor cells under no stimulus. No crosstalk has been recorded in any test case, proving the benefit of the in-pixel biasing generation of Fig. 10 combined with the digital-only pixel interface. From the application viewpoint, the absence of noticeable crosstalk between adjacent pixels strongly enhances image sharpness and contrast.

Figure 17. Experimental results of the in-pixel test capabilities for $T_{\text{test}}=7\mu\text{s}$, $V_{T_{\text{th}}}=265\text{mV}$ (gain programming code ‘00101000000’) and $T_{\text{acq}}=7.5\text{ms}$.

X. CONCLUSIONS
A new low-power and compact CMOS active pixel circuit specifically optimized for full-field digital mammography has been presented. The proposed DPS includes self-bias capability, dark-current auto-calibration, built-in test mechanisms, selectable e−/h+ collection, lossless charge-integration A/D conversion, individual gain tuning for FPN cancellation, and digital-only I/O interfacing. A 70$\mu$m-pitch 8$\mu$W DPS cell has been integrated and tested in standard 0.18$\mu$m CMOS 1-polySi 6-metal technology, returning good results in terms of linearity, noise, crosstalk and speed for its usage in X-ray imagers for digital mammography.

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