Direct fabrication of thin layer MoS_2 field-effect nanoscale transistors by oxidation scanning probe lithography

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Thin layer MoS_2-based field effect transistors (FET) are emerging candidates to fabricate very fast and sensitive devices. Here we demonstrate a method to fabricate very narrow transistor channel widths on a single layer MoS_2 flake connected to gold electrodes. Oxidation scanning probe lithography is applied to pattern insulating barriers on the flake. The process narrows the electron path to about 200 nm. The output and transfer characteristics of the fabricated FET show a behavior that is consistent with the minimum channel width of the device. The method relies on the direct and local chemical modification of MoS_2. The straightforward character and the lack of specific requirements envisage the controlled patterning of sub-100 nm electron channels in MoS_2 FETs.

Single layer MoS_2 is a relevant two-dimensional semiconductor material with the potential to fabricate novel electronic and optical devices[1-4]. Field effect transistors based on MoS_2 have been devised [5,6,7] and applied as label-free biosensors [8,9,10] or memory cells[11]. The integration of MoS_2 electronics will be enhanced by the development of direct patterning methods with the capability to generate nanoscale features on MoS_2.

The optimization of the MoS_2 nanoscale devices and the enhancement of their applications require the development of direct, reliable and easy-to use nanopatterning methods. The positioning capabilities and patterning resolution of scanning probe lithography (SPL) [12] make SPL a candidate to pattern MoS_2 flakes at the nanoscale level. Different SPL methods have been applied to pattern graphene-like and other carbon-based materials[13-16].

Oxidation scanning probe lithography (o-SPL) has been used to fabricate a variety of nanoscale devices on different materials such as nanowire FETs on silicon[17,18] , random access memories on gallium arsenide[19] , single photon detectors on niobium nitride[20] or quantum dots on graphene[21] .

We report the development of o-SPL to directly change the chemical composition of selected regions of a MoS_2 flake by applying a negative voltage pulse between the tip and the flake in the presence of ozone. The modification produces structures that protrude from the flake baseline. Those barriers effectively suppress the electron transport across them. The ability to control the size of the patterns is exploited to reduce the conduction channel of a MoS_2 monolayer field-effect transistor from microns to hundreds of nanometers. The output curves of the FET before and after o-SPL demonstrate that the electrons are channeled through a 200 nm constriction. It also shows that the o-SPL process does not degrade the electrical properties of the unmodified MoS_2 regions.

The MoS_2 layers were grown by means of chemical vapor deposition (CVD) on sapphire substrates based on the gas phase reaction of MoO_3 and sulfur at 700°C[22]. Single triangular domains of single layer MoS_2 are formed on the surface. Their orientation follows the underlying sapphire crystal structure. For the fabrication of field-effect transistors the material was transferred to a Si substrate covered with 270 nm thermally grown SiO_2 using the wet transfer KOH method and 950PMMA A2 as support polymer. After transferring PMMA is removed in acetone and residues are removed during annealing in Ar atmosphere at 350°C for 5 hours. Metallic contacts were defined by means of conventional electron beam lithography (EBL) followed by the deposition of 90 nm Au. Finally, contact annealing at 200°C in Ar atmosphere was performed to reduce contact resistance and eliminate resist residues.

The atomic force microscope (AFM) and the sample are kept in a closed chamber to control the relative humidity and the temperature during the oxidation process. The o-SPL is performed by operating the AFM in the amplitude modulation

mode[23] with a free amplitude in the 5-10 nm range and a set point amplitude/free amplitude ratio of about 0.9. We have used n+-doped silicon cantilevers (NCH-W, NanoWorld) with a force constant of about 40 N/m and a resonant frequency of about 300 kHz. The relative humidity is kept in 40-60 % range. Voltage pulses of 40-60 V and 0.5 ms were used. To enhance the oxidation of MoS_2, we have enriched the SPL chamber with ozone[24]. The ozone was generated by illuminating the chamber with ultraviolet light for 30 minutes. Figure 1 shows a scheme of o-SPL applied to pattern MoS_2 flakes. Figure 3(a) shows several MoS_2 flakes transferred on a SiO_2 layer 270 nm thick. They are contacted with gold pads by EBL[5].

The I-V curves were recorded before and after the lithography process to check the effect of the patterning on the device. The measurements were performed at room temperature in a probe station (Everbeing EB 06, Taiwan) with a semiconductor analyser (Keithley 4200).

Figure 2(a) shows several nanostructures fabricated by o-SPL. An array of dots and a line were fabricated with voltage pulse amplitude and duration, relative humidity and free amplitude of, respectively, 54 V and 250 μs, 45% and 5 nm. Figures 2(b) and 2(c) show, respectively, the AFM topographic image and cross section of one of the rows of dots represented in figure 2(a). The structures protrude 2-5 nm from the MoS_2 flake and the widths, given at full width at half maximum (FWHM), are between 40-50 nm (Fig.2(c)).

We propose that the application of high electric fields during o-SPL (about 10 V/nm) favors the formation of MoO_3. Rolandi *et al*[25] have applied o-SPL to transform selected regions of a molybdenum thin film into MoO_3. The stoichiometry of the formed oxide (MoO_3) was inferred because the patterns were soluble in water. In addition, Ross and Sussman[26] have described the reaction of MoS_2 surface in presence of water vapor and a temperature of 85 ^oC as:

$$2\boldsymbol{MoS}_2 + 9\boldsymbol{O}_2 + 4\boldsymbol{H}_2\boldsymbol{O} \rightarrow 2\boldsymbol{MoO}_3 + 4\boldsymbol{H}_2\boldsymbol{SO}_4 \qquad (1)$$

We propose that the electric field replaces the role of the temperature to facilitate the transformation of MoS_2 into MoO_3. In fact, the patterns fabricated on MoS_2 by o-SPL are readily etched in water which supports the formation of MoO_3 during the lithographic process.

The process to fabricate a 200 nm channel constriction on a thin layer MoS_2 FET starts from contacting a flake on SiO_2 layer with two gold microelectrodes (Fig. 3(a)). The optical image shows a flake derived from the coalescence of two triangular flakes bridging the electrodes. This system could already be operated as a FET having the silicon substrate as a third electrode (back gate) underneath the SiO_2. Oxidation SPL is used to decrease the width of the FET channel. For this we pattern two parallel lines running from source to drain gold electrodes. To avoid any damage in the Au electrodes, the patterning starts and ends about 100-200 nm from the Au electrodes. To direct the electron flow from the Au electrodes through the space defined by the oxide

lines we have also patterned a line running perpendicular to the oxide channel lines as it is shown in the AFM phase image (Fig. 3(b)). This line will act as a dielectric barrier to prevent the electron leakage outside the electron channel.

To illustrate the performance of the fabricated FET we have compared the output and transfer curves before and after (nano-FET) the patterning process. Those curves were acquired by using the same values of source-to-drain and gate voltages. The device is an *n*-channel transistor because the current increases with the positive gate voltage. The output and transfer curves before the o-SPL patterning are shown in Fig. 4 (panels a and b). From the transfer curve a subthreshold swing (SS) of 3.78 V/dec is obtained. The output and transfer characteristics of the nano-FET are depicted in Fig. 4c and 4d. The output curves show a reduction of the current of about one order of magnitude. In the linear regime of the output curves (V_g = 20 V and V_{ds} = 0.05 V) we obtain a current ratio between the original FET and the nano-FET of 12.4. This ratio is very close to the change in the ohmic resistance from the 2100 nm wide MoS_2 flake to the 200 nm wide channel constriction. We also observe that the saturation regime is reached at lower V_{ds} values in the nano-FET. The SS obtained from the transfer curve of the nano-FET is of 3.02 V/dec. This value is smaller than the one obtained before o-SPL. In any case those values are higher than the ones obtained by using thicker MoS_2 flakes[27]. The high SS values obtained here are attributed to the use of an ultra-thin MoS_2 flakes and the type of dielectric (SiO_2)[27].

In short, we have demonstrated an o-SPL method to fabricate thin layer MoS_2 field effect transistors with a channel width of 200 nm. Oxidation SPL is applied to define the transistor channel across the source and drain electrodes by patterning dielectric barriers on the thin layer MoS_2 flake. The decrease of the electron conductance in the nano-FET with respect to the precursor MoS_2 FET scales linearly with the channel width ratio. This lithography process is direct and does not require any specific sample preparation. In addition, the dielectric barrier width (30 nm) envisages the fabrication of MoS_2 field effect transistors with sub-100 nm channel widths.

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Figure Captions

Figure 1. (a) Scheme of the fabrication process of dielectric barriers on a MoS_2 flake by o-SPL. An ozone enriched atmosphere enhances the oxidation rate of the surface. (b) Scheme of the final device. The dielectric barriers define the electron channel.

Figure 2. (a) AFM topography image of some o-SPL nanostructures fabricated on a MoS_2 flake. (b) High resolution AFM topographic image of the array of o-SPL dots shown in (a). (c) AFM cross section along the line marked in (b).

Figure 3. (a). Optical image of several MoS_2 flakes deposited on a 270 nm thick SiO_2 layer. One of these flakes has been contacted with gold pads by electron beam lithography. (b) AFM phase image of a MoS_2 thin layer FET. The narrowest section of the channel is 200 nm wide. An additional dielectric barrier prevents the current flow outside the channel.

Figure 4. Output and transfer characteristics of a MoS_2 FET. (a) Output and (b) transfer curves before the fabrication of dielectric barriers by o-SPL. (c) Output and (d) transfer curves of the nano-FET after o-SPL. The current ratio observed between the thin layer FET and the nano FET corresponds to the change in the ohmic resistance given by the width ratio between the channel and the unmodified flake. The curves were taken at room temperature. The dashed lines in (b) and (d) represent the section where the SS values have been calculated.

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Figure 1

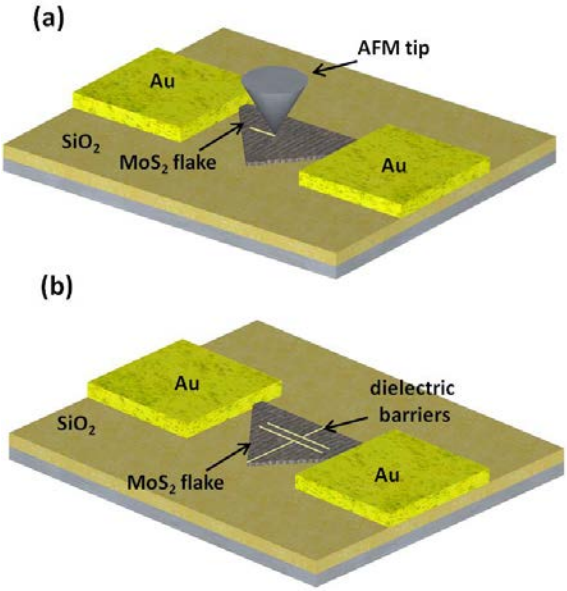

(a)
AFM tip
Au
SiO2
MoS2 flake
Au
(b)
Au
dielectric
barriers
SiO2
MoS2 flake
Au

Figure 2

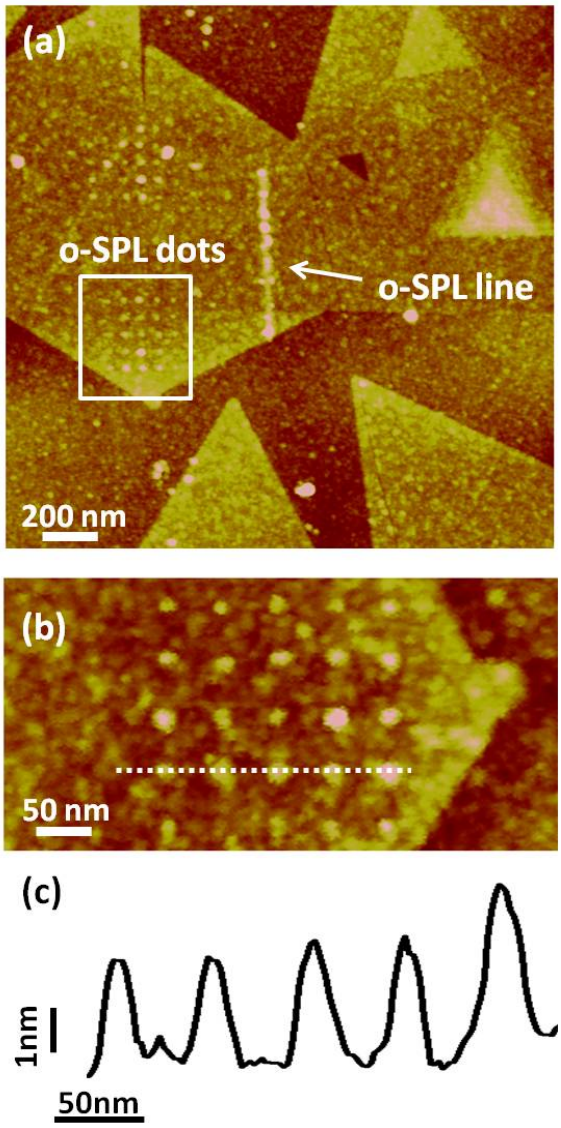


Figure 3

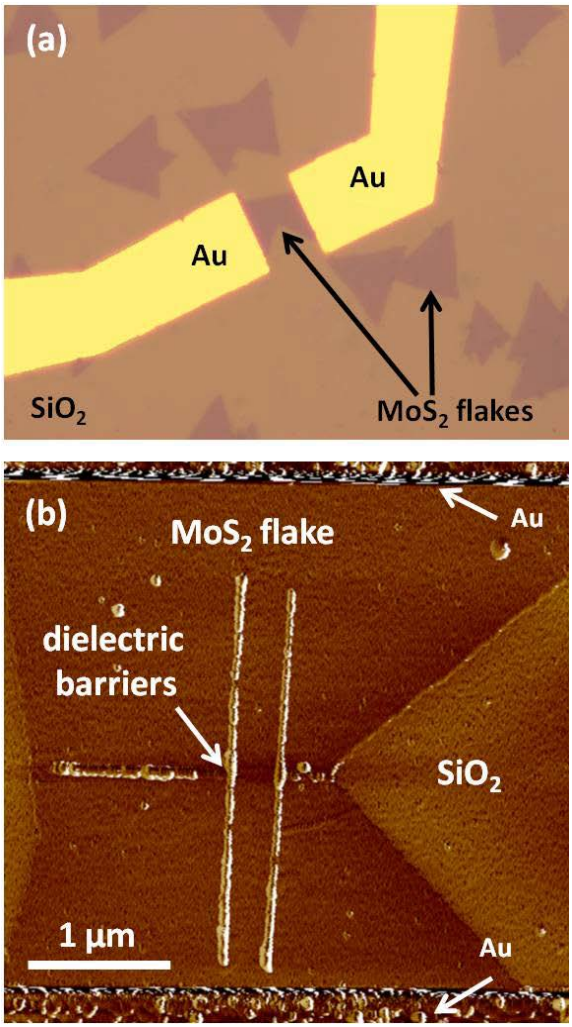
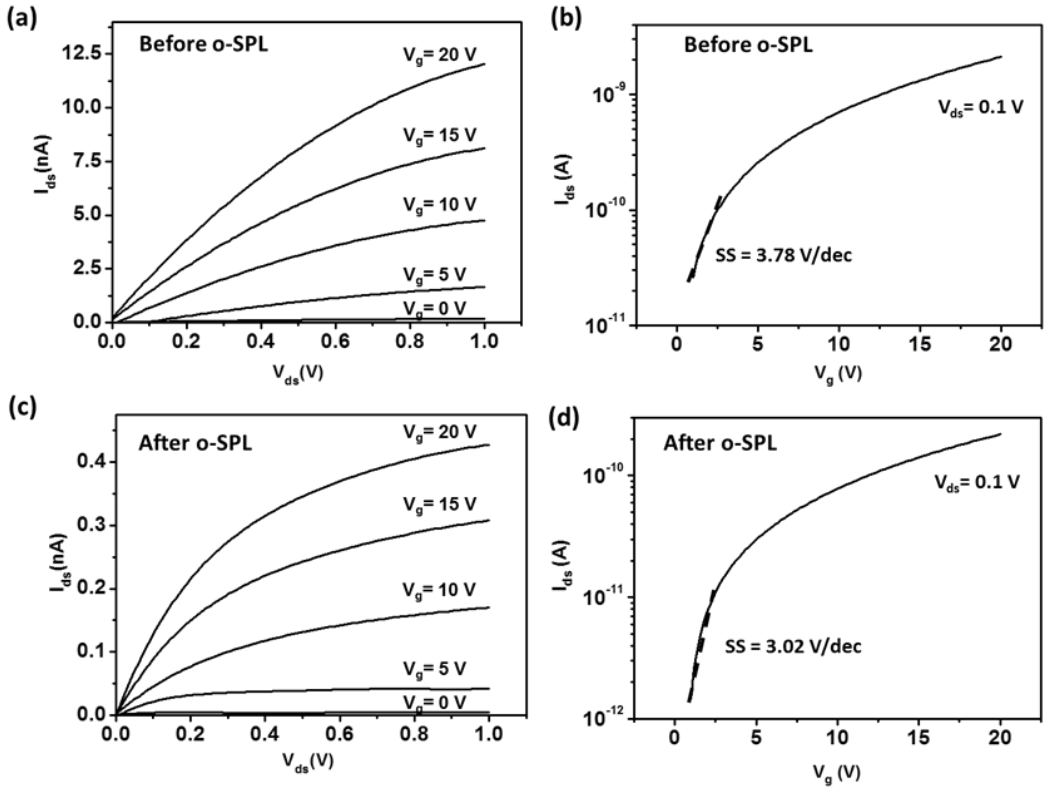

(a)
Au
Au
SiO2
MoS2 flakes
(b)
MoS2 flake
Au
dielectric
barriers
SiO2
1 µm
Au

Figure 4


(a)
Before o-SPL
V_g= 20 V
V_g= 15 V
V_g= 10 V
V_g= 5 V
V_g= 0 V
I_{ds} (nA)
V_{ds}(V)
(b)
Before o-SPL
V_{ds}= 0.1 V
SS = 3.78 V/dec
I_{ds} (A)
V_g (V)
(c)
After o-SPL
V_g= 20 V
V_g= 15 V
V_g= 10 V
V_g= 5 V
V_g= 0 V
I_{ds} (nA)
V_{ds}(V)
(d)
After o-SPL
V_{ds}= 0.1 V
SS = 3.02 V/dec
I_{ds} (A)
V_g (V)