UNIVERSITAT POLITÈCNICA DE CATALUNYA
BARCELONATECH

Departament d'Enginyeria Electrònica

LOW-POWER CMOS DIGITAL-PIXEL IMAGERS FOR HIGH-SPEED UNCOOLED PbSe IR APPLICATIONS

Josep Maria Margarit Taulé

A dissertation
submitted for the degree of

DOCTOR OF PHILOSOPHY BY THE
UNIVERSITAT POLITÈCNICA DE CATALUNYA,

under the PhD program in
ELECTRONIC ENGINEERING

November 2015

Revised

UNIVERSITAT POLITÈCNICA
DE CATALUNYA
BARCELONA**TECH**

INSTITUT DE MICROELECTRÒNICA DE BARCELONA
CSIC

Dr. Francesc Serra Graells, Associate Professor at the Microelectronics and Electronic Systems Department of *Universitat Autònoma de Barcelona*, Dr. Lluís Terés Terés, Tenured Scientist at *Consejo Superior de Investigaciones Científicas*, and Dr. Jordi Madrenas Boadas, Associate Professor at the Electronic Engineering Department of *Universitat Politècnica de Catalunya*,

Certify

that the dissertation “Low-Power CMOS Digital-Pixel Imagers for High-Speed Uncooled PbSe IR Applications” presented by Josep Maria Margarit Taulé in partial fulfillment of the requirements for the degree of Doctor of Philosophy in Electronic Engineering has been performed under their supervision at the Institute of Microelectronics of Barcelona belonging to the *Centro Nacional de Microelectrónica*, *Consejo Superior de Investigaciones Científicas*, and has been tutored at the Electronic Engineering Department of *Universitat Politècnica de Catalunya.*

Supervisors	Dr. Francesc Serra Graells	....
	Dr. Lluís Terés Terés	....
Tutor	Dr. Jordi Madrenas Boadas	....

......................., ...

In the loving memory of my brother, Pere,
and my grandparents Eulalia and Josep.

Abstract

This PhD dissertation describes the research and development of a new low-cost medium wavelength infrared (MWIR) monolithic imager technology for high-speed uncooled industrial applications. It takes the baton on the latest technological advances in the field of vapour phase deposition (VPD) PbSe-based MWIR detection accomplished by the industrial partner NIT S.L., adding fundamental knowledge on the investigation of novel VLSI analog and mixed-signal design techniques at circuit and system levels for the development of the readout integrated device attached to the detector.

The work supports on the hypothesis that, by the use of the preceding design techniques, current standard inexpensive CMOS technologies fulfill all operational requirements of the VPD PbSe detector in terms of connectivity, reliability, functionality and scalability to integrate the device. The resulting monolithic PbSe-CMOS camera must consume very low power, operate at kHz frequencies, exhibit good uniformity and fit the CMOS read-out active pixels in the compact pitch of the focal plane, all while addressing the particular characteristics of the MWIR detector: high dark-to-signal ratios, large input parasitic capacitance values and remarkable mismatching in PbSe integration.

In order to achieve these demands, this thesis proposes null inter-pixel crosstalk vision sensor architectures based on a digital-only focal plane array (FPA) of configurable pixel sensors. Each digital pixel sensor (DPS) cell is equipped with fast communication modules, self-biasing, offset cancellation, analog-to-digital converter (ADC) and fixed pattern noise (FPN) correction. In-pixel power consumption is minimized by the use of comprehensive MOSFET subthreshold operation.

The main aim is to potentiate the integration of PbSe-based infrared (IR)-image sensing technologies so as to widen its use, not only in distinct scenarios, but also at different stages of PbSe-CMOS integration maturity. For this purpose, we posit to investigate a comprehensive set of functional blocks distributed in two parallel approaches:

- **Frame-based "Smart" MWIR imaging** based on new DPS circuit topologies with gain and offset FPN correction capabilities. This research line exploits the detector pitch to offer fully-digital programmability at pixel level and complete functionality with input parasitic capacitance compensation and internal frame memory.

- **Frame-free "Compact"-pitch MWIR vision** based on a novel DPS lossless analog integrator and configurable temporal difference, combined with asynchronous communication protocols inside the focal plane. This strategy is conceived to allow extensive pitch compaction and readout speed increase by the suppression of in-pixel digital filtering, and the use of dynamic bandwidth allocation in each pixel of the FPA.

In order to make the electrical validation of first prototypes independent of the expensive PbSe deposition processes at wafer level, investigation is extended as well to the development of affordable sensor emulation strategies and integrated test platforms specifically oriented to image read-out integrated circuits. DPS cells, imagers and test chips have been fabricated and characterized in standard 0.15μm 1P6M, 0.35μm 2P4M and 2.5μm 2P1M CMOS technologies, all as part of research projects with industrial partnership.

The research has led to the first high-speed uncooled frame-based IR quantum imager monolithically fabricated in a standard VLSI CMOS technology, and has given rise to the Tachyon series [1], a new line of commercial IR cameras used in real-time industrial, environmental and transportation control systems. The frame-free architectures investigated in this work represent a firm step forward to push further pixel pitch and system bandwidth up to the limits imposed by the evolving PbSe detector in future generations of the device.

Acknowledgements

My first and foremost acknowledgments to **Paco Serra** and **Lluís Terés** for their incombustible guidance, moving enthusiasm and great patience. Thanks for believing in my work from the start to the very end, and giving me the opportunity to grow as a scientist and as a person in the IMB.

My next big thank you to the NIT people, **Carlos Fernández, Luis Gómez, Raúl Gutiérrez, Maria Teresa Montojo, Germán Vergara** and **Víctor Villamayor**. Your immediate feedback, exhaustive characterization and methodical debugging were invaluable throughout this work.

I am also grateful to all the previous, the current and the almost members of the ICAS team that helped me along this dissertation. Thanks to **Xavier Bullich, Álvaro Calleja, Adrià Conde, Michele Dei, Roger Durà, Roger Figueras, Aymen Jemni, Ricardo Martínez, Andreu Marzal, Sergio Morlans, Jofre Pallarès, Xavier Redondo, Justo Sabadell, Jordi Sacristán, Stepan Sutula, Fortià Vila, Francesc Vila** and **Pedro Zuccarello**, for the bright discussions, helpful suggestions and support. Thanks to **Josep Lorente** and **Joan Puertas** for their crash course in PCB design, and to **Enric Cabruja** and **Alberto Moreno** for making possible the flip-chip and the wire-bonding of the ICs. To **Albert Beltran, Sergi Peña** and **Jared Villanueva** my gratitude for their major, hard-working contributions to Matlab simulations, pixel design, and test, respectively. My appreciation also to **Jordi Madrenas** for his neat academic supervision as tutor at the UPC.

To **Tobi Delbruck** and **Shih-Chii Liu**, thanks for giving me the opportunity to visit the INI and to come back as a postdoc. I was immediately captivated by the warm and stimulating atmosphere of the Institute, and the humility and talent of its people. But amongst all, I learned A LOT. I am sure that was only the beginning of many fruitful collaborations between both centers. Thanks to **Raphael Berner** as well for his conclusive advice in the design of AER interfaces, and to **Mathias Bannwart**, for his master lessons on german, cooking, and friendship.

Gràcies a la familia i als amics! A la meva mare i la meva germana, ***les dues Roses****, i a* ***l'Andreu, el Dani, l'Ivan, la Neus, l'Oscar*** *i* ***el Xavi*** *per les incontables paraules de suport, ànims i mostres d'afecte que m'heu regalat. I gràcies als meus nebots* ***Carla, Roger*** *i* ***Pau*** *per robar-me sempre un somriure.*

Because I would not have succeeded without your intellectual and emotional support, there is a bit of every one of you in this thesis.

THANK YOU!!

Contents

1 Introduction **1**

1.1 Seeing Beyond the Visible 1

1.1.1 Vision Cameras 1

1.1.2 Seizing the Red End 3

1.2 Common Metrics and Figures of Merit 7

1.3 IR Direct Detectors 12

1.3.1 Thermal and Photonic Transduction 12

1.3.2 IR Detection Today 14

1.4 Uncooled PbSe Photoconductive Technology 16

1.4.1 Detection Basis 16

1.4.2 Device Performance 19

1.4.3 Electrical Model 22

1.5 CMOS IR Imagers 24

1.5.1 Readout Techniques 24

1.5.2 FPA Architectures 27

1.5.3 State-of-the-Art IR Vision Sensors 30

1.6 Objectives and Scope 31

1.6.1 Motivation 31

1.6.2 R&D Context 34

1.6.3 Working Hypothesis 36

1.6.4 The Challenges 37

1.6.5 Methodology and Contents 39

2 Frame-Based Smart IR Imagers **43**

2.1 Imager Architecture and Operation Proposal 43

2.2 All-Digital Program-In and Read-Out Interface 47

2.2.1 Motivation and Design Proposal 47

2.2.2 Compact CMOS Implementation 50

2.3 Input Signal Conditioning 54

2.3.1 Motivation and Design Proposal 54

2.3.2 Compact CMOS Implementation 54

2.4 Asynchronous ADC with CDS 63

2.4.1 Motivation and Design Proposal 63

2.4.2 Compact CMOS Implementation 67

2.5 Individual Gain Tuning 76

2.5.1 Motivation and Design Proposal 76

2.5.2 Compact CMOS Implementation 78

2.6 Local Bias Generation 80

2.6.1 Motivation and Design Proposal 80
2.6.2 Compact CMOS Implementation 82

3 Frame-Free Compact-Pitch IR Imagers 85
3.1 Imager Architecture and Operation Proposal 85
3.2 Event-Driven Communications 86
3.2.1 Motivation and Design Proposal 86
3.2.2 In-pixel compact CMOS Implementation 92
3.3 Self-Biasing and Temporal-Difference Filtering 95
3.3.1 Motivation and Design Proposal 95
3.3.2 Compact CMOS Implementation 97
3.4 Digital Contrast Tuning 103
3.4.1 Motivation and Design Proposal 103
3.4.2 Compact CMOS Implementation 104
3.5 Reset-Insensitive Spike-Counting ADC 106
3.5.1 Motivation and Design Proposal 106
3.5.2 Compact CMOS Implementation 111
3.6 Fair AE Arbitration 113
3.6.1 Motivation and Design Proposal 113
3.6.2 Compact CMOS Implementation 115

4 Pixel Test Chips in 0.35μm and 0.15μm CMOS Technologies 119
4.1 A 100μm-Pitch Smart Pixel with Offset Auto-Calibration and Gain Programming 120
4.1.1 Full-Custom ASIC Design 122

4.1.2 Experimental Results 127

4.2 A 200μm and 130μm-pitch Smart Pixel with Full Programmability 137

4.2.1 Full-Custom ASIC Designs 139

4.2.2 Experimental Results 143

4.3 A Self-Biased 45μm-Pitch AER Pixel with Temporal Difference Filtering 151

4.3.1 Full-Custom ASIC Design 151

4.3.2 Experimental Results 155

5 Imager Test Chips in 2.5μm, 0.35μm and 0.15μm CMOS Technologies 159

5.1 A Low-Cost 32×32 Integrated Test Platform for Electrical Characterization of Imagers 159

5.1.1 Full-Custom ASIC Design 166

5.1.2 Experimental Results 171

5.2 An 80×80 Sub-1μW/pix 2kfps Smart MWIR Imager 175

5.2.1 Monolithic PbSe-CMOS Integration 176

5.2.2 Experimental Results 180

5.3 A 32×32 Frame-Free Compact-Pitch MWIR Imager 189

5.3.1 Full-Custom ASIC Design 190

5.3.2 Experimental Results 191

5.4 Comparison with State-of-the-Art IR Imagers 195

6 Conclusions 199

6.1 Contributions 199

6.2 Discussion and Future Work 205

List of Figures

1.1 General view of a staring-FPA photonic CMOS imager. Optical sensors may be integrated in the same Si substrate, post-processed on top of the CMOS dice or hybridized with the ROIC. Drawing not in scale. 4

1.2 Electromagnetic spectrum (a); Visible bands (b); IR bands and absorption notches (c). Adapted from [9]. 5

1.3 Example of glass container quality inspection using visible (a) and MWIR-radiation (b) sensitive cameras [16]. 6

1.4 Typical spectral response of main IR thermal and photon detectors at 295K room temperature (gray and red, respectively), and photon detectors at 77K cryogenic temperature (blue). Background illumination is assumed to be at a temperature of 300K [20]. 15

1.5 Simplified layout (a) and cross-section (b) of the MWIR VPD PbSe detector after being post-processed on top of its CMOS wafer. 18

1.6 Experimental response of the integrated VPD PbSe photoconductor at 300K in terms of MWIR spectral detectivity (a) and modulation bandwidth (b). 19

1.7 Experimental output capacitance versus pixel size (a); dark resistance versus bias potential for several pixel pitch values (b) of the VPD PbSe photoconductor. 20

1.8 Experimental noise of the VPD PbSe photoconductor versus bias potential at 330Hz, for several pixel pitch values. 21

1.9 Experimental noise margins of the VPD PbSe photoconductor for a fixed pitch of 40μm and an applied bias potential of 1V. 21

1.10 VPD PbSe detector circuit equivalent (a) and schematic view (b). 23

1.11 Common readout input circuit schemes: SFD (a), DI and buffering (dashed amplifier) (b), GMI (c) and CTIA (d). . . . 26

1.12 Classic chip-level external (a) and internal (b) ADC readout architectures. Dashed lines indicate variable circuit location: S/H, CDS and buffering can be moved outside the FPA in order to lessen pixel dimensions. 28

1.13 Typical column-level (a) and pixel-level (b) ADC readout architectures. Dashed lines indicate variable circuit location: S/H, CDS, buffering and digital integration can be moved outside the FPA in order to compact pixel pitch. 29

1.14 Full-custom ASIC EDA design flow used in this work. 42

2.1 Frame-based IR imager proposal. Practical examples of raw imaging under no FPN compensation (a) and in-pixel FPN-corrected aquisition (b). General DPS architecture (c). Figure not in scale. 45

2.2 Frame-based Smart IR imager operation. General DPS architecture (a) and operational chronogram (b). 46

2.3 General scheme of a 15-bit LFSR reconfigurable counter with MLS feedback polynomial for the digital I/O interface of Fig. 2.1. When low, control signal `count` fixes the module to behave as a shift register. 48

2.4 Reconfigurable digital I/O interface scheme proposal for the DPS of Fig. 2.1(a). Internal configuration for communication (b) and acquisition (c). 49

2.5 Full-scale transitions (black) and additional transistors (red) in reconfigurable ripple (solid line) and PRMLS (dashed line) counters. Values for 7 to 15-bit design cases. 50

2.6 Reconfigurable basic building block of the LFSR-based I/O interface with overflow detection (a). CMOS implementation of each bit register, with external initialization of type reset (b) and set (c). 52

2.7 Reconfigurable basic building block of the ripple-counter based I/O interface with overflow detection (a). CMOS implementation of each bit register (b) and signal multiplexing for T-like functionality (c). 53

2.8 Linear model of the DPS input stage proposal with dark current cancellation (a) and input capacitance compensation (b) for the frame-based Smart imager of Fig. 2.1. 55

2.9 DPS parasitic capacitance compensation circuit (a) and detailed CMOS implementation for Fig. 2.8(b). 56

2.10 DPS offset cancellation schemes: analog self-calibration (a) and digital external tuning (b). 58

2.11 CMOS circuit implementation of the DPS offset self-calibration scheme of Fig. 2.10 with simple (a) and regulated (b) cascode toppologies. 58

2.12 DPS input stage offset cancellation with external tuning for Fig. 2.10(b): CMOS DAC implementation in voltage (a) and current (b). Non-overlapping clock circuit and chronogram used in both schemes (c). Black filling in transmission gates indicates side includes a dummy device. All signals are active high. 60

2.13 General scheme of a first-order PDM predictive ADC (a) and adaptation to frame-based DPS cells (b). 65

2.14 Classical scheme (a) and single-capacitor integration/CDS proposal (b) for the PDM part of the in-pixel integrate-and-fire ADC ($I_{eff} > 0$ case) of Fig. 2.13. 66

2.15 DPS CMOS implementation of the analog integrator (a) in Fig. 2.14(b) and operation in reset (b) and acquisition (c) phases. 69

2.16 DPS CMOS comparator implementation as part of the PDM modulator of Fig. 2.14(b). 69

2.17 Complete asynchronous ADC signal path of frame-based DPS cells during acquisition phase. Input charge integrating scheme including noise sources (a) and equivalent small-signal noise model (b). 70

2.18 General scheme of the individual gain tuning proposal for the in-pixel PDM ADC of Fig. 2.14(b). 78

2.19 CMOS DAC implementation of the DPS individual gain tuning circuit for frame-based imagers reusing the SC-DAC of Fig. 2.12 (a). Non-overlapping clock circuit and operational chronogram (b). Black filling in transmission gates indicates side includes a dummy device. All signals are active high. . . 79

2.20 PTAT reference architecture proposal for the local bias generation in frame-based DPS of Fig 2.1. 81

2.21 CMOS implementation of the DPS PTAT local bias generator based on the log companding architecture of Fig. 2.20. 82

3.1 Frame-free Compact-pitch IR imager proposal. Practical examples of raw (a) and low-pass filtered output imaging (b). General DPS architecture (c). Figure not in scale. 87

3.2 r_{amax} vs. N_{evfs} from 32 to 2048-pixel binary FPA sizes and $N_{out} = 32$ pads. Direct readout (solid line) and column encoding (dashed line). 91

3.3 Row-addressed parallel column-readout block diagram for the M×N MWIR imager of Fig. 3.1 (a) and in-pixel signaling detail (b). 93

3.4 CMOS implementation of the in-pixel AER communication interface depicted in Fig. 3.3: high-speed state-holding comparator (a), pull-up handshaking circuit (b) and operation for $I_{eff} < 0$ (c). Small MOSFET symbols correspond to minimum size devices. Chronogram not in scale. 94

3.5 General scheme of the self-biasing and TD filtering proposal for the frame-free Compact-pitch imager of Fig. 3.1. 96

3.6 Simplified CMOS schematic of the proposed circuit for DPS self-biasing and TD filtering of Fig. 3.5 (a). GD (b) and SD (c) implementations for the non-linear resistor R_{bias}. 98

3.7 Simplified small-signal model of the log-domain filtering circuit of Fig. 3.6(a). 100

3.8 PLL-based proposal for the dynamical tuning of the log-domain filter in the frame-free Compact-pitch imager of Fig. 3.1. 104

3.9 Simplified CMOS schematic (a) and operation (b) for the PLL-based tuning of the log-domain low-pass filter used in Fig. 3.8. 105

3.10 Proposed lossless-reset integrate-and-fire ADC architectures and comparative performance: hard-fixed charge subtraction (a), and differential (b) and absolute (c) OpAmp-charged subtraction. Window detection part common to all three schemes (d). 108

3.11 Integrate-and-fire operation according to the ideal (a), classical (b) and proposed (c) reset schemes ($I_{eff} > 0$ case) of Fig. 3.10. In this example, classical operation losses the charge equivalent to 1 spike compared to ideal behavior. Figure not in scale. 109

3.12 Event request frequency dependency on reset time as described in (3.36). Values normalized to an expected maximum request frequency value $f_{req4\sigma} = \overline{f_{req}} + 4\sigma(f_{req})$. 110

3.13 CMOS implementation of the lossless-reset integrate-and-fire ADC of Fig. 3.10(c) (a) and overintegration-guarding circuit (b). 112

3.14 Binary arbiter tree and distributed row encoding proposal for the frame-free Compact-picth medium wavelength IR (MWIR) vision architecture of Fig. 3.1. 114

3.15 Comparative chronogram showing event acknowledgement between alternative arbitration strategies: fixed priority [132] (a), collision-only priority toggling [133] (b) and last-attended priority toggling (this work, c). Top arrows indicate event collision, double arrows causality in priority switching. 115

3.16 CMOS implementation of the basic row-encoder (a) and arbiter (b) cells, and the programmable pull-down NAND gate used in the design of the latter (c). 117

4.1 General architecture of the DPS-S100 cell (a) and detail of simplified CMOS PDM implementation (b). 121

4.2 Operational chronogram of the DPS-S100 cell for the frame-based Smart imager of Fig. 4.1. 123

4.3 General recommendations for CMOS device matching. Reprinted with permission from [95]. 125

4.4 Physical CMOS layout of the DPS-S100 for frame-based Smart imagers. Metal-4 power-line routing (a); metal-3 routing of control signals and main block allocation (b). 126

4.5 Basic scheme of the IR detector emulation circuit employed in the characterization of Smart DPS cells (a) and stimulus distribution in the mini-FPA (b). 128

4.6 Experimental sensitivity (a) and absolute current levels (b) of the NMOS detector emulator included in test chips (dashed lines indicate process corners). Micrograph of the test chip fabricated to characterize 100μm-pitch frame-based Smart digital pixel sensor (DPS-S100) cells (c). 129

4.7 Simplified scheme of the electrical testbench deployed for the electrical characterization of DPS-S cells (a). Read-out captures (b) and Labview interface front panel (c). 130

4.8 Transfer memory (a) and I_{dark} memory retention (b) characterization protocols for frame-based Smart digital pixel sensor (DPS-S) cells. 133

4.9 Experimental measurements of I_{dark} memory retention in DPS-S100 cells of Fig. 4.6(c) (a), and illustration of possible sources (b), for $I_{dark} = 1\mu$A and $I_{eff} = 0.5\mu$A. 134

4.10 Examples of experimental transfer functions for different gain control values over a DPS-S100 cell of Fig. 4.6(c), for $I_{dark} = 1\mu$A. 135

4.11 General architecture of the DPS-S200 (a) and the DPS-S130 (b). 138

4.12 Operational chronogram of DPS-S200 and DPS-S130 cells for frame-based Smart imagers. 140

4.13 Standard operating routine of DPS-S200 and DPS-S130 cells for frame-based Smart imagers. 141

4.14 Physical CMOS layout of the DPS-S200 cell for frame-based Smart imagers. External interconnections (a) and main block allocation (b). 142

4.15 Physical CMOS layout of the DPS-S130 cell for frame-based Smart imagers. Metal-4 power-line routing (a); metal-3 routing of control signals and main block allocation (b). 144

4.16 Micrograph of the test chip fabricated to characterize DPS-S200 (a) and DPS-S130 (b) cells. 145

4.17 Experimental transfer curve of the DPS-S200 (a,b) and the DPS-S130 cells (c,d) for different individual offset (top) and gain (bottom) digital tuning codes, respectively. 146

4.18 Experimental range of I_{dark} (a,c) and V_{th} memory leakage rates (b,d) inside the DPS-S200 and the DPS-S130 cells, respectively, in terms of digital output error when only the other parameter is refreshed. 147

4.19 Experimental offset (a,c) and gain (b,d) deviations between 480 DPS-S200 and 105 DPS-S130 cells for the digital tuning codes I_{dark} = '`1000000000`' and V_{th} = '`1000000000`'. 149

4.20 Proposed architecture for the DPS-C45 cell. 152

4.21 CMOS layout of the DPS-C45 cell. Metal usage and I/O pin location in the AER pixel (a) and main block allocation (b). . 154

4.22 Physical CMOS layout of the test cell for the internal characterization of the DPS-C45. 155

4.23 Experimental measurements vs. process reported leakage values for the CMOS technology adopted in the design of the DPS-C45. 156

4.24 Simulated log-domain high-pass filtering at room temperature (a) and critical effects of high-leakage devices on the functionality of the PLL (b) and TD (c) blocks of the DPS-C45 of Fig. 4.21. 157

5.1 Functional (a) and physical (b) description of the ITP concept.161

5.2 ITP architecture (a) and pixel cell with and row and column controls (b). 162

5.3 Examples of digital image synthesis using the proposed ITP for real life scenes (a) and regular patterns (b,c) using 16-level DACs. Image size is 32×32. 163

5.4 Analytical (black) versus typical (green) and corner (red) electrical simulations of the ITP pixel current for $I_{cx} = 1\mu$A (a) and $I_{ry} = 1\mu$A (b). Supply voltage is +5V 165

5.5 Pixel cell (a) and physical CMOS layout (b) of the ITP chip. Pixel bounding box is 50μm×50μm. Bump pad window diameter is 20μm. 167

5.6 General chronogram for the digital programming of the ITP of Fig. 5.5(b). Fully parallelized case. 168

5.7 Microscope photograph of the ITP, pinout and core array map. 170

5.8 Phantom IUT chip (a) attached by flip-chip to the ITP chip (b). IUT die size is 3.5mm×3.5mm (12.3mm^2). 170

5.9 Electrical characterization testbench used for the ITP chip of Fig. 5.8(b) and the IUT chip of Fig. 5.27 171

5.10 FPGA configuration employed to evaluate the ITP chip of Fig. 5.8(b) and the IUT chip of Fig. 5.27. 172

5.11 Measured ITP pixel current curves versus digital row (a) and column (b) programming for $I_{bkgd} = 0$ and $I_{fs} = 1\mu$A. 173

5.12 Example of dynamic programming at 12.5Mbps (a) and generated current at 10kfps (b) of an ITP pixel (3,3) for $I_{bkgd} = 0.8\mu$A and $I_{fs} = 1\mu$A. 174

5.13 Basic operation flow of the Smart IR imager. 175

5.14 Example of clock tree distribution for a 32×32-pixel Smart MWIR imager, following the same distribution that 80×80 FPAs. `BU8`, `BU4` and `BU2` stand for 8, 4 and 2mA digital buffers, respectively. 177

5.15 Microscope photograph of the VPD PbSe post-processed wafer with sapphire protection (a), FPA detail with (bottom-right) and without (top-left) Au and PbSe deposited on top (b), and pixel detail before post-processing (c). 178

5.16 Micrograph of the Smart MWIR imager fabricated in 0.35μm 2P4M CMOS technology with VPD PbSe post-processing. The ROIC is directly wire bonded to chip-carrier PCB for 64-pin LCC-like sockets. 179

5.17 Electrooptical validation setup used for imager screening at wafer level. Experimental results were obtained utilizing the same blackbody and NI-PXI measurement system. 180

5.18 Experimental offset (a) and gain (b) tuning curves of 24 DPS cells distributed over the 80×80-pixel FPA. Operating conditions are no IR illumination and $\mathtt{d_{gain}}$ = 226LSB (a), and calibrated $\mathtt{d_{offset}}$ to achieve $\mathtt{d_{out}}$ = 512LSB at $\mathtt{d_{gain}}$ = 226LSB (b). Results averaged over 150 frames from the same FPA with $\bar{\sigma}_{\bar{\mathtt{d}}_{\mathtt{out}}}$ = 4LSB. 182

5.19 Experimental deviations of offset cancellation codes (a) and gain programming slope values (b) of the 6400 DPS cells of the entire FPA of Fig. 5.16. 183

5.20 Measured image and read-out dispersion before (a) and after (b) in-pixel FPN equalization. 184

5.21 Measured image pixel-to-pixel (red), row-to-row (blue) and column-to-column (green) FPN versus incoming IR irradiance before and after in-pixel FPN equalization. 186

5.22 Average saturated-pixel read-out values over imager focal plane versus incoming IR irradiance before (red) and after (blue) in-pixel equalization. Offset is calibrated at 480LSB read-out in order to reach saturation. 186

5.23 Experimental NETD statistics at 773K (a) and 1173K (b) blackbody temperatures. Noise measurements are averaged for each one of the 49 imagers of an entire wafer. 187

5.24 Measured imager speed performance with mechanical chopper (a) and practical lighter switch-on sequence example (b). 188

5.25 Sample photograms of hot round plate (a) and flame (b) captured at 1650fps. 188

5.26 Proposed architecture for the frame-free Compact-pitch MWIR imager. 190

5.27 Micrograph of the 32×32 frame-free DPS-C45 IUT test chip tracing the location of main blocks and the I/O bumping pads that conform the pinout bridge (a). Pixel detail (b) and Cu-UBM zoom-in with height profile (c). Bounding box including scribe-line is about 2.6mm×2.6mm (6.8mm^2). . . . 192

5.28 Micrograph of the complete test SIP integrated for the electrical validation of the frame-free Compact-pitch imager of Fig. 5.27 (a), and detail of the SnAg bumps grown in the ITP side at wafer level (b). 193

5.29 General scheme of the experimental setup defined for the electrical validation of the frame-free Compact-pitch imager architecture of Chapter 3. 194

List of Tables

1.1 Overview of IR detector types and materials. 14

1.2 Performance and cost comparison between leading IR detection technologies. *Depending on temperature and detection mode (i.e. PV or PC). 17

1.3 Typical parameters of the VPD PbSe photoconductor. 20

1.4 Performance comparison between state-of-the-art IR vision sensors. 32

3.1 Truth table of the arbitration unit depicted in Fig. 3.16. * means current state. 116

4.1 Operational specifications of the industrial DPS prototypes for frame-based Smart imagers. 120

4.2 I/O diagram of the initial DPS-S100 cell for frame-based Smart imagers ((P)ower, (D)igital, (I)nput, (O)utput) of Fig. 4.1.122

4.3 Design parameters of the initial DPS-S100 cell for frame-based Smart imagers of Fig. 4.1. 124

4.4 Summary of experimental results for the DPS-S100 cells of Fig. 4.6(c). 136

4.5 Measured performance of the initial DPS-S100 for frame-based Smart imagers 136

4.6 I/O diagram of DPS-S200 and DPS-S130 cells for frame-based Smart imagers (P)ower, (D)igital, (I)nput, (O)utput). . 139

4.7 Design parameters of both the DPS-S200 and the DPS-S130 pixels for frame-based Smart imagers of Fig. 4.15 and Fig. 4.14.143

4.8 Measured performance of the DPS-S200 and DPS-S130 cells for frame-based Smart imagers. 150

4.9 Operational specs of the DPS-C45 prototype for frame-free Compact-pitch imagers. 151

4.10 I/O diagram of the DPS-C45 cell for frame-free Compact-pitch imagers ((P)ower, (D)igital, (I)nput, (O)utput). 153

5.1 Full list of the ITP pin-out for (P)ower, (A)nalog and (D)igital types and (I)nput and (O)utput directions. The physical location of each pin and the row/column origin are defined in Fig. 5.7. 169

5.2 Performance summary of the ITP device of Fig. 5.8(b). . . . 174

5.3 Full list of the frame-free IUT pin-out for (P)ower, (A)anlog and (D)igital types and (I)nput and (O)utput directions. The physical location of each pin and the row/column origin is defined in Fig. 5.27. 191

5.4 Performance comparison between this work and state-of-the-art IR vision sensors. 197

List of Acronyms

AC	alternating current	100
AE	adressed event	88
AER	address event representation	85
ADC	analog-to-digital converter	24
AGC	automatic gain control	76
ALOHA	additive links on-line Hawaii area	113
APS	active pixel sensor	2
ASIC	application specific integrated circuit	31
BDI	buffered direct injection	24
BGMI	buffered gate modulation input	24
BLIP	background-limited infrared performance	8
BW	bandwidth	85
CBD	chemical bath deposition	16
CCD	charge-coupled device	2
CCO	current-controlled oscillator	103

CDS	correlated double sampling	27
CMOS	complementary metal-oxide-semiconductor	1
CNM25	2.5μm 2-polySi 1-metal CMOS CNM Technology	163
CP	charge pump	103
CTIA	capacitive transimpedance amplifier	24
DAC	digital-to-analog converter	50
DC	direct current	12
DI	direct injection	24
DFM	design for manufacturability	168
DPS	digital pixel sensor	24
DPS-C	frame-free Compact-pitch digital pixel sensor	119
DPS-C45	45μm-pitch frame-free Compact-pitch digital pixel sensor	151
DPS-S	frame-based Smart digital pixel sensor	119
DPS-S100	100μm-pitch frame-based Smart digital pixel sensor	120
DPS-S130	130μm-pitch frame-based Smart digital pixel sensor	137
DPS-S200	200μm-pitch frame-based Smart digital pixel sensor	137
EDA	electronic design automation	39
EKV	Enz-Krummenacher-Vittoz	55
ELIN	externally-linear internally-nonlinear	95
QE	quantum efficiency	7
DR	dynamic range	7
ESD	electrostatic discharge	168
FF	fill factor	7
FPA	focal plane array	1
FPGA	field-programmable gate array	171
FPN	fixed pattern noise	9
FOM	figure of merit	7
GD	gate-driven	97

GMI	gate modulation input	24
GPIB	general purpose interface bus	127
HMI	human-machine interface	172
IC	integrated circuit	38
ITP	integrated test platform	153
IUT	imager under test	160
IR	infrared	1
LCC	leadless chip carrier	177
LCD	liquid crystal display	205
LFSR	linear-feedback shift register	47
LSB	least significant bit	50
LUT	look-up table	48
LVS	layout versus schematic	39
LWIR	long wavelength IR	5
MEMS	micro-electro-mechanical systems	3
MIM	metal-insulator-metal	153
MLS	maximum-length sequence	47
MOS	metal-oxide semiconductor	49
MOSFET	metal-oxide-semiconductor field-effect transistor	25
MPW	multi-project wafer	175
MSB	most significant bit	50
MWIR	medium wavelength IR	5
NEP	noise equivalent power	10
NIR	near infrared	5
NTF	noise transfer function	72
NETD	noise equivalent temperature difference	11
NMOS	n-channel metal-oxide-semiconductor	56
PC	photoconductive	13

PCB	printed circuit board	34
PDK	process design kit	40
PE	photoemissive	13
PIP	polysilicon-insulator-polysilicon	153
PRMLS	pseudo-random maximum length sequence	49
PV	photovoltaic	13
PVT	process, voltage, temperature	37
OA	operational amplifier	25
ODE	ordinary differential equation	95
PC	photoconductive	13
PCB	printed circuit board	34
PDM	pulse density modulation	30
PFD	phase-frequency detector	103
PLL	phase-locked loop	103
PM	pulse modulation	30
PMOS	p-channel metal-oxide-semiconductor	25
PSD	power spectral density	19
PTAT	proportional to absolute temperature	80
PV	photovoltaic	13
PVT	process, voltage and temperature	37
PWM	pulse width modulation	30
QWIP	quantum well IR photodetector	13
RMS	root mean square	8
ROI	region of interest	76
ROIC	read-out integrated circuit	2
SBDI	share-buffered direct injection	24
SC	switched-capacitor	62
SCI	switched-current integrator	24

SD	source-driven	97
SDRAM	synchronous dynamic random access memory	172
SFD	source follower per detector	24
SI	switched current	57
SIP	system-in-package	190
SNR	signal to noise ratio	8
STF	signal transfer function	72
SWIR	short wavelength IR	5
TD	temporal difference	95
TFS	time-to-first spike	88
TV	television	205
UBM	under bump metallization	190
USB	universal serial bus	172
VCO	voltage-controlled oscillator	103
VLSI	very-large-scale integration	2
VPD	vapour phase deposition	1

Introduction | 1

Infrared (IR) thermal imaging is an emerging technology with promising industrial, scientific and medical applications. The recent introduction of uncooled photonic sensors based on vapour phase deposition (VPD) PbSe technologies [2] opens the door to a new generation of high-speed and low-cost IR vision devices made of monolithic active focal plane arrays (FPAs). This thesis investigates novel complementary metal-oxide-semiconductor (CMOS) circuit design techniques and fully-digital configurable-readout architectures specially conceived to operate these detectors. In this context, the present chapter introduces the motivation, background and trends of current thermography systems, and highlights the main aims of the work.

1.1 Seeing Beyond the Visible

1.1.1 Vision Cameras

Vision, widely acknowledged as our foremost human sense, is a highly regarded resource to perceive and interact with the world that surrounds us. It is not by chance that numerous expressions like “to watch out”, “to look after" or "to foresee" populate the English language and have equivalent examples in many other human cultures. But what does it mean to see something? When we are looking at a scene, our eyes capture electromagnetic radiation and convert it to electrical signals depending on the color, brightness and contrast of the image received. Visual information is then processed and interpreted in our brains as shape and motion, and used to identify objects so as to facilitate a proper behavior for survival. Guided by chance and curiosity, and attracted by the opportunity to spot distant places and times out of one's natural sight, many thinkers have contributed to apply imaging principles to the development of human-made vision sensors. It all started with the observation of the pinhole effect [3] and the creation of the camera obscura back in the fifth century B.C. [4], and continued with the invention of the first permanent photographic cameras by Niépce [5] and Daguerre [6] in the nineteenth century. These two initial discoveries triggered off 200 years of frame-based imaging revolution.

The high degree of maturity reached today by Silicon-based semiconductor technologies has bloomed into the high-resolution and portable digital cameras we can find in stores. Contemporary imagers are made of very-large-scale integration (VLSI) microelectronic devices. They include millions of transistors, placed in extremely reduced areas and capable to process millions of data per second at a very competitive price. The present generation of digital cameras is dominated by CMOS image sensors that, as predicted by [7], have been progressively gaining market share where their older charge-coupled device (CCD) relatives have lost. Prevailing are staring FPA architectures as depicted in Fig. 1.1, whose pixelated photonic detectors are monolithically or hybridly joined to an array of CMOS read-out circuit cells. Every one of the resulting individual sensors that compose the focal plane is called an active pixel sensor (APS). Such CMOS read-out integrated circuit (ROIC) implementations are typically preferred because they offer:

- Reduced technological costs, if last generation of sub-micron CMOS processes are not required.
- Direct integration of mixed analog-digital circuits in the same Silicon substrate.

- Compatibility with micro-electro-mechanical systems (MEMS) structures and devices, increasing performance and reducing the cost of the complete camera integration.
- Large scalability, leading integration trends in the sector of consumer electronics [8].

Most of these devices are only sensitive to a reduced part of the electromagnetic spectrum: visible and near IR light, and provide affordable artificial vision with a spectral response slightly beyond human eye's reach. But this tendency is steadily changing. Current demand for significant strategic, industrial, scientific and medical equipment is pushing these capabilities into the deep IR range.

1.1.2 Seizing the Red End

Discovered by Sir William Herschel in 1800, IR radiation refers to that located just above the red end of visible spectrum. Most of the thermal radiation emitted by objects at room temperature is in the IR range, generated or absorbed by molecules at the transition between their rotational-vibrational movements. Extending the detectable electromagnetic spectrum towards IR implies remarkable functionality gains due to both, the aforesaid capability of matter to self emit at this wavelength range and the energy information obtained from the observed materials. The former allows to see in poor lightning scenarios such as dusty and cloudy environments, or those with no external light sources like the Sun or the Moon; the latter offers valuable information, not apparent under regular visible radiation, that facilitates thermal and chemical identification. Hot objects, people and animals glare in pitch-black darkness, distant planets and stars can be examined in their early stellar days, and weaknesses are revealed in structures.

Much of the IR emission spectrum is unusable for detection systems because radiation is absorbed by water or carbon dioxide in the atmosphere. There are several wavelength bands, however, that exhibit good transmittance (Fig. 1.2):

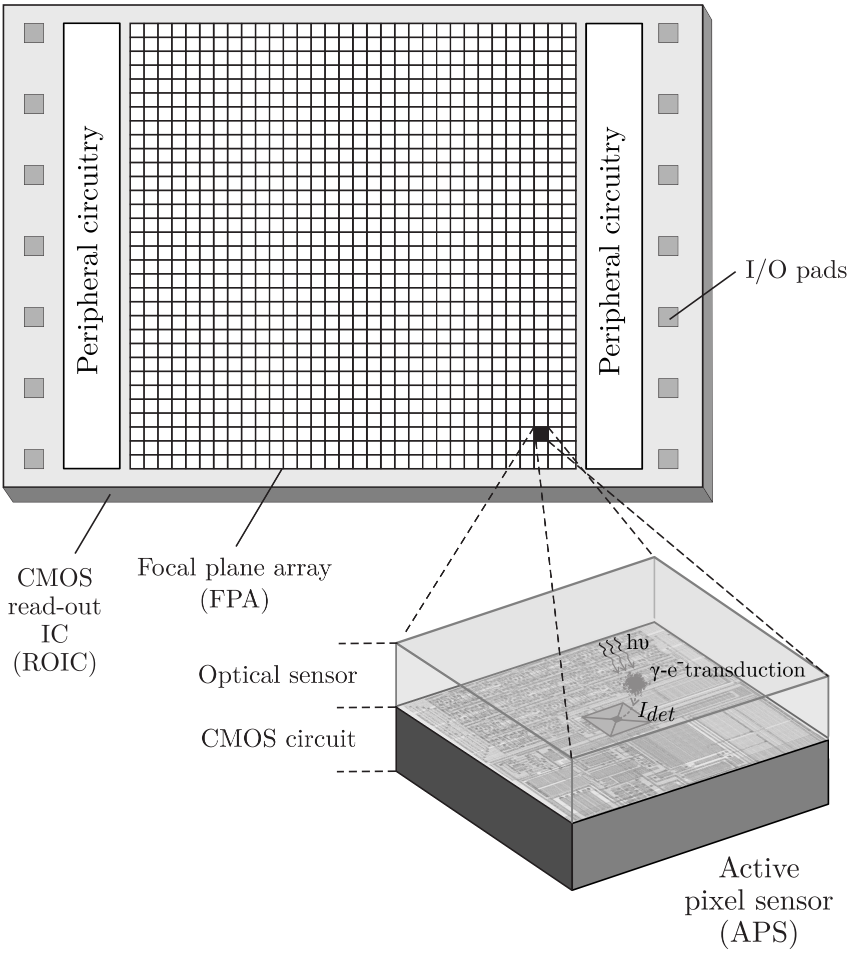
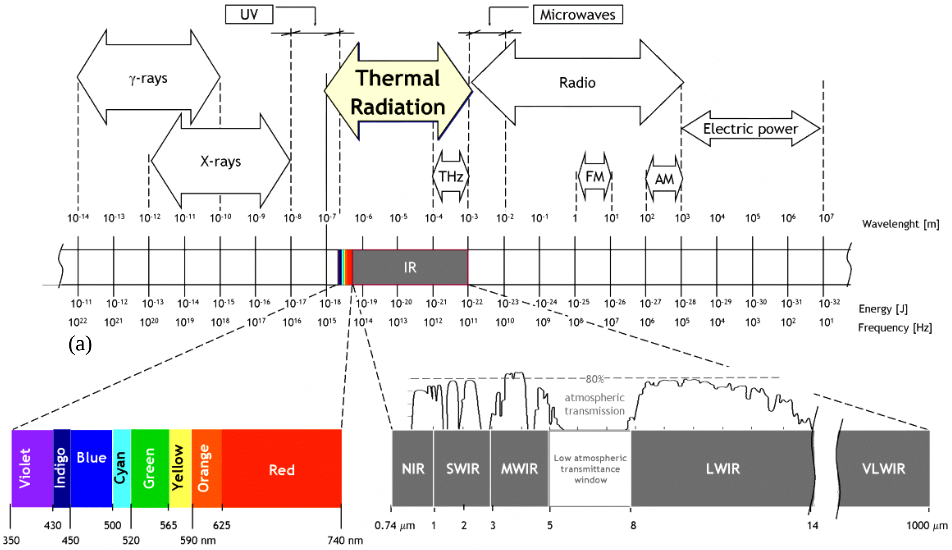

Peripheral circuitry
Peripheral circuitry
I/O pads
CMOS read-out IC (ROIC)
Focal plane array (FPA)
Optical sensor
CMOS circuit
hυ
γ-e⁻ transduction
I_{det}
Active pixel sensor (APS)

Figure 1.1 General view of a staring-FPA photonic CMOS imager. Optical sensors may be integrated in the same Si substrate, postprocessed on top of the CMOS dice or hybridized with the ROIC. Drawing not in scale.

- **Long wavelength infrared (LWIR).** This band extends roughly from 8 to 14 μm, with nearly full transmission on the 9 μm to 12 μm band. LWIR offers excellent visibility of most terrestrial objects.

- **Medium wavelength infrared (MWIR).** This wavelength range also delivers nearly 100 % transmission in the spectrum between 3 μm to 5 μm, with the added benefit of lower ambient background noise.

- **Short wavelength infrared (SWIR) - near infrared (NIR).** Also known as “reflected infrared” since light of these wavelengths are reflected by objects in a similar way than the visible spectra. Bands of high atmospheric transmission and maximum solar illumination (1 μm to 2.5 μm and 0.7 μm to 1 μm, respectively), detectors operating in these spectral ranges usually have better clarity and resolution than in the other two cases. Still, SWIR imagers need moonlight or artificial illumination in order to provide perceivable images at temperatures around 300 K.


UV
Microwaves
γ-rays
X-rays
Thermal Radiation
Radio
Electric power
THz
FM
AM
IR
Wavelenght [m]
Energy [J]
Frequency [Hz]
(a)
Violet
Indigo
Blue
Cyan
Green
Yellow
Orange
Red
350
430
450
500
520
565
590 nm
625
740 nm
80%
atmospheric transmission
NIR
SWIR
MWIR
Low atmospheric transmittance window
LWIR
VLWIR
0.74 μm
1
2
3
5
8
14
1000 μm

(b) **Visible** (c) **Infrared**

Figure 1.2 Electromagnetic spectrum (a); Visible bands (b); IR bands and absorption notches (c). Adapted from [9].

IR imaging is used for military and civilian purposes in all three spectral bands. Its multiple applications cover subjects as diverse as surface examination by thermography [10] (Fig. 1.3), automotive night vision [11], object tracking [12], weather forecast [13] and atomic analysis [14]. The global IR and thermal imaging market is predicted to grow from USD 3350 million in 2014 to USD 5220 million in 2019, at an estimated annual rate of 9.3% [15].

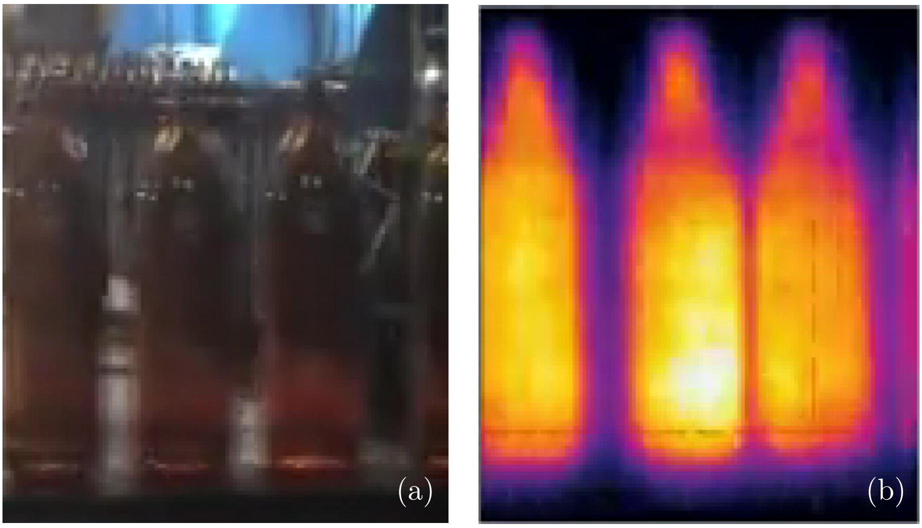


Figure 1.3 Example of glass container quality inspection using visible (a) and MWIR-radiation (b) sensitive cameras [16].

The next sections introduce the reader to the scope of this work. Sec. 1.2 reviews common metrics to evaluate the performance of IR cameras. Background on detector materials and structures used today in IR imagery is recounted in Sec. 1.3. Sec. 1.4 highlights the major characteristics of the adopted MWIR detector technology. The state-of-the-art of both FPA architectures and CMOS pixel readout techniques is presented in Sec. 1.5. This same section also enlists their operational requirements and summarizes their main modern representatives. This chapter finishes in Sec. 1.6 with a general overview of the research objectives.

1.2 Common Metrics and Figures of Merit

Common metrics and figure of merits (FOMs) are very useful tools to evaluate the performance of IR vision sensors, as they provide objective numeric values to compare between different design proposals. The following paragraphs review the top definitions that have been formulated along history.

Power Density: A typical requirement in applications using photonic FPAs. The local power (in W/pixel) dissipated by ROICs that operate this kind of detectors should be kept low to avoid undesired carrier generation effects.

Array Size and Pitch: Both array size and pitch are usually set by FPA technology. Higher image resolutions require larger array sizes and smaller pixel pitches. The former demand higher CMOS yields; the latter accommodate smaller integrator (charge storage) capacitances with a potential negative impact on the dynamic range figure defined below.

Dynamic Range (DR): The DR is defined as the power ratio of maximum signal capacity to noise floor and distortion components. The required dynamic range of imagers is determined by the ratio of the brightest to the weakest perceivable illumination level. Larger dynamic ranges are desirable but limited by storage capacitance, linearity and composite pixel noise.

Fill Factor (FF): Not all of the image sensor surface is sensitive to electromagnetic energy: each individual detector is commonly surrounded by material exclusively used to fit polarization and readout circuitry. The ratio of active sensing material to total pixel area is called the fill factor. Ideal pixel sensors have fill factors of 100% and devote all their surface to phototransduction, increasing their sensitivity and improving image quality. Today's best infrared staring-FPA cameras offer figures as high as 90%.

Quantum Efficiency (QE): QE is the fraction of photon flux that contributes to the total current generated by a photodetector. A crucial parameter to evaluate the quality of a detector, it is also known as spectral response due to its dependence on input radiation wavelength.

Thermal Contrast (C): The relative scene contrast C (given in K^{-1}) quantifies system sensitivity to thermal radiation and is defined by (1.1), where S is the root mean square (RMS) signal provided at the output of the device (expressed either as a voltage or current value) and T is the source temperature. It depends on the spectral photon (a.k.a. thermal) contrast $C_{T\lambda}$ $(\partial\Phi_e/\partial T)/\Phi_e$, where Φ_e is the spectral photon incidence; also on detector responsivity and charge losses in the pixel sensor readout chain.

$$\mathrm{C} = \frac{\partial S/\partial T}{S} \tag{1.1}$$

The MWIR spectral band is the region where thermal contrast is higher, and provides better contrast at room temperature than LWIR [17]. Even though most terrestrial objects radiate more heat in the latter region, this radiation is usually less sensitive to temperature changes.

Signal-to-Noise Ratio (SNR): In electronics, the minimum level below which a meaningful signal becomes masked and unrecoverable is usually delimited by noise or random electrical fluctuations. Considering this threshold value, the SNR provides a useful FOM in order to measure the transmission quality of a given signal of interest, defined as the ratio between the average power of signal and noise:

$$\mathrm{SNR} = \frac{P_s}{P_n} \tag{1.2}$$

IR photonic detectors like the PbSe sensor used in this work are designed so as to keep all other dark current, generation-recombination, thermal and flicker noise sources below the random fluctuations of photon-excited carriers at background radiation. This condition is known as background-limited infrared performance (BLIP). In this case, the SNR referred to the input of the detector is defined as

$$SNR_{BLIP} \doteq \frac{\mathrm{E}[S_{ph}]}{\sigma_{N_{ph}}} \tag{1.3}$$

where E is the expected value, and S_{ph} and N_{ph} are photon-signal and photon-noise random variables. Photogenerated carriers follow a Poisson distribution with well-defined expected value and variance

$$SNR_{BLIP} = \frac{N_c}{\sqrt{N_c}} = \sqrt{N_c} \tag{1.4}$$

where N_c is the number of generated carriers collected by the device. In quantum vision systems, the overall SNR is commonly related to the ideal BLIP performance

$$SNR_{img} = \eta_{BLIP} SNR_{BLIP} = \frac{SNR_{BLIP}}{\sqrt{1 + \sigma^2_{ROIC}/\sigma^2_{N_{ph}}}} \tag{1.5}$$

being η_{BLIP} the ratio of photon noise to composite imager noise and σ^2_{ROIC} the sum of all ROIC contributions. In this sense, most efforts in photonic vision sensor research are directed towards achieving a BLIP-level SNR by minimizing all other detector noise sources and reducing thermal, flicker and KTC readout temporal noise to an equivalent $\eta_{BLIP} = 1$.

Besides temporal noise sources, a second random and time-invariant noise source has to be taken into account: the fixed pattern noise (FPN). The pattern noise σ^2_{FPN} is associated with mismatch in the fabrication process of both detectors and readout circuits, and produces offset and gain drifts among the APS cells of the focal plane. This spatial noise component is usually included in the previous equation as an additive component composed of an equivalent average nonuniformity factor U multiplied by the N_c electronic signal [17]:

$$SNR_{img} = \frac{SNR_{BLIP}}{\sqrt{1 + \frac{\sigma^2_{ROIC} + \sigma^2_{FPN}}{\sigma^2_{N_{ph}}}}} \simeq \frac{SNR_{BLIP}}{\sqrt{1 + \frac{\sigma^2_{ROIC} + U^2 N_c^2}{\sigma^2_{N_{ph}}}}} \tag{1.6}$$

Responsivity: The responsivity of an infrared detector measures the ratio of the RMS value of the electrical output signal of the detector to the RMS value of the input radiation power. It is usually expressed in V/W or A/W.

In polychromatic IR radiation, the voltage spectral responsivity is given by

$$\mathrm{R_V} = \frac{V_s}{\Phi_e} = \frac{V_s}{\int\limits_0^\infty \Phi_e(\lambda) d\lambda} \tag{1.7}$$

where V_s is the RMS signal voltage due to Φ_e, and $\Phi_e(\lambda)$ is the spectral radiant incident power.

Current spectral responsivity, its most common form, can also be expressed analogously to $\mathrm{R_V}$ as a function of Φ_e, or directly as

$$\mathrm{R_I} = \eta \frac{q}{hf} = \eta \frac{q\lambda}{hc} \tag{1.8}$$

where η is the quantum efficiency of the incident photon to converted electron ratio at the detector for a given wavelength, q is the electron charge, h is Planck's constant, and f is the frequency of the optical signal. The right-hand equality defines it in terms of λ, the wavelength of the incident radiation, and the velocity of light c.

Noise Equivalent Power (NEP): The NEP is defined as the incident light power on a detector that generates an output signal equal to its output RMS noise. In other words, the NEP is the IR radiation that produces an SNR of 1. It is expressed in W and written in terms of responsivity as

$$\mathrm{NEP} = \frac{V_n}{\mathrm{R_V}} = \frac{I_n}{\mathrm{R_I}} \tag{1.9}$$

where V_n and I_n are RMS noise voltage and current signals, respectively. When it is referred to a fixed 1-Hz reference bandwidth, NEP has a unit of $\mathrm{W}/\sqrt{\mathrm{Hz}}$.

Detectivity (D): Detectivity is the reciprocal of NEP, commonly normalized (D^*) to the square root of the detector area A_d and electrical bandwidth Δf. Thus, D^* is defined as the RMS SNR in a 1 Hz bandwidth per unit RMS incident radiant power per square root of detector area, and expressed in Jones or $\mathrm{cm}\sqrt{\mathrm{Hz}}/\mathrm{W}$ as

$$\mathrm{D}^* = \frac{(A_d \Delta f)^{1/2}}{\mathrm{NEP}} \tag{1.10}$$

As detectivity depends on the spectral distribution of the photon source and the wavelength of the incident radiation, peak detectivity or D^*_{pk} is often preferred over the standard detectivity explained above. This measurement is taken at the wavelength of maximum spectral responsivity.

Noise Equivalent Temperature Difference (NETD): One of the most relevant metrics used today to measure the performance of IR imaging systems is the NETD. It is stated in K and summarizes the aforementioned FOMs by providing a unique, simple expression to evaluate the response in terms of their thermal sensitivity. NETD is described by (1.11) and represents the temperature change ΔT, for incident radiation, that gives an output signal change ΔV_s equal to the RMS noise level V_n [18]

$$\mathrm{NETD} = V_n \frac{\partial T}{\partial V_s} \tag{1.11}$$

Therefore, the NETD of a device is intimately linked to its overall SNR, the thermal contrast $C_{T\lambda}$ and the optics transmission τ_o taking into account optics, array and readout electronics in the form of

$$\mathrm{NETD} = \frac{1}{\tau_o C_{T\lambda} SNR_{img}} \tag{1.12}$$

Unnormalizing the thermal contrast by Φ_e unveils the also direct relation existent between NETD, NEP and D

$$\mathrm{NETD} = \frac{\partial T}{\partial \Phi_e}\mathrm{NEP} = \frac{\partial T / \partial \Phi_e}{\mathrm{D}} \tag{1.13}$$

As it can be seen, optimizing the NETD implies better thermal sensitivity either by improving the optics transmission, increasing the thermal contrast and/or the SNR, reducing the NEP or boosting detectivity. In order to account for both imaging speed and resolution, NETD×τ_{img} is usually employed as ultimate FOM. The second variable of this expression (τ_{img}) is the acquisition time constant of the device.

1.3 IR Direct Detectors

Various IR sensors have been developed to convert incident radiation, directly or indirectly, into electrical signals. There are two fundamental methods of IR detection, each one based on either thermal or photonic effects [19, 20]. Both technologies and their variants are described in detail in the succeeding sections.

1.3.1 Thermal and Photonic Transduction

Thermal or energy detectors change their electrical properties according to temperature rises on their composing material. These thermal variations are caused by the energy absorbed from an incident IR radiation, and transduced as fluctuations in physical aspects like their conductivity or dielectric constant. Thermal detectors are low-cost, operate at room temperature, and exhibit a characteristic wide, flat spectral response. Since the operation of energy detectors implies a second interaction with the temperature of the material - and sensitiveness is enhanced by insulating this material from its surroundings - they are intrinsically slow and present higher time constants that their photonic analogues. The response time and sensitivity of a thermal detector depend on the heat capacity of the detector structure and the wavelength of the incoming photon flux.

Among all thermal transductors, thermopiles stand out for their low cost and high sensitivity in low-frequency/direct current (DC) applications. Pyroelectric detectors and (micro)bolometers offer better performance at higher frequencies, and are widely extended in this range. Nevertheless, the former reliance on external chopping and their sensitivity to vibration have made the latter the present technology of choice for uncooled thermal imagers below 100Hz.

Photon detectors exploit the quantum properties of semiconductor materials to perform direct transduction of IR illumination. The energy supplied by photonic radiation is absorbed in the crystalline lattice so as to generate new e-h pairs, free carriers that provide the electrical signal to acquire. Because of this direct interaction with light, photon detectors are faster than their thermal counterparts. Thermal transitions compete, however, with the optical ones, making non-cooled devices prone to present high background noise. Bulky cooling mechanisms are usually required to avoid these effects [21]. Popular photon-based transduction technologies are P-N junction photovoltaic (PV), photoemissive (PE), photoconductive (PC) and quantum well IR photodetector (QWIP) detectors.

PV transducers often achieve high sensitivity, low time constants and nearly-null power consumption. Compared to P-N junction devices, photo-emissive detectors lack of high-temperature diffusion processes, and exhibit a faster response with practically unnoticeable 1/f noise. However, the low quantum efficiency (around 1%) and slow spectral response of Schottky-barrier detectors limit the application to industrial MWIR imagers. PCs generally have higher responsivity than non-avalanche photovoltaic detectors, but lower yield and additional generation-recombination noise sources than PV detectors. Their dynamic ranges and sensitivities are notoriously variable depending on which semiconductor material they are based on. Quantum well devices are attractive for their fast response time, low power consumption and high manufacturing yield. Nonetheless, they typically exhibit low quantum efficiencies ($< 10\%$), rely on cryocooling, and present a very narrow spectral response band.

Table 1.1 summarizes the main types and materials of IR detectors. Many of them are based on compound semiconductors made of III-V (e.g. indium, gallium, arsenic, antimony), II-VI (e.g. mercury, cadmium, telluride), or IV-VI elements (e.g. lead, sulfur, selenide). They can be also combined into binary compounds like GaAs, InSb, PbS and PbSe, or even into ternaries such as InGaAs or HgCdTe.

Fig. 1.4 shows the spectral detectivity D^* of leading infrared detector technologies, under different operational temperatures. InSb and PtSi PE display topping MWIR figures at the cost of needing additional cooling. Uncooled lead-salt photoconductors such as PbS and PbSe also have higher detectivity than thermal transducers, specially PbS, the latest at lower SWIR wavelengths and typical cut-off frequencies (around 10 times below) than PbSe-based detectors [22]. InAs PV sensors lie very close to PbSe too, but are still on an early stage of development and their integration require of expensive hybridization procedures. On the LWIR band, best detectivities are reserved to cryocooled photonic transducers like HgCdTe PV and GaAs QWIP detectors. PV detectors excel at SWIR performance in ambient temperature.

Photon detectors		**Energy detectors**	
Intrinsic, PV	- HgCdTe - Si, Ge - InGaAs - InSb, InAsSb	(μ)bolometers	- V_2O_5 - PolySiGe - PolySi - Amorph Si
Intrinsic, PC	- HgCdTe - PbS, PbSe	Thermopiles	- BiSb
Extrinsic	- SiX	Pyroelectrics	- LiTa - PbZT
Photoemissive	- PtSi	Ferroelectrics	- BST
QWIP	- GaAs/AlGaAs	(micro)cantilevers	- Bimetals

Table 1.1 | Overview of IR detector types and materials.

1.3.2 IR Detection Today

Based on the transduction materials explained in the previous section, a wide range of high-performance IR cameras have been developed and are commercially available at present. However, and unlike Si CCDs and CMOS imagers for visible applications, most of them are still far from reaching volume applications. Key limiting factors are:

1. **Sensor complexity.** Mainstream IR imagers are based on "exotic" materials (e.g. InP, HgCdTe, SiPt, etc.) with complex fabrication procedures behind.

2. **Packaging costs.** Most of them are not compatible with Silicon technology. They need to be hybridized with the Si ROIC, resulting in cumbersome and expensive packaging (e.g. bump bonding by flip chip).

3. **Need of bulky cooling mechanisms.** The majority of photon detectors need to be cooled at cryogenic temperatures to avoid the serious performance limitations caused by thermally-induced carriers.

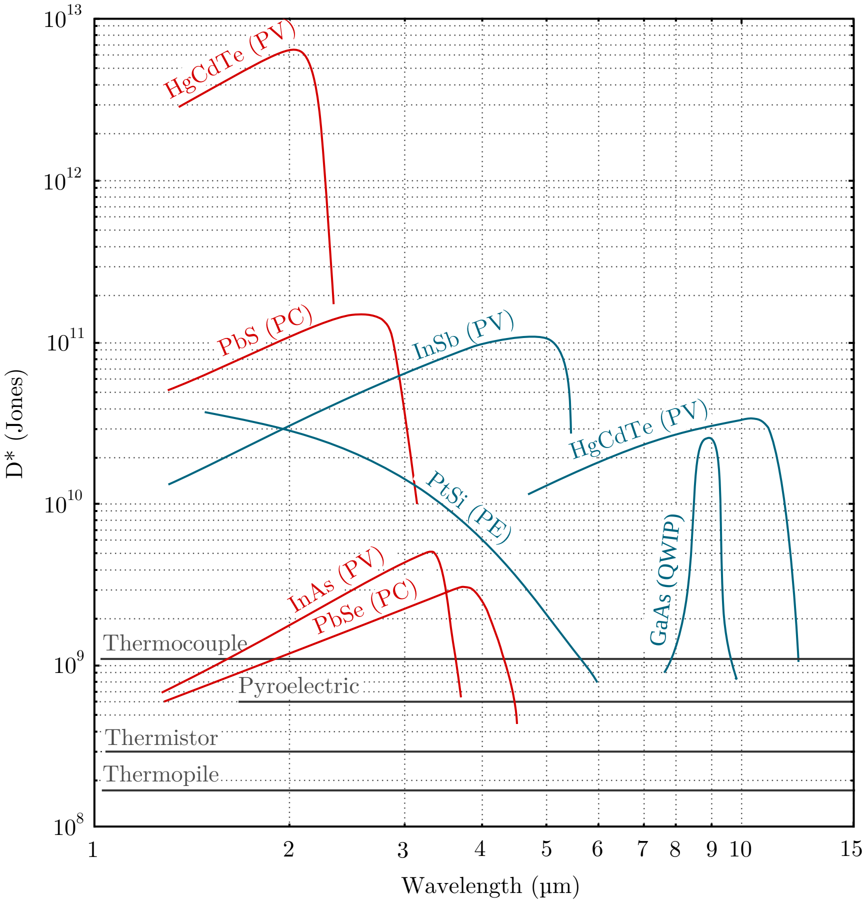


Figure 1.4 Typical spectral response of main IR thermal and photon detectors at 295K room temperature (gray and red, respectively), and photon detectors at 77K cryogenic temperature (blue). Background illumination is assumed to be at a temperature of 300K [20].

Among all, three major technologies are in practice dominating the IR imaging market. Microbolometers are the common choice for thermal imaging in the LWIR range, showing very low-cost figures thanks to their CMOS technology compatibility and uncooled operation. Although pixel pitch is being progressively improved, microbolometers intrinsically suffer from limited signal sensitivity, poor spectral discrimination and low frame rate (below 100 fps), and need to be packaged in vacuum. On the other hand, QWIP can cover those applications demanding both high-speed and high-sensitivity, typically in the SWIR range, at the expense of higher fabrication costs and power consumption due to their hybrid packaging and cryogenic cooling, respectively. HgCdTe and InSb detectors are the material of choice for high performance M/LWIR appliances but are susceptible to manufacturing mismatch and require of cryogenic refrigeration to operate at such wavelengths. An interesting alternative to avoid this trade-off is the choice of PbSe photoconductive technologies. These MWIR detectors allow uncooled operation like microbolometers, but with the high-speed capabilities of their photonic counterparts.

1.4 Uncooled PbSe Photoconductive Technology

1.4.1 Detection Basis

Polycrystalline lead-selenide photoconductors are composed of a compact layer of PbSe microcrystals able to provide high and fast response to radiation in the MWIR spectrum range at room temperature. As quantum high-resistance semiconductor detectors, they exhibit low thermally activated mobility. Their conductivity increases proportionally to direct light intensity and is strongly influenced by intergran barriers. Accordingly, detectivities up to 10^9 cm$\sqrt{\mathrm{Hz}}$/W and response times in the μs range can be achieved at ambient heat levels of 300 K, which makes them remarkable candidates for high-speed and low-cost uncooled IR detection.

Standard polycrystalline PbSe films are produced by chemical bath deposition (CBD) in order to introduce effective minority carrier traps and make them sensitive to IR radiation. Nonetheless, wet CBD imposes serious technological limitations on uniformity and reproducibility to manufacture medium and large-scale 2D detector arrays in monolithic devices. To overcome this limitations, an alternative procedure based on thermal evaporation of PbSe in vacuum followed by a specific sensitization method was developed [23, 2]. The new VPD method deposits a thin layer of PbSe on standard CMOS wafers that provide the readout electronics. The resulting monolithic 2D detectors show higher uniformity and longer term stability than PbSe detectors manufactured with standard CBD procedures. Vision sensors made by VPD offer good yield in standard 8-inch wafers, and are compatible with complex monolithic multilayer structures like interference filters.

Such features allocate polycrystalline PbSe among the major players in the short list of uncooled IR detectors. Unlike thermal detectors, PbSe salts constitute a quantum detector sensitive to the MWIR band able to deliver acquisition rates beyond the kfps range. The list of applications is extensive, some of them specific and highly demanded in the strategic fields such as fast Active Protection Systems or low cost seekers. Table 1.2 compares major characteristics of present prime technologies - in the MWIR and LWIR bands of self-emission - versus VPD PbSe detectors.

	IR Technology			
	VPD PbSe	microbolometers	QWIP	HgCdTe/InSb
Peak detectivity	medium	medium-low	medium-high	high
Quantum efficy.	medium	n/a	low	high
Response speed	**fast**	slow	very fast	very fast
Si compatibility	**yes**	yes	no	yes
Uniformity	medium	high	good	medium
Active cooling	**no**	no	yes	yes
Integration cost	**low**	low	medium	high
Packaging reqs.	**low**	high	high	medium
Optics	**economical**	expensive	economical	economical
Spectral selecty.	**high**	very low	very high	high
Spectral band	**MWIR**	LWIR	LWIR	S/M/LWIR*

Table 1.2 Performance and cost comparison between leading IR detection technologies.
*Depending on temperature and detection mode (i.e. PV or PC).

In order to reconcile detector and circuit materials at their interface, PbSe is contacted by gold (Au) on top of a stacked metal layer to access each individual CMOS sensor. The obtained pixel stacked structure allows fill factors to exceed 50% for the DPS. The smooth edges of Fig. 1.5(a) homogenize electrical field and avoid point effects in paths. Unlike microbolometers, photoconductive PbSe detectors do not need to be operated in vacuum to minimize thermal conductivity effects from surrounding environment. Hence, the whole IR system can be encapsulated in low-cost standard packages with sapphire window.

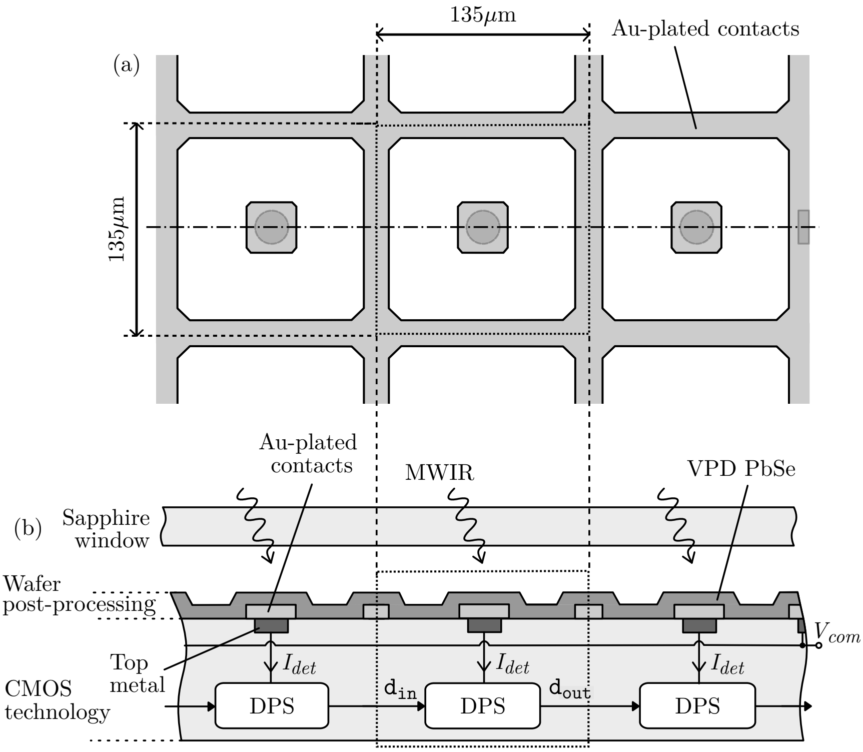

(a)
135μm
Au-plated contacts
135μm
(b)
Sapphire window
Au-plated contacts
MWIR
VPD PbSe
Wafer post-processing
Top metal
CMOS technology
I_{det}
I_{det}
I_{det}
V_{com}
DPS
DPS
DPS
$\mathtt{d_{in}}$
$\mathtt{d_{out}}$

Figure 1.5 | Simplified layout (a) and cross-section (b) of the MWIR VPD PbSe detector after being post-processed on top of its CMOS wafer.

1.4.2 Device Performance

Fig. 1.6 shows the MWIR response of current implementations of the post-processed PbSe detector at room temperature, which returns the typical triangular-shaped spectral profile of quantum detectors. Signal modulation bandwidth under uncooled operation extends up to 60kHz. Due to the high resistive (typically around 1MΩ) nature of PbSe detectors, current readout at constant voltage bias is preferred over voltage readout at constant current strategies. Contrary to the typical ohmic behavior, the PbSe resistance depicted in Fig. 1.7(b) decreases exponentially with the applied bias voltage and exhibits even larger drops under electrical fields exceeding 1.5μV/m. The former effect is attributed to operational self-heating.

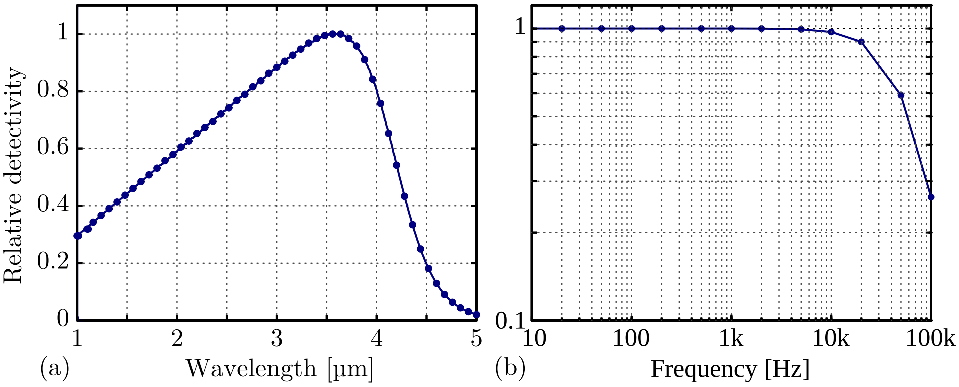


Figure 1.6 Experimental response of the integrated VPD PbSe photoconductor at 300K in terms of MWIR spectral detectivity (a) and modulation bandwidth (b).

Fig. 1.8 displays the photoconductor noise response to the same voltage sweep at 330Hz, approximately in the middle of the flicker-noise dominant region. Voltage dependence is again exponential, but in this case crescent. Its magnitude is strongly influenced by the quality of PbSe post-processing, and barely depends on the concrete pixel geometry. Fixing the bias close to 1V allows to keep noise values at moderate pA/Hz$^{-1/2}$ levels. Fig. 1.9 shows typical power spectral density (PSD) boundaries for a 40μm pitch detector biased at the suggested 1V value, and evinces the predominance of 1/f noise up to a corner frequency located between 100kHz and 1MHz. At low frequencies, flicker noise becomes masked by transducer thermal stability. Output capacitance under these bias conditions is inversely proportional to the square of pixel pitch as illustrated in Fig. 1.7(a).

In practice, PbSe exhibits both noticeable background photogeneration mean and deviation due to uncooled operation and the amorphous nature of its structure, respectively. The latter can lead to signal-to-dark current ratios close to unity under common radiation scenarios (e.g. 1μA for a 1-V biasing). The measured parameters of the VPD PbSe photoconductor are summarized in Table 1.3. NETD performance was measured at a temperature of 600K, accordingly to the MWIR spectral range of the transducer.

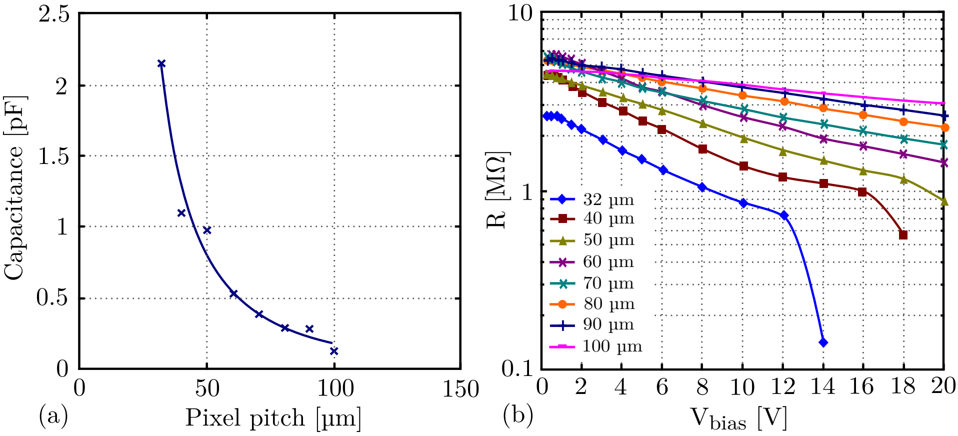


Figure 1.7 | Experimental output capacitance versus pixel size (a); dark resistance versus bias potential for several pixel pitch values (b) of the VPD PbSe photoconductor.

Parameter	Value	Units
Spectral range at -3dB	1.7 to 4.3	μm
Peak detection wavelength	3.7	μm
Peak detectivity	1.9×10^9	cm$\sqrt{\text{Hz}}$/W
Flicker corner frequency (f_c)	60	kHz
NETD at 600K	125	mK

Table 1.3 | Typical parameters of the VPD PbSe photoconductor.

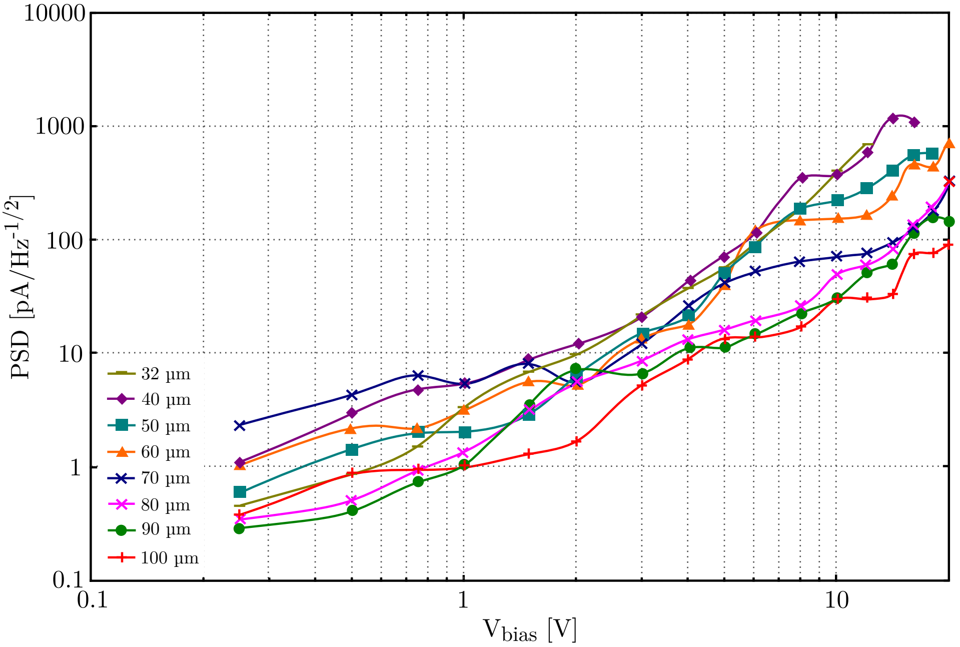


Figure 1.8 Experimental noise of the VPD PbSe photoconductor versus bias potential at 330Hz, for several pixel pitch values.

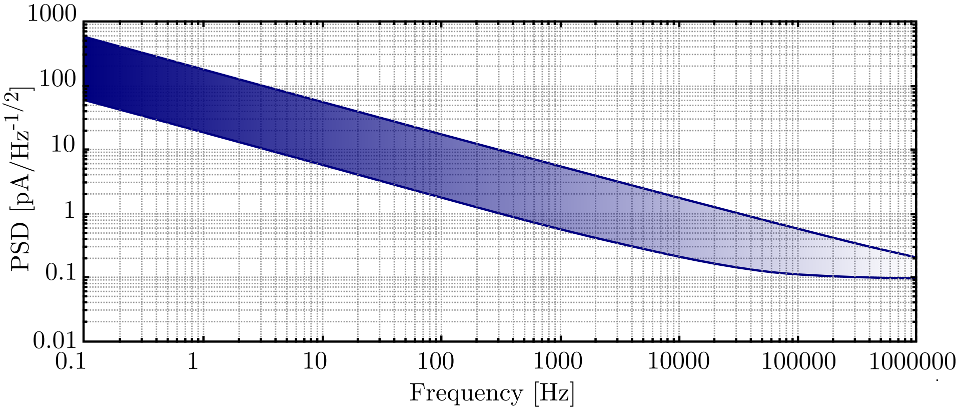


Figure 1.9 Experimental noise margins of the VPD PbSe photoconductor for a fixed pitch of 40μm and an applied bias potential of 1V.

1.4.3 Electrical Model

All main non-idealities of the PbSe sensor have been modeled into a practical and flexible circuit suitable for the electrical simulation of APS CMOS designs. The model incorporates sensor current I_{det} dependence on both optical responsivity (R_{opt}) and incident light power (P_{in}), including also:

Dark current: At non-cryogenic temperatures, PbSe presents a certain value of dark current that can be represented with no thermal drift as a DC component (I_{dark}) independent from IR illumination. Because the measured ratio between the offset and the effective current is relatively high (μA/nA), it is strongly desirable to obtain a fine model for this phenomena.

Noise: Modeled as a thermal, white noise or as a flicker, pink component depending on the frequency of operation.

Non-lineal output resistance: I_{det} variability with bias voltage (V_{det}) is represented as a finite non-linear resistance described by means of an $I_{det} = g(V_{det})$ lookup table.

Output capacitance: As its own name suggests, this electric component (C_{out}) characterizes I_{det}-V_{det} dynamics.

Based on the previous detector parameters, an equivalent circuit is proposed for global system simulation. Its key features are:

- Inclusion of all the effects previously related.
- SPICE language compatibility.
- Easily-configurable detector variables.
- Direct tuning based on experimental characterization.

This circuit is shown in Fig. 1.10, where I_{gen} is the photogenerated current, R_{neq} is the equivalent noise resistance, f_c is the flicker noise corner frequency, $\bar{g}$ is the normalized output conductance and C_{out} is the output capacitance.

The suggested model is made of two main subcircuits, relative to current generation (e.g. dark and noise currents) and to output port (e.g. nonlineal resistance and capacitance). Concerning first section, R_{neq} is also used for I_{dark} generation, creating noise dependence on current biasing. The second part of the circuit is composed of an output resistance, as a function of I_{gen}, which ensures no I_{det} under zero V_{det} conditions. The SPICE implementation of Fig. 1.10(a) is made through the schematic of Fig. 1.10(b), where each component function can be easily recognized. The model also uses the sens_Rneq and sens_Rout files as noise and normalized output conductance tables, granting a direct inclusion of PbSe experimental characterization results.

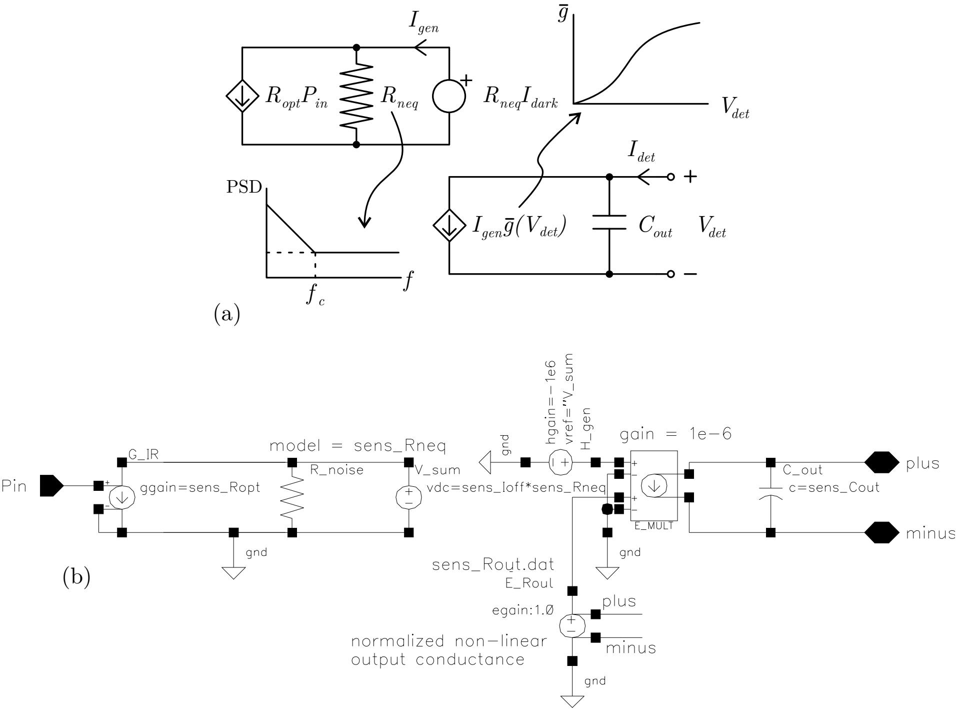

I_{gen}
$\bar{g}$
$R_{opt}P_{in}$
R_{neq}
+
$R_{neq}I_{dark}$
V_{det}
I_{det}
+
PSD
$I_{gen}\bar{g}(V_{det})$
C_{out}
V_{det}
−
f_c
f
(a)
hgain=−1e6
vref="V_sum
H_gen
gnd
gain = 1e−6
model = sens_Rneq
G_IR
R_noise
V_sum
Pin
ggain=sens_Ropt
vdc=sens_Ioff*sens_Rneq
E_MULT
C_out
c=sens_Cout
plus
minus
gnd
gnd
(b)
sens_Rout.dat
E_Rout
egain:1.0
plus
minus
normalized non−linear
output conductance
gnd

Figure 1.10 | VPD PbSe detector circuit equivalent (a) and schematic view (b).

1.5 CMOS IR Imagers

1.5.1 Readout Techniques

The relentless growth of imaging applications has rocketed on-chip sophistication in both visible and IR FPAs. To achieve good overall performance, a suitable trade-off has to be achieved among circuit performance, power dissipation, chip area, and image resolution. CMOS readout electronics play a key role in satisfying these demands so as to ensure a proper interface between detectors and the following signal processing stage. A considerable amount of pixel readout structures have been developed for different system applications and concerns. In this scenario, circuit techniques are evolving from purely analog APS cells in voltage [19, 24–26] or current [27–30] domains to digital pixel sensors (DPSs) with built-in analog-to-digital converters (ADCs). Digital imager architectures are dominated by in-pixel readout stages containing analog-integrator preamplification and a posterior sampler-and-hold. In the case of large IR staring-FPAs, straightforward input topologies like source follower per detector (SFD) [31–35], direct injection (DI) [36–39] and gate modulation input (GMI) [31, 40] are still popular because of their compactness and reduced power consumption [19]. Other complex circuit techniques like buffered direct injection (BDI) [36, 41] and capacitive transimpedance amplifier (CTIA) [42–44, 39] offer higher performance by providing excellent bias control, high injection efficiency, linearity and lower noise figures. More recent structures like share-buffered direct injection (SBDI) [45], switched-current integrator (SCI) [46] and buffered gate modulation input (BGMI) [47] are intended to provide better compromise between pixel size constraints and readout performance.

Source Follower per Detector (SFD: The simplicity of SFD circuits is shown in Fig. 1.11(a). In this scheme, I_{det} current is integrated directly into the intrinsic detector capacitance C_{det} and reset at the input node. The consequent voltage-mode signal is source-followed through M1, and conducted to the following stage. Major setback of this topology is its non-linear behavior as a direct result of detector bias voltage changes along integration. Reset switching noise also has noticeable effects on the integrity of output signal. SFDs are most commonly found in large-format hybrid astronomy FPAs and commercial monolithic CMOS devices.

Direct Injection (DI): The DI circuit was one of the first circuits to be developed as input stage for CCDs and visible imagers. The simpleness of the DI circuit is illustrated in Fig. 1.11(b), where the p-channel metal-oxide-semiconductor (PMOS) transistor M2 is used to direct I_{det} charges into C_{int}. The integrating capacitor is reset through the `reset` signal. DI is commonly employed for tactical applications, where background illumination is high and detector equivalent resistances are average. Direct injection provides better bias control than SFD during integration using the common-gate PMOS, but is not suitable for low IR background applications due to injection efficiency issues. Other concerns are its nonlinearity, noise sensitivity, and its reliance on stable and low-noise DC biasing. In order to achieve better linearity and noise behavior, the inverting amplifier -A is provided between the detector node and the input M2 gate. This improvement comes at the cost of increasing power consumption and considerably higher Si area requirements. The SBDI topology described in [45] relax this constrains by splitting the differential amplifier that constitutes -A gain stage and sharing it between the pixel cells of each row.

Gate modulation input (GMI): The GMI readout circuit of Fig. 1.11(c) has a current-mirror configuration with the V_s-tunable current gain. C_{int} capacitor is charged by the M4-mirrored current to an output voltage signal. This topology offers the possibility to perform logarithmic sensing by operating the current mirror in subthreshold. Pros of GMI are higher sensitivity and noise immunity than DI, and its capacity to widen the dynamic range by direct current gain adaptation to background levels. On the other hand, both injection efficiency and current gain of GMIs are easily affected by variations in V_s and metal-oxide-semiconductor field-effect transistor (MOSFET) threshold voltages.

Capacitive transimpedance amplifier (CTIA): The schematic description of a CTIA is depicted in Fig. 1.11(d), and locates the integration circuit in the feedback loop of the preamplification stage. In this case, C_{int} is reset to an adjustable V_{ref} value using the operational amplifier (OA) negative feedback. CTIA circuits are more complex and power-greedy than DI, SFD and GMI implementations but in return they deliver an extremely linear response. Because changes at the input node of the amplifier are directly compensated by the inverting loop, CTIAs provide stable detector biasing with low input impedances. Moreover, and unlike (B)DI, the input impedance of the CTIA is independent of transducer's current, providing bipolar integration for both positive and negative biases. High frequency bandwidths and good photon current injection efficiencies are also expected from this circuit. Proper CTIA designs must, however, take into account feedthrough effects of the reset clock on both detector bias and the operational amplifier.

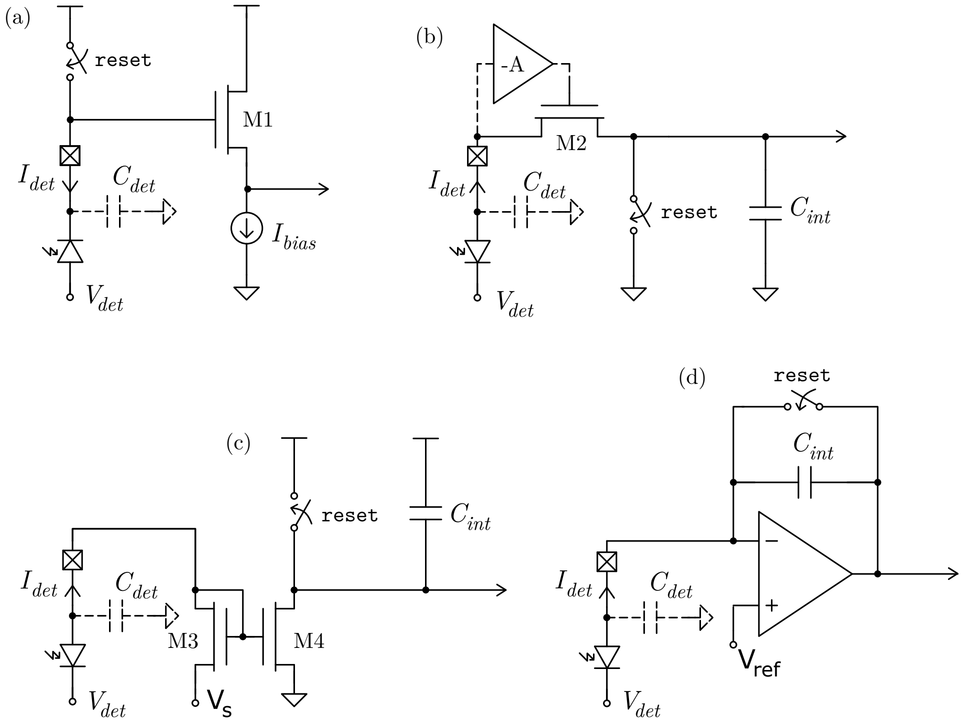

(a)
reset
M1
I_{det}
C_{det}
I_{bias}
V_{det}
(b)
-A
M2
I_{det}
C_{det}
reset
C_{int}
V_{det}
(c)
reset
C_{int}
I_{det}
C_{det}
M3
M4
V_{det}
V_s
(d)
reset
C_{int}
I_{det}
C_{det}
−
+
V_{ref}
V_{det}

Figure 1.11 Common readout input circuit schemes: SFD (a), DI and buffering (dashed amplifier) (b), GMI (c) and CTIA (d).

1.5.2 FPA Architectures

Once converted to voltage in the previously referred readout input schemes, the photogenerated signal is sampled, by either a plain S/H circuit or a correlated double sampling (CDS) circuit, and buffered by a line driver. Pixel outputs are multiplexed in the analog domain and, in case of digital imaging, transferred to an internal ADC before or after multiplexation. The former case corresponds to the classic imagers of Fig. 1.12(a) constituted by an FPA of analog APS cells, addressed through peripheral row/column digital scanners and biased by means of a global reference generator. S/H memory elements can be taken outside the FPA, and shared by columns [48–50] to reduce pixel pitch. In this context, imager noise includes contributions from the CMOS circuitry itself. Considering all major temporal noise sources as uncorrelated, the SNR figure of (1.5) for traditional APS-based vision devices is limited by the percentage of BLIP:

$$\eta_{BLIP} \simeq \frac{\sqrt{N_c}}{\sqrt{N_c + \sigma_{det}^2 + \sigma_{integ}^2 + \sigma_{samp}^2 + \sigma_{drv}^2 + \sigma_{MUX}^2 + \sigma_{ADC}^2}} \tag{1.14}$$

where the sum of all ROIC noise contributions are: composite dark current, thermal and flicker detector noise (σ_{det}^2), integrator noise (σ_{integ}^2), KTC noise of the sample-and-hold stage (σ_{samp}^2), line driver buffering noise (σ_{drv}^2), and the additional noise introduced by the analog multiplexer (σ_{MUX}^2) and final ADC stages (σ_{ADC}^2).

The CDS technique is employed to suppress offset and low-frequency noise components up to the sampling stage. In order to furtherly improve signal integrity, some imager architectures still implement analog pixel schemes, but perform internal A/D conversion at chip [51, 52] or row/column levels [53–55], the latter earlier to output multiplexing. Fig. 1.12(b) and Fig. 1.13(a) illustrate, respectively, an example of such systems. Compared to Fig. 1.12(a,b), ADC sampling ratio in Fig. 1.13(a) - so equivalent noise bandwidth - can be reduced proportionally to the number of columns, with the corresponding N-times downscaling of σ_{ADC}^2 in case ADC is thermal noise limited. Furthermore, σ_{MUX}^2 is also lowered as row multiplexing is performed in the digital domain, but it still remains in (1.14) due to the existence of analog buses that tend to cause inter-pixel crosstalk. On the other hand, power consumption for each ADC of Fig. 1.13(b) is required to be also downscaled N-times with respect to their counterparts in Fig. 1.12(a,b).

DPS architectures like Fig. 1.13(b) further minimize the effects of the aforementioned noise sources on the overall SNR (1.5) by implementing A/D conversion internally in the pixel. First point to note in the architecture

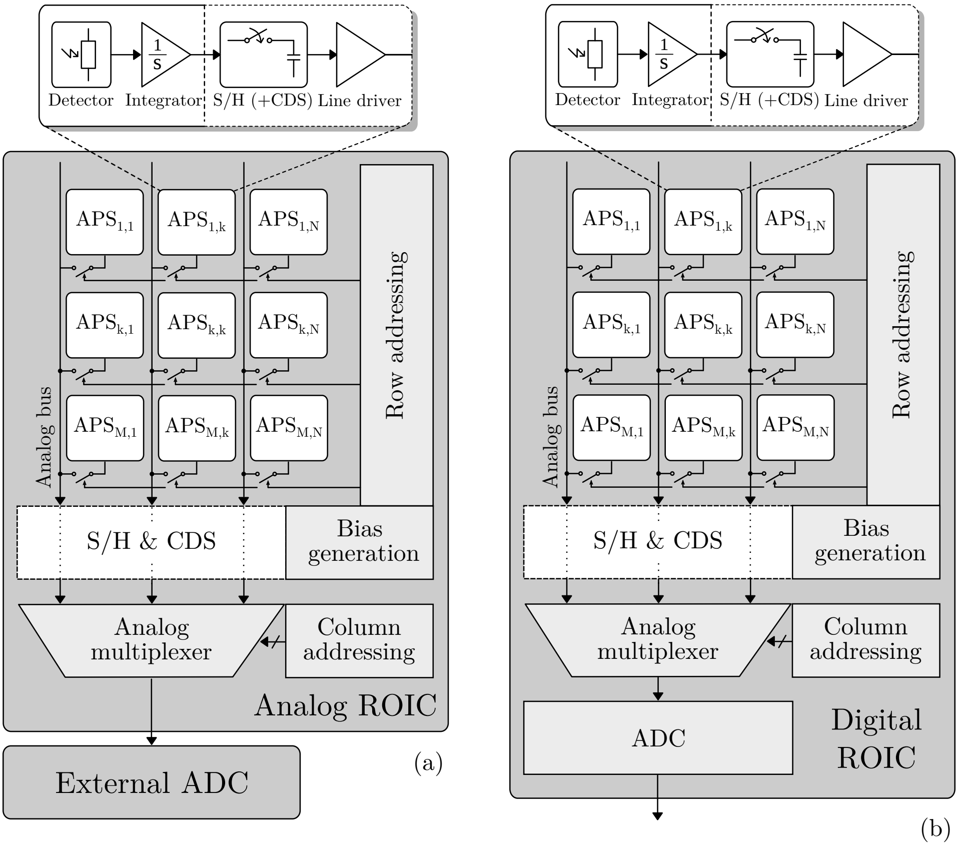

Detector
Integrator
S/H (+CDS)
Line driver
1/s
APS$_{1,1}$
APS$_{1,k}$
APS$_{1,N}$
APS$_{k,1}$
APS$_{k,k}$
APS$_{k,N}$
APS$_{M,1}$
APS$_{M,k}$
APS$_{M,N}$
Analog bus
Row addressing
S/H & CDS
Bias generation
Analog multiplexer
Column addressing
Analog ROIC
External ADC
(a)
ADC
Digital ROIC
(b)

Figure 1.12 Classic chip-level external (a) and internal (b) ADC readout architectures. Dashed lines indicate variable circuit location: S/H, CDS and buffering can be moved outside the FPA in order to lessen pixel dimensions.

of Fig. 1.13(b) is the avoidance of inter-pixel analog signaling. The use of digital readout cells results in the reduction σ^2_{MUX} and σ^2_{drv} contributions from (1.14), the elimination of read-related column FPN and a drastical optimization of digital pixel output buffers in terms of power. Second, the in-pixel ADC strategy allows to further scale noise bandwidth down to σ^2_{ADC}/MN compared to Fig. 1.12 at the cost of even stronger power and area circuit design constrains. Fully parallel ADC at pixel level also facil-

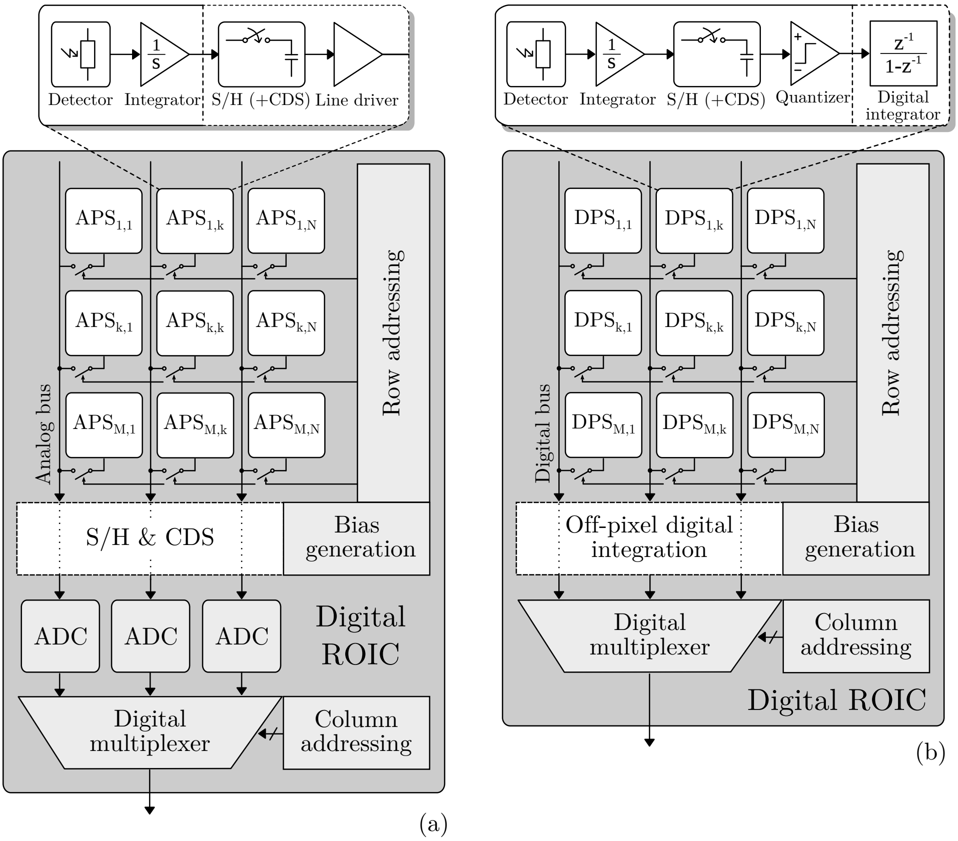

Detector
$\frac{1}{s}$
Integrator
S/H (+CDS)
Line driver
$\text{APS}_{1,1}$
$\text{APS}_{1,k}$
$\text{APS}_{1,N}$
$\text{APS}_{k,1}$
$\text{APS}_{k,k}$
$\text{APS}_{k,N}$
$\text{APS}_{M,1}$
$\text{APS}_{M,k}$
$\text{APS}_{M,N}$
Analog bus
Row addressing
S/H & CDS
Bias generation
ADC
ADC
ADC
Digital ROIC
Digital multiplexer
Column addressing
(a)
Detector
$\frac{1}{s}$
Integrator
S/H (+CDS)
+
−
Quantizer
$\frac{z^{-1}}{1-z^{-1}}$
Digital integrator
$\text{DPS}_{1,1}$
$\text{DPS}_{1,k}$
$\text{DPS}_{1,N}$
$\text{DPS}_{k,1}$
$\text{DPS}_{k,k}$
$\text{DPS}_{k,N}$
$\text{DPS}_{M,1}$
$\text{DPS}_{M,k}$
$\text{DPS}_{M,N}$
Digital bus
Row addressing
Off-pixel digital integration
Bias generation
Digital multiplexer
Column addressing
Digital ROIC
(b)

Figure 1.13 Typical column-level (a) and pixel-level (b) ADC readout architectures. Dashed lines indicate variable circuit location: S/H, CDS, buffering and digital integration can be moved outside the FPA in order to compact pixel pitch.

itates the inclusion of additional image and video processing functionality in the ROIC, boosts technological downscaling and opens the possibility to shoot readout speeds up to real-time operation.

In order to curtail the analog parts of the DPS ADC, predictive architectures (e.g. integrating, sigma-delta) are usually preferred at pixel level over direct (e.g. flash) or algorithmic (e.g. successive approximations) alternatives. Such predictive ADCs usually involve a pulse modulator, in charge of quantifying in continuous-time the amplitude of the sensor signal at 1 bit, and a digital filter to cut off the high frequency components of the resulting quantification noise and to complete discretization in time. Basically, two different pulse modulation (PM) approaches can be found for the first stage of the ADC: pulse width modulation (PWM) also known as time-to-first-spike [56–64], and pulse density modulation (PDM) also called spike-counting [65–68, 62, 69, 70], or even mixed solutions like [71, 72]. Each one of these pixel modulation strategies can be performed synchronously by means of traditional frame acquisition times [56, 65, 57–62] or the more recently introduced event-based approach [63]. This last scheme was, nonetheless, developed to allow an asynchronous event-driven readout [73, 74, 68, 69, 64, 70, 72] and is commonly exploited in this frame-free scenario. Synchronous frame-based readout DPSs usually implement in-pixel digital counters in order to integrate the output spikes.

1.5.3 State-of-the-Art IR Vision Sensors

Table 1.4 resumes the main characteristics of state-of-the-art top-notch CMOS IR imagers. Current efforts are focused on improving the transportability, sensitivity and resolution of these systems in the MWIR and LWIR spectral bands. Focal plane resolution is extended by means of reducing pixel sensor and readout circuit area, physically increasing FPA matrix dimensions, or both. The first strategy requires a progressive scaling of integration technologies, especially in CMOS ROIC circuits, reduction of the APS power consumption and an optical refinement of the complete system. The second strategy is applied through high yield IR detector and VLSI CMOS technologies. In order to achieve small process variances in both implementations, megapixel IR camera designs usually integrate each technology separately and attach them by new experimental modular hybrid strategies [75, 76].

Upper-end IR devices offer higher sensitivity and resolution by incorporating highly-selective refrigerated quantum detectors hybridized at CMOS wafer level [33–35, 77–84]. Dual-band QWIP implementations like [85, 86] extend vision capabilities to bispectral M/LWIR vision applications. Low-cost IR imaging solutions are mostly based on monolithic VOx [87, 88] or a-Si [89–91] microbolometers thermal approaches, and avoid any incorporation of external cooling mechanisms. Common trend is to move ROIC designs to the digital domain performing A/D conversion either at column or pixel stages. All systems integrate full-custom application specific integrated circuit (ASIC) designs by using advanced, but mature and affordable, CMOS technologies. FPN-compensated or high-speed kfps-range FPAs architectures are particularly scarce in literature.

1.6 Objectives and Scope

The goal of this thesis is to investigate novel CMOS analog and mixed-signal circuit design techniques for low-cost and high-speed MWIR vision sensors to be used in real-time scenarios. The work takes the baton on the latest technological advances in the field of VPD PbSe detectors accomplished by NIT S.L. [2], adding fundamental research on the development of the full-custom readout circuitry with the objective to integrate a complete line of state-of-the-art uncooled MWIR cameras for industrial applications.

1.6.1 Motivation

The available IR systems described in Sec. 1.5.3 are based on either thermal or photonic principles of detection. Whereas thermal detectors like microbolometers offer low-cost CMOS-compatible integrated solutions attractive to the mainstream market, they drag on fundamental limitations on sensitivity an operational speed that make them unsuited for high-speed applications such as real-time control and monitoring of fast moving objects. Photonic detectors are not an exception: based on internal photon-electron

	Posch et al. [90]	Lv et al. [88]	Gunapala et al. [85, 86]	Peirezat et al. [81, 82]	Ilan et al. [83, 84]	Units
Pixel array	64×64	640×512	1024×1024	320×256	1920×1536	pixels
Pixel pitch	50	25	30	30	10	μm
Cryocooling-free	Yes	Yes	No	No	No	-
Packaging tech.	Monolithic	Monolithic	Hybrid	Hybrid	Hybrid	-
CMOS tech.	0.35μm 2P4M	0.5μm 2P3M	0.5μm 2P3M	0.18μm 1P6M	0.18μm	-
IR technology	a-Si μbolom.	VOx μbolom.	QWIP	HgCdTe PV	InSb PV	-
IR wavelth.	LWIR	LWIR	M/LWIR	LWIR	MWIR	-
Fill factor	69	75	50	~100	~100	%
Spectral range	8 to 15	8 to 14	4.4 to 5.1; 7.8 to 8.8	7.7 to 9.5	1 to 5.4	μm
Peak det. wavelth.	-	-	4.6; 8.4	N.A.	4.7	μm
Peak detectivity	$\sim \times 10^8$	$\sim \times 10^9$	4×10^{11}; 1×10^{11}	$\sim \times 10^{10}$	$\sim \times 10^{11}$	cm$\sqrt{\text{Hz}}$/W
Readout technique	CTIA	CTIA	DI	CTIA	DI	-
Pixel output	Digital AER	Analog	Analog	Digital 11b	Analog	-
ROIC output	Digital AER	Analog/Digital	Analog	Digital 16b	Digital 13b	-
ADC	In-pixel PDM	Col-wise PWM	None	In-pixel PDM Col-wise flash	Col-wise PWM	
In-pixel FPN cancel.	None	Offset only	None	None	None	-
Max. frame rate	30	60 (analog)	30	320	120	fps
NETD at 300K	> 1000	45	27; 40	25	25	mK
NETD×τ_{img}	N.A.	375	450; 665	40	105	mK×ms
Supply voltage	3.3	5	5	1.8	1.8	V
Static power cons.	< 1	< 1	< 1	< 1	< 1	μW/pix

Table 1.4 | Performance comparison between state-of-the-art IR vision sensors.

interactions, they are capable to exhibit fast illumination responses with bandwidths beyond the kHz range, but are commonly based on complex CMOS-uncompatible technologies and are highly sensitive to carrier generation at room temperature. As a result, external mechanisms of cooling are needed to reduce base noise levels. These are two important drawbacks that considerably pump up both cost and dimensions of commercial IR cameras, and lower their attractiveness at eyes of a wider customer niche.

Current IR imaging devices cannot cover a remarkable market gap on low-cost and portable devices for high-speed thermography applications [92–94]. Accordingly, MWIR uncooled thermal vision systems are expected to observe the highest growth rate between the period 2014 and 2020, with annual figures surpassing the 10% [15]. These imagers are particularly interesting in market sectors like:

- **Industrial:** Such as automotive, glass, metallurgy and paper. Soldering robotics and hot production temperatures in these cases allocate in the MWIR radiation, and are currently inspected using point detectors. Power generation is another example with a thermal dissipation centered on the MWIR wavelength. All the previous cases share a strong interest in incorporating affordable vision devices to avoid the generation of false alarms.

- **Environmental:** Ranging from recycling to pollution monitoring, where C-H and C-O compounds are abundant. MWIR spectroscopy has been proven to offer good sensitivity to carbon-based molecules, and has a strong potential in this area.

- **Transportation:** Railway vehicles and automobiles demand an increasing number of MWIR infrared detectors capable of monitoring the temperature of both axis and wheels, in the first case, and to prevent motor overheating and malfunctioning combustion in the second.

The monolithic combination of uncooled VPD PbSe detectors and CMOS technologies (see Sec. 1.4) stands out as an affordable uncooled solution for the MWIR spectral range of operation, opening up a broad range of kHz-thermography usages previously unreachable. Nonetheless, this novel sensing technology introduces specific design challenges both at FPA and APS levels of the system, and requires the research of precise CMOS readout circuit strategies to squeeze the potential uncooled high-sensitivity high-speed capabilities of the device.

1.6.2 R&D Context

This dissertation is set within a multidisciplinary project whose ultimate objective is to bring VPD PbSe technology to industrial applications. The whole work includes the parallel realization of the sequel research activities:

1. **Design and integration of CMOS readout electronics** for 8-inch wafer production.
2. **Technological optimization of PbSe thin-film deposition processes**, pixel pitch definition, and investigation of a compatible monolithic interface with the CMOS microelectronics.
3. **Low-cost packaging at wafer level**, involving sapphire window glueing, chip sawing, printed circuit board (PCB) assembling, wire bonding and dam & fill.
4. **Electrooptical characterization**. Definition and implementation of an electrooptical testbenches capable to characterize individual and multielement pixel sensors, for both initial detectorless prototypes and complete high-density focal planes.

The work presented in this document focuses on 1, assumes all the electrical characterization of first test vehicles in 4 and has strong dependence on the results of 2.

This thesis has been developed within the Integrated Circuits and Systems (ICAS) research group of the *Institut de Microelectrònica de Barcelona* belonging to the *Centro Nacional de Microelectrónica, Consejo Superior de Investigaciones Científicas* IMB-CNM(CSIC). Research is conceived with a strong focus on the commercial exploitation of the results as the first mainstream kHz IR quantum vision sensors operative at room temperature and monolithically integrated in standard VLSI CMOS technology. In this sense, intellectual property is covered by publications in international peer-reviewed journals, as well as conferences and patents, together with technology transfer to the industrial partner NIT S.L. in the final phase of the research. It has been partially funded with two industrial and outgoing research fellowship grant awards from *Generalitat de Catalunya* (2009-TEM-00020 and 2011-BE-DGR-00908, respectively) and has been supported by the following projects:

- **Miniaturized Infrared Detector.**

  RETIR: AEESD I+D TSI-100101-2013-101

  Partners: New Infrared Technologies (NIT) S.L., D+T Microelectrónica A.I.E.

- **IR Image Devices and Systems with High-Density Focal Plane Arrays, High-Precision Pixels and Image Read-Out Based on AER Algorithms.**

  SI2R: AVANZA I+D TSI-020100-2010-738

  Partners: New Infrared Technologies (NIT) S.L., D+T Microelectrónica A.I.E.

- **Industrial Research on High-Performance Uncooled IR Imagers for Low-Cost Civil Applications.**

  IRASE: AVANZA I+D TSI-020100-2009-004

  Partners: New Infrared Technologies (NIT) S.L., D+T Microelectrónica A.I.E.

- **A Modular and Digital CMOS Imager for Hybrid Focal Planes of IR Sensors.**

  SEADIR: DN-8835-100301006300

  Partners: Centro de Investigación y Desarrollo de la Armada - D+T Microelectrónica A.I.E.

1.6.3 Working Hypothesis

"Low-Power CMOS Digital-Pixel Imagers for High-Speed Uncooled PbSe IR Applications" supports on the hypothesis that, by the use of novel low-power mixed-signal VLSI design techniques at system and circuit levels, high-speed uncooled MWIR imagers can be monolithically integrated and validated in standard low-cost CMOS technologies. This implies fulfilling all operational requirements of the VPD PbSe detector in terms of connectivity, reliability, functionality and scalability for its use in industrial applications.

In order to achieve the aforementioned demands, this thesis proposes null inter-pixel crosstalk vision sensor architectures based on a digital-only FPA of configurable DPSs. Each DPS cell is equipped with fast communication modules, self-biasing, offset cancellation, ADC and FPN correction. In-pixel power consumption is minimized by the exploitation of comprehensive MOSFET subthreshold operation [95–97], while compact pitch is achieved by circuit reuse and dynamic bandwidth allocation.

This work aims to potentiate the integration of PbSe-based sensing technologies so as to widen its use, not only in distinct MWIR vision scenarios, but also at different stages of PbSe-CMOS integration maturity. For this purpose, we posit to investigate a comprehensive set of functional blocks distributed in two parallel approaches:

- **Frame-based "Smart" imaging** with full DR adjustment and FPN correction capabilities. This research line takes advantage of current limitations on detector-pitch reduction to enhance image NETD by offering full programmability at pixel level and complete functionality in terms of input parasitic capacitance compensation, frame memory and local bias generation.

- **Frame-free "Compact"-pitch vision** based on an event-driven architecture, keeping pixel output in the digital but continous-time domain. This strategy is conceived to obtain extensive pitch compaction and readout speed increase by the suppression of in-pixel digital filtering, and the use of dynamic bandwidth allocation in each element of the FPA.

Whereas frame-based Smart imagers pursue delivering a contemporary robust solution to maximize video performance in first industrial prototypes, frame-free Compact-pitch sensors explore new fully-asynchronous vision paradigms in order to exploit detector bandwidth and reduce readout area requirements as the PbSe technology matures.

1.6.4 The Challenges

Achieving good operational performance in monolithic PbSe-CMOS focal planes poses specific technological challenges on readout functionality, prototype characterization and design for manufacturing that needed to be overcome along the work. On the VPD PbSe post-processing side, two key technological bottlenecks emerge as critical: procuring good compatibility and yield between detector and VLSI materials at their interface, and defining proper temperature and duration in each post-processing step so as to avoid CMOS operational drifts caused by PbSe sensitization treatments. These tasks were performed by NIT S.L. and are out of the scope of this thesis. From the CMOS circuit viewpoint, and besides satisfying readout needs, research activities were adapted to be performed in parallel with the development of the detector and independently of one another during first prototype, die-level designs.

The main challenge of this project is to conceive, design and integrate ROIC architectures that consume very low power, operate at kHz frequencies, exhibit good uniformity and fit in the compact pitch of the focal plane, all while addressing the particular characteristics of the MWIR detector:

1. **High dark-to-signal ratios.** PbSe detectors deliver dark-to-signal current ratios strongly higher than those from the rest of quantum light sensing technologies (typically orders of magnitude below unity). As a result, a direct cancellation mechanism of this process, voltage and temperature (PVT)-dependent large offset current is needed inside each APS, which is not covered by the existing background suppression techniques [98, 50].

2. **Large input parasitic capacitance values.** The large parasitic capacitance of the post-processed PbSe detector can limit signal band-

width in case of using it as the pixel integration capacitor. Hence, in-pixel CTIAs [49, 99, 54, 100] are required in practice to exploit the high-speed capabilities of PbSe detectors.

3. **Mismatch on PbSe deposition.** Due to the nature of VPD post-processing, fixed pattern noise plays an important role on the response of PbSe FPAs. In consequence, both offset (dark current) and gain (responsivity) corrections are also needed inside each pixel sensor. A solution for this double compensation is not addressed by the available FPN reduction approaches [49, 53, 101, 48, 70, 55].

The latter implies including additional functionality to the CMOS designs without exceeding the area-power trade-off. Sub-μpower operation is mandatory for the CMOS pixel circuits to minimize thermal effects on the uncooled MWIR detector stacked on top of the APS cells. The quality of the solutions will dictate the ultimate success of the novel IR cameras.

Apart from the primary design challenges pointed above, the presented work also has to fare the following bottlenecks:

- **Detectorless prototype validation.** The MWIR PbSe detector technology employed in this thesis is only accessible after VPD post-processing at wafer level. Unfortunately, full wafer implementations are not typically available until the engineering run stage, long after the integration of first ROIC prototypes. Pixel validation is, nevertheless, an essential milestone in preliminary vision sensor designs. This translates in fact into extending the research to add complementary coverage on affordable sensor emulation strategies and integrated test platforms. Such devices should be effective in terms of providing precise quantitative control of the photogenerated-alike input current in detectorless pixel test matrices. They should also offer good accuracy so as to permit the automation of the previous values.

- **Design for manufacturing.** As already commented in preceding chapters, all research efforts converge to one final aim: obtaining a commercial monolithic device reliable enough to exhibit good performance in actual usages. All integrated circuits (ICs) that face this last stage must meet the strict material coverage, spacing, width and vias requirements of an engineering run. In our particular case, and according to foundry recommendations, design rules for high-stress environments had to be observed in order to safeguard circuit designs from later thermal treatments during PbSe deposition.

1.6.5 Methodology and Contents

The frame-based and frame-free worklines of Sec. 1.6.3 have been investigated according to a top-down modular VLSI design approach. First efforts centered on exploring focal plane and DPS architectures from a functional viewpoint. Departing from state-of-the-art CMOS vision sensor techniques, the new low-power circuit topologies detailed in Chapter 2 and 3 were elaborated so as to meet the specific objectives of this dissertation. In this sense, ROIC design activities trail the design flow of Fig. 1.14. General ROIC architecture essays are run under Matlab; integrated circuit design is performed under the Cadence IC front-backend environment. The complete project is structured according to an inter-dependent high-level/low-level research open to cyclic iteration depending on the outcomes achieved at the end of each task.

In this process, initial Matlab numerical simulations evaluate prior readout architectural candidates. The selected optimal strategies are then translated into electrical circuits, and refined in their basic device parameters using accurate analog low-power MOSFET analytical expressions (i.e. the EKV model [96]). All circuit variables are fine-tuned exploiting the electronic design automation (EDA) capabilities of the Cadence Virtuoso suite: Mismatch effects are carefully evaluated through Montecarlo analyses, and overall system functionality secured for critical temperature and process corners. Next step involves full custom layout design, extraction and layout versus schematic (LVS). Main efforts during physical implementation are directed towards reducing device mismatch, delivering proper A/D isolation, and improving low and top-level power line routing [102]. A final post-layout simulation takes into consideration any additional parasitic effects. If the resulting behavior is under specs, the circuit is redefined to take into account the previously uncovered second order effects. Electrical simulations, physical design and extraction support on accurate technological data and models. The characteristics of the detector are supplied by direct partnership with NIT S.L.; CMOS design information is provided as process design kit (PDK) by the CMOS foundries manufacturing the ICs.

The electrical design phase of every work package is divided into successive CMOS prototyping, test and upgrade rounds to be executed until the desired performance is met. Each cycle is not only limited by internal engineering time, but also notably influenced by foundry calendars, along with project funding and scheduling. This stage is conceived hierarchically: every block is split into subcircuits depending on its functionality, and the latter divided into basic structures composed of a limited number of transistors. Hence, both design and simulation are simplified, shortening the localization of possible system issues. The computational requirements of complex focal plane automated analyses are lowered combining analog and mixed-signal Verilog-AMS simulations.

Many differences reveal between Smart and Compact-pitch pixel sensor proposals. Because the complexity of the former resides in the DPS itself, the cell requires at least of one electrical demonstrator for later improvement and redesign. Once the frame-based DPSs satisfy electrical requirements, next step is devoted to full FPA integration and PbSe post-processing for succeeding electrooptical evaluation. In contrast, a big part of the engineering efforts of the latter frame-free proposal point to overall architecture development. Therefore, its schedule plans simultaneous DPS/FPA prototyping and evaluation through simple electrical test arrays. The characterization of this device requires also the use of special hardware such as high-speed event-driven interfaces and VLSI platforms fabricated in house, and constitutes the major exposure of the research. If successful, a succeeding run pursues electrooptical validation of the full PbSe-CMOS vision system.

The outcomes of these research activities are detailed in the nearing chapters. Chapter 2 and 3 describe the architecture, operation, and CMOS implementation of the functional blocks conceived for both frame-based and frame-free approaches. Chapters 4 and 5 recount the DPS cells, imagers and test plaforms that have been integrated in 0.35μm 2P4M, 0.15μm 1P6M and 2.5μm 2P1M CMOS technologies, respectively. These same chapters also enumerate the experiments (e.g. pixel response, analog memory retention, individual programmability, crosstalk) that were carried out on each design library, presenting statistical results and showing practical operation examples. All pilot chips included mechanisms for IR detector current emulation and single/matricial DPS testing, and were evaluated at in-house electrical characterization laboratories. Electrooptical trials were performed collaboratively at NIT S.L. facilities. Every IC update started with a common revision of system specs and concluded with bilateral technical reports. The final contributions of this dissertation are discussed in Chapter 6, in view of potential future unfolding in the field.

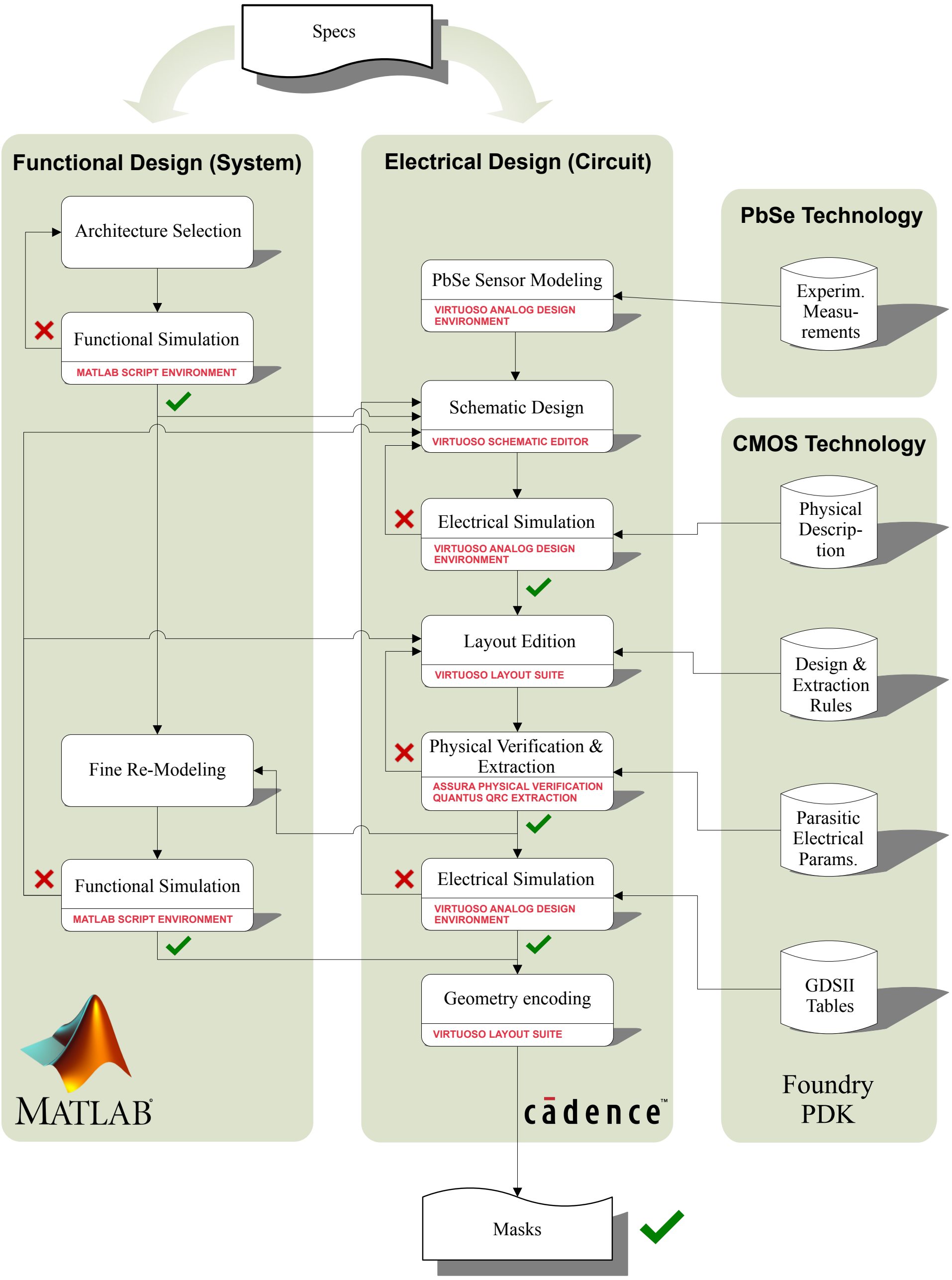

Specs
Functional Design (System)
Architecture Selection
Functional Simulation
MATLAB SCRIPT ENVIRONMENT
Fine Re-Modeling
Functional Simulation
MATLAB SCRIPT ENVIRONMENT
MATLAB
Electrical Design (Circuit)
PbSe Sensor Modeling
VIRTUOSO ANALOG DESIGN ENVIRONMENT
Schematic Design
VIRTUOSO SCHEMATIC EDITOR
Electrical Simulation
VIRTUOSO ANALOG DESIGN ENVIRONMENT
Layout Edition
VIRTUOSO LAYOUT SUITE
Physical Verification & Extraction
ASSURA PHYSICAL VERIFICATION
QUANTUS QRC EXTRACTION
Electrical Simulation
VIRTUOSO ANALOG DESIGN ENVIRONMENT
Geometry encoding
VIRTUOSO LAYOUT SUITE
cādence
PbSe Technology
Experim. Measurements
CMOS Technology
Physical Description
Design & Extraction Rules
Parasitic Electrical Params.
GDSII Tables
Foundry PDK
Masks

Figure 1.14 | Full-custom ASIC EDA design flow used in this work.

Frame-Based Smart IR Imagers

2

2.1 Imager Architecture and Operation Proposal

The Smart imager approach depicted in Fig. 2.1 is conceived to exploit the pitch limitations of first VPD PbSe detector designs so as to minimize power density, and enhance both dynamic range and NETD$\times\tau_{img}$ metrics of Sec. 1.2. This architecture optimizes such figures by developing high-end digital pixel sensors with the following in-pixel functionality:

- Local biasing generation
- Detector dark current (i.e. offset) cancellation
- Detector parasitic capacitance compensation
- Integrating A/D conversion
- Gain tuning of the ADC
- Fixed pattern noise suppression
- Digital frame memory
- Digital-only I/O interface

to address the particular system requirements highlighted in Sec. 1.6.4. These constraints are specially demanding at the first stages of camera development, when VPD PbSe detection technology is not yet mature.

The vast majority of image sensor architectures reviewed in Sec. 1.5.2 distribute pixel bias, digital control, row/column decoding and/or ADC outside the focal plane [48–50, 55, 54, 53]. The proposed readout architecture of Fig. 2.1 follows the trend of Sec. 1.5.1 optimizing noise performance by implementing a digital-only I/O interface with full in-pixel A/D conversion. In this scheme, all analog buses are replaced by the serial concatenation of DPS cells for the purpose of digitally programming-in and reading-out each pixel row simultaneously. As a result, σ^2_{MUX} and σ^2_{drv} contributions are automatically removed from (1.3) while providing the ADC noise bandwidth benefits of DPS-based imager architectures; connectivity requirements for CMOS technology are more relaxed, noise contributions to the readout chain are reduced and inter-pixel crosstalk is dissolved.

The PbSe quantum detector described in Sec. 1.4 is accessed by deposition on top of the CMOS array to perform photoconductive transduction of MWIR radiation. All pixels in the FPA are grouped and accessed by rows, and operated according to the two modes of Fig. 2.2(b): acquisition or communication. In the first case, the input blocks of Fig. 2.1(c) compensate C_{det} and the DC dark current (I_{dark}). The resulting effective input current I_{eff}, ideally proportional to the incoming IR power, can be codified by the spike-counting ADC (i.e. $\mathtt{d_{ADC}}$) and stored in the digital I/O block in order to deliver fast and high-SNR output video frame sequences. During the communication phase, the same digital block is reconfigured to allow the simultaneous serial readout of the IR sample with the alternate programming-in of both I_{dark} and the gain of the ADC as $\mathtt{d_{DAC}}$, the latter by use of the `cal` signal. Thus, offset and gain correction maps are globally written-in through the bus of row inputs and FPN-compensated frames are read out through the bus of row outputs. These two parameters can be configured in every pixel ($\mathtt{q_{in}}$) at a resolution as high as the output frame code is read ($\mathtt{q_{out}}$). Hence, both technology-dependent spatial noise and dynamic range on output images can be improved in real-time and without noticeable speed costs.

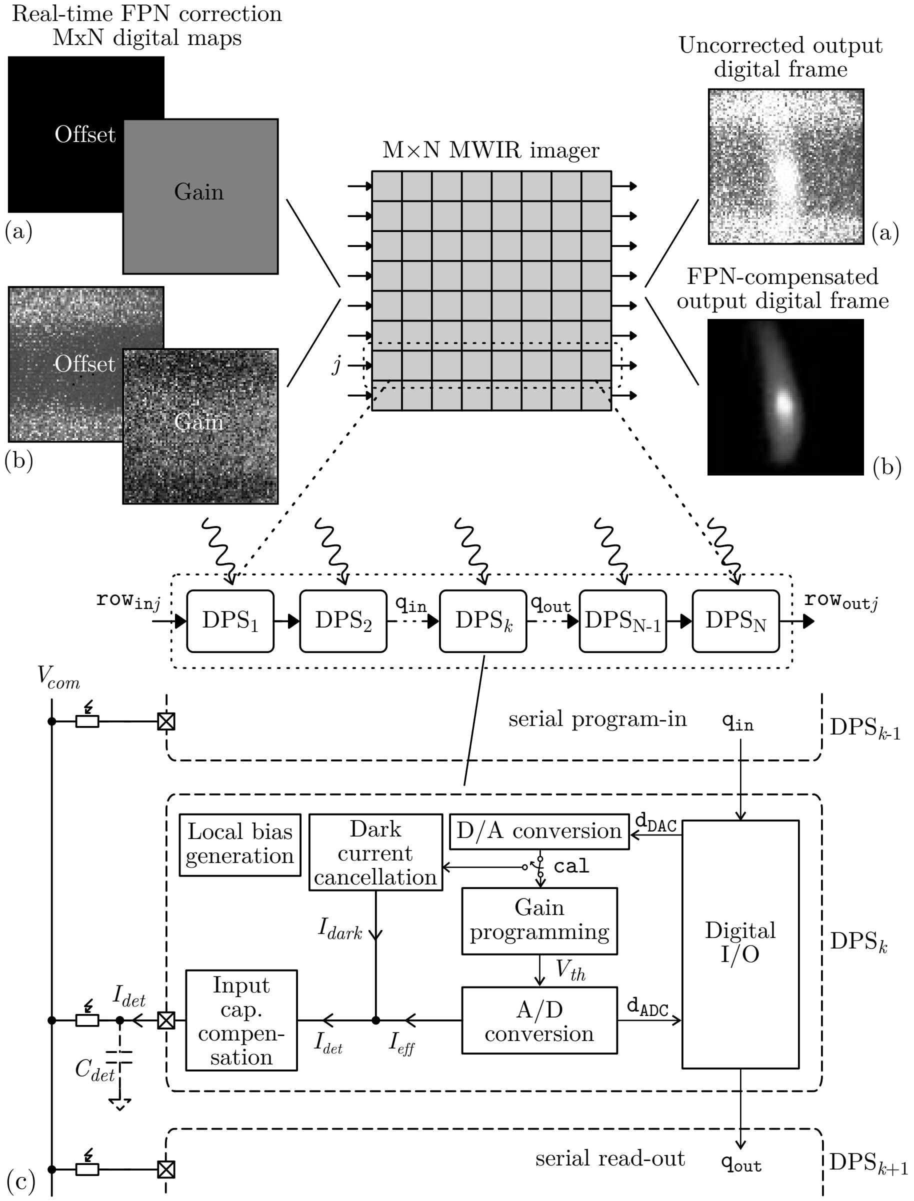

Real-time FPN correction
MxN digital maps
Offset
Gain
(a)
Offset
Gain
(b)
M×N MWIR imager
j
Uncorrected output
digital frame
(a)
FPN-compensated
output digital frame
(b)
row_inj
DPS1
DPS2
q_in
DPSk
q_out
DPSN-1
DPSN
row_outj
Vcom
serial program-in
q_in
DPSk-1
Local bias
generation
Dark
current
cancellation
D/A conversion
d_DAC
cal
Gain
programming
Idark
Vth
Digital
I/O
DPSk
Idet
Input
cap.
compen-
sation
Idet
Ieff
A/D
conversion
d_ADC
Cdet
serial read-out
q_out
DPSk+1
(c)

Figure 2.1 Frame-based IR imager proposal. Practical examples of raw imaging under no FPN compensation (a) and in-pixel FPN-corrected aquisition (b). General DPS architecture (c). Figure not in scale.

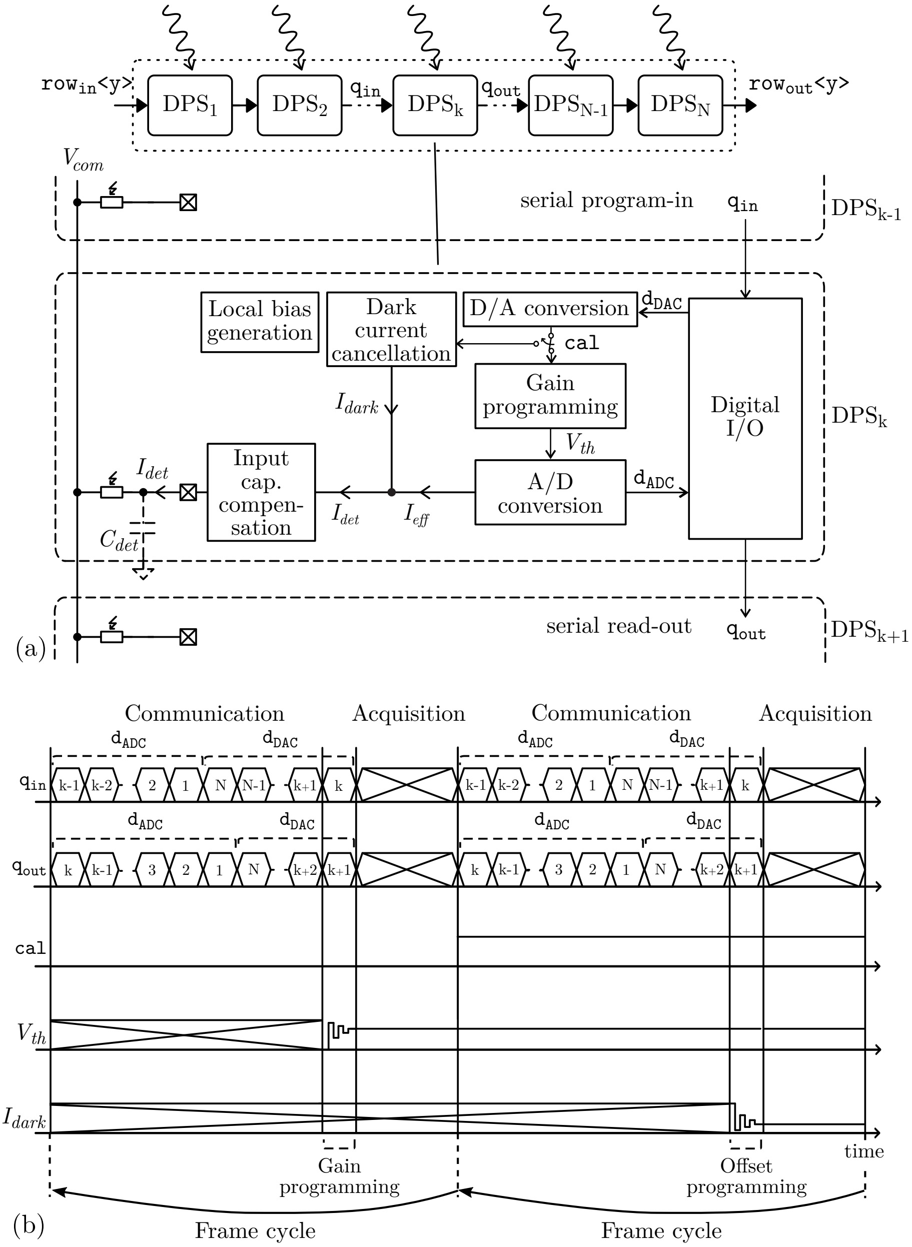

row_in<y>
DPS1
DPS2
q_in
DPSk
q_out
DPSN-1
DPSN
row_out<y>
Vcom
serial program-in
q_in
DPSk-1
Local bias generation
Dark current cancellation
D/A conversion
d_DAC
cal
Gain programming
Digital I/O
DPSk
I_dark
V_th
I_det
Input cap. compen-sation
A/D conversion
d_ADC
I_det
I_eff
C_det
serial read-out
q_out
DPSk+1
(a)
Communication
Acquisition
Communication
Acquisition
d_ADC
d_DAC
q_in
k-1
k-2
2
1
N
N-1
k+1
k
q_out
k
k-1
3
2
1
N
k+2
k+1
cal
V_th
I_dark
Gain programming
Offset programming
time
Frame cycle
Frame cycle
(b)

Figure 2.2 | Frame-based Smart IR imager operation. General DPS architecture (a) and operational chronogram (b).

Under this scheme, no clock is generated during the acquisition and asynchronous A/D conversion phase. This last factor is key to reduce switching noise inside active pixels. Fig. 2.1 also shows a practical scenario of complete offset and gain tuning with in-pixel FPN compensation. A frame set with no offset compensation and a common medium gain value for the entire focal plane could exhibit the visual noise of Fig. 2.1(a). Appropriate individual pixel calibration would significantly optimize image generation as depicted in Fig. 2.1(b). Apart from attenuating detector and CMOS FPN along the focal plane, offset programming circuitry allows to boost the number of effective photogenerated carriers integrated in acquisition, and provides additional NETD enhancement according to (1.3) and (1.12).

2.2 All-Digital Program-In and Read-Out Interface

2.2.1 Motivation and Design Proposal

Traditional scanning and/or encoding proposals such as the examples [56, 60, 61] cited in Sec. 1.5.2 are grouped at either row or column levels to operate at the periphery of the focal plane. In contrast, the system architecture pursued in this first research line embeds all functionality inside the pixel itself. Hence, it requires of a compact digital interface able to configure each pixel individually, as well as integrating and storing its internal signal conversion at the minimum time and operational complexity costs.

LFSR Based Interface

An interesting solution for the reconfigurable digital interface of Fig. 2.1 are linear-feedback shift registers (LFSRs) [103, 104], as they can implement both data shifting and pseudo-random counting functionalities by the addition of a few multiplexers at their inputs. Fig. 2.3 illustrates a feedback example for a 15-bit register with feedback polynomial $x^{14}+x^{13}$, which exhibits maximum-length sequence (MLS) [105]. In this particular case, the MLS topology ensures that each binary code is generated exactly once during a complete cycle except for the ‘0...0’ case. Therefore, it almost exploits the full output range of a classic counter.

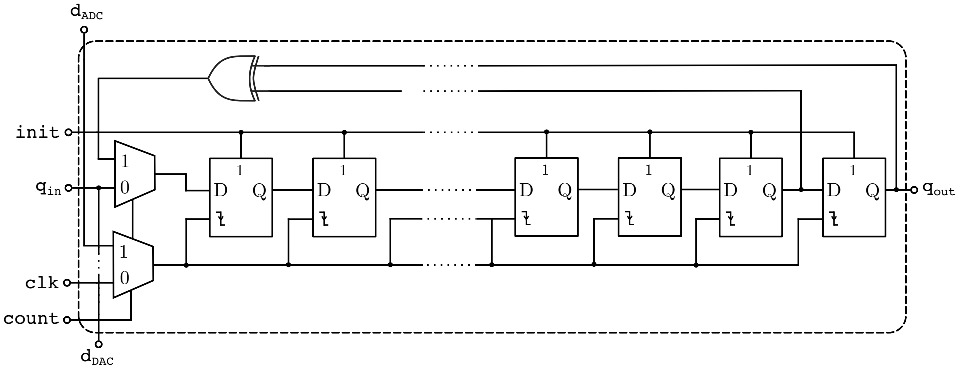


Figure 2.3 General scheme of a 15-bit LFSR reconfigurable counter with MLS feedback polynomial for the digital I/O interface of Fig. 2.1. When low, control signal `count` fixes the module to behave as a shift register.

LFSR implementations suffer, nonetheless, of a significant drawback: decoding their pseudo-random codes commonly requires of an additional look-up table (LUT), which may become a practical bottleneck in large dynamic range or high-speed imagers. This fact adds up to the higher number of binary transitions each flip-flop output has compared to conventional ripple counting devices. The latter is directly related with the dynamic power consumption of the digital part and facilitates the induction of crosstalk to the analog parts of the active pixel.

Ripple-Counter Based Interface

Fig. 2.4 depicts the digital scheme posit to avoid such effects. As in Fig. 2.3, the modular circuit of Fig. 2.4(a) saves in-pixel Si area by reconfiguring its D-type flip-flop core blocks according to the two operational modes of the imager. When in communication (`count` = 0), a synchronous scanning path is implemented through the shift register of Fig. 2.4(b), which in turn connects all the DPS cells along the rows of the focal plane. Internal counting and storing of pulses is performed in acquisition (`count` = 1). Fig. 2.4(c) shows how all flip-flops are reconfigured as T-type cells, in this period, for the asynchronous operation of the digital integrator.

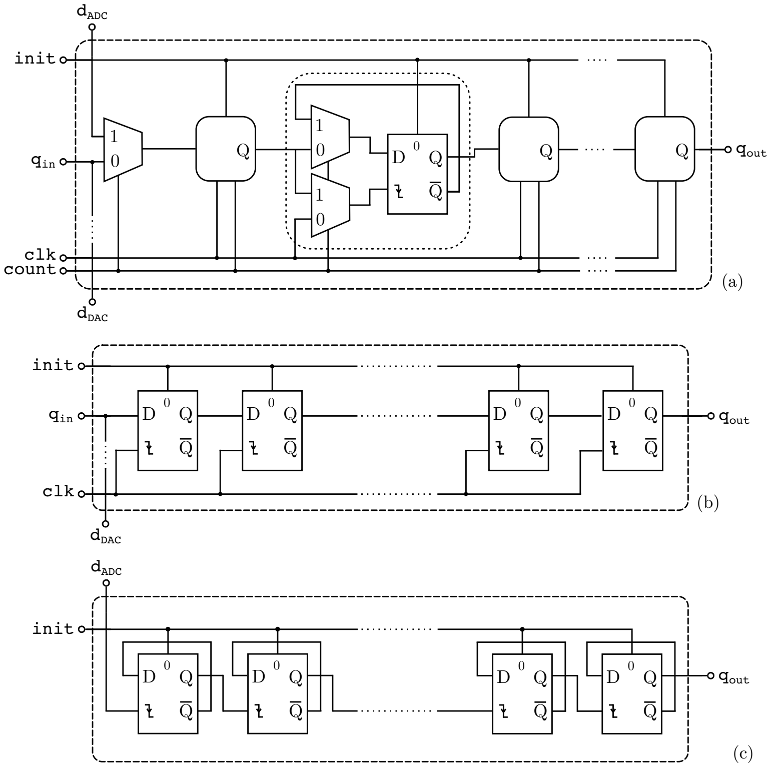

d_ADC
init
q_in
clk
count
d_DAC
1
0
Q
D
0
Q
Q̄
q_out
(a)
init
q_in
clk
d_DAC
D
Q
Q̄
q_out
(b)
d_ADC
init
D
Q
Q̄
q_out
(c)

Figure 2.4 Reconfigurable digital I/O interface scheme proposal for the DPS of Fig. 2.1(a). Internal configuration for communication (b) and acquisition (c).

Fig. 2.5 compares ripple and pseudo-random maximum length sequence (PRMLS) counters in terms of their number of transitions at full scale and the number of extra metal-oxide semiconductor (MOS) devices required for their reuse as I/O scanning path. The latter remains stable and low in PRMLS-based interfaces, a noteworthy aspect to be exploited in compact pixel designs. On the other hand, its power consumption shoots up to more than twice the one exhibited by the alternative ripple version for 7 to 15-bit design cases.

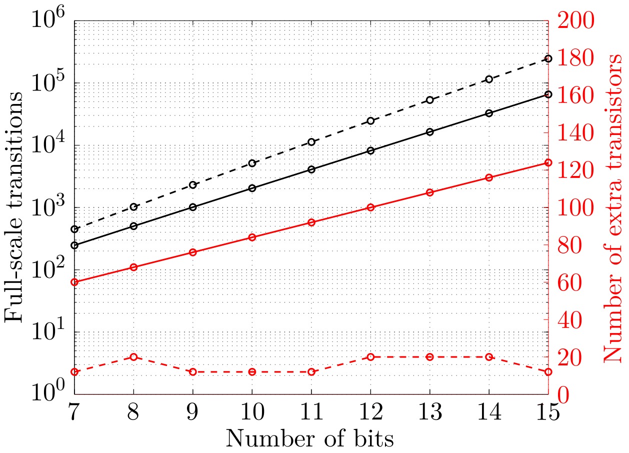


Figure 2.5 Full-scale transitions (black) and additional transistors (red) in reconfigurable ripple (solid line) and PRMLS (dashed line) counters. Values for 7 to 15-bit design cases.

2.2.2 Compact CMOS Implementation

LFSR Based Interface

The digital LFSR I/O interface of Fig. 2.6(a) exploits the compactness of this strategy by including up to 15 unitary register cells, where MLS feedback uses only the last two most significant bit (MSB) outputs. This additive feedback is brought by means of a static XOR gate and dual-transmission-gate multiplexers. All MOS devices appearing in the figures that follow have their bulk terminals connected to ground and supply voltages, respectively, depending on whether they are N or PMOS devices. Provided `count` signal is low, all flip-flops serially read input data from their precedent cell; turning this signal high connects the input of the least significant bit (LSB) flip-flop to the output of the XOR logic. In the first case (communication), all D-type cells enter the data synchronously with the `clk`, and each input bit $\mathtt{d}_{\mathtt{DAC}}$ of the in-pixel digital-to-analog converter (DAC) is directly input from $\mathtt{q}_{\mathtt{in}}$. Configuration for acquisition ties all transitions to pulse generation at $\mathtt{d}_{\mathtt{ADC}}$.

To ensure proper counting, an starting minimum 0x4000 word value is fixed by initializing all but the MSB flip-flop to ‘0’ ($\overline{\texttt{reset}}$ signal), and this remaining cell to ‘1’ (`set` input). These two flip-flops are depicted in Fig. 2.6(b-c). Concerning the unwanted cyclic operation of the counter, this effect is avoided by the inclusion of a highest-code, overflow detector. Such functionality can be executed by either an extra overflow register, the use of classical static logic AND function along 1-bit register outputs, or local detection by the distribution of a serial pull-up/down at each one of these outputs in the digital block. This last alternative was finally adopted as optimum in terms of area for an expected maximum bit length of 15 bit for both LFSR and ripple-based I/O interfaces. The active-high `ovflw` signal disables acquisition by stopping pulse modulation once full scale is reached.

Ripple-Counter Based Interface

Fig. 2.7(b) shows the CMOS implementation of each unitary register of the ripple-counter based digital block, together with the internal signal multiplexation (c) employed to operate the two modes of the device. During digital integration `count` is set to ‘1’ and the biestable operates as an asynchronous T-type flip-flop triggered either by the $\texttt{d}_{\texttt{ADC}}$ falling edge - in case to be the LSB bit - or by the output bit of the previous flip-flop. When `count` is ‘0’, serial communication flows through the now D-type flip-flops synchronized with the falling edge of `clk`. Like in the previous LFSR scheme, $\texttt{d}_{\texttt{DAC}}$ is also straightly supplied from $\texttt{q}_{\texttt{in}}$. In order to avoid undesired transitions, the clock signal must rest low after the last communication period and return to high immediately before the next scan.

Both configurations use the same basic master-slave topology of Fig. 2.7(b). Asynchronous count operation significantly optimizes the area requirements of T-type flip-flop cells. Again, a standard NAND initialization gate is used to reset the module. Such parallel reset mechanism speeds up the process by forcing a high output value to all master latches independently to its current output state. As a rule of thumb to reduce both area and power consumption the entire block but the output inverter can be implemented with minimum W-L gates. Overflows are caught through the PMOS pull-up structure of Fig. 2.7(a).

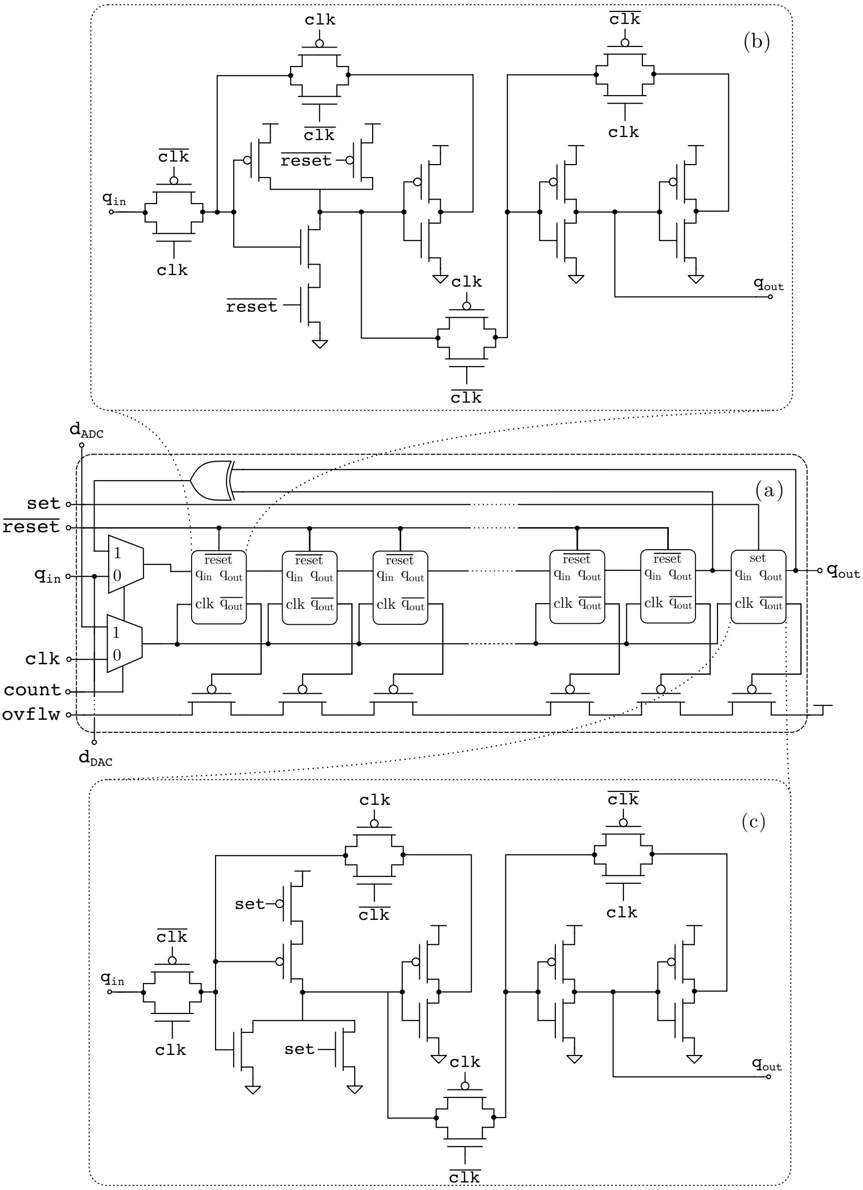

clk
clk
(b)
clk
clk
reset
clk
q_in
clk
clk
reset
q_out
clk
d_ADC
set
reset
(a)
q_in
clk
count
ovflw
1
0
1
0
reset
q_in q_out
clk q_out
set
q_out
d_DAC
clk
clk
(c)
set
clk
clk
q_in
clk
set
clk
q_out
clk

Figure 2.6 Reconfigurable basic building block of the LFSR-based I/O interface with overflow detection (a). CMOS implementation of each bit register, with external initialization of type reset (b) and set (c).

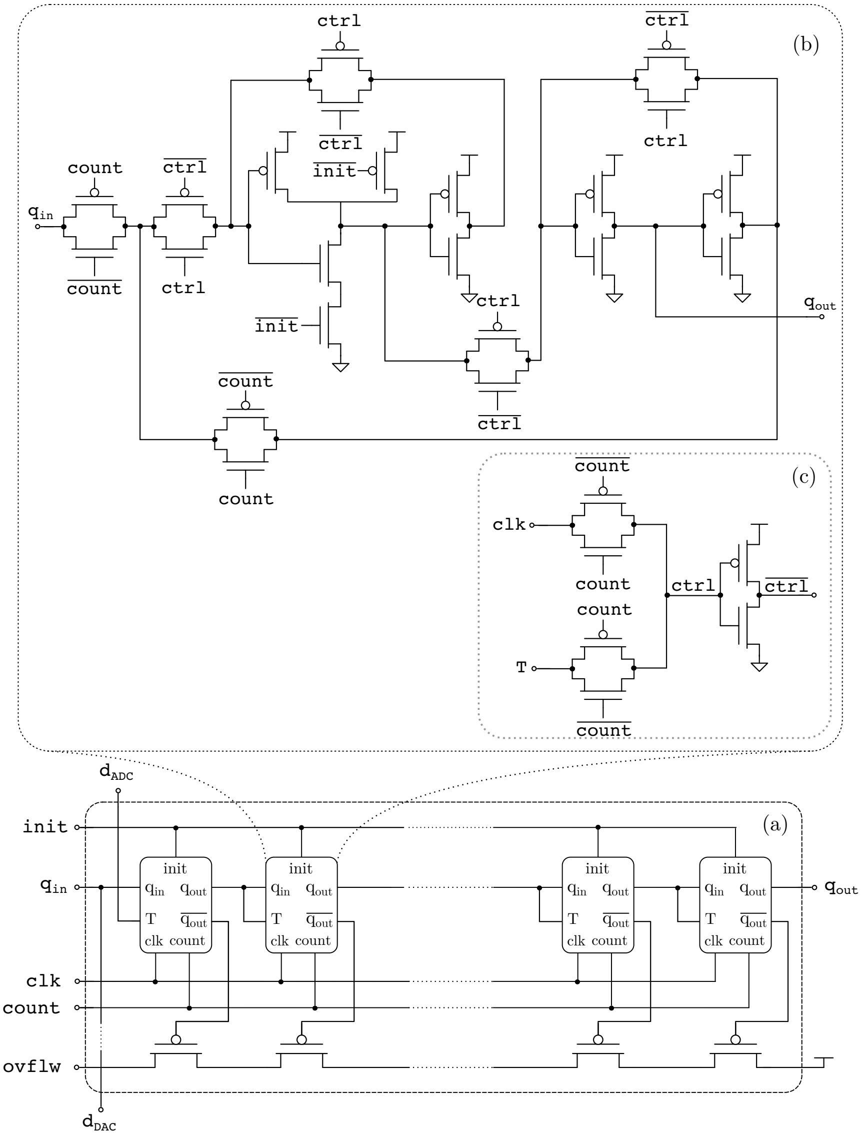

(b)
ctrl
$\overline{\text{ctrl}}$
count
$\overline{\text{count}}$
$\overline{\text{init}}$
q_{in}
q_{out}
(c)
clk
T
(a)
init
d_{ADC}
q_{in}
q_{out}
$\overline{q_{out}}$
clk
count
ovflw
d_{DAC}

Figure 2.7 Reconfigurable basic building block of the ripple-counter based I/O interface with overflow detection (a). CMOS implementation of each bit register (b) and signal multiplexing for T-like functionality (c).

2.3 Input Signal Conditioning

2.3.1 Motivation and Design Proposal

The input stage of the DPS is devoted to overcome two of the main PbSe-related challenges pinpointed in Sec. 1.6.4: its large capacitance values and high dark-to-effective signal ratios. As current-mode input circuit, total system bandwidth can be severely limited by the PbSe detector capacitance. Charge losses through C_{det} would impose the use of generous integrating capacitance C_{int} and/or gain values. Even in the case that this capacitance was considerably smaller than C_{int}, its finite output resistance may distort integration in the presence of induced voltage variations at the input node. Potential at this contact pad must be kept stable so as to avoid any signal leakage through the PVT-reliant detector output impedance, and allow for more-capacitive hybridization procedures in pro to increase the dimensions of the focal plane. For such task the transconductance of Fig. 2.8(b) is proposed, whose negative feedback loop nulls input impedance and fixes zero input voltage to bias the IR detector differentially to -V_{com}.

With respect to detector dark current, this variable is treated as a DC component since its spectrum falls clearly behind the kHz operating frequency of the DPS. Because its value depends on PVT effects, it can be seen in practice as an offset FPN that must be cancelled in order to maximize the SNR (1.6) and NETD (1.12) performance of the imager. A high resolution cancellation is needed in practice to subtract μA-range I_{dark} to I_{eff} currents as low as nA. This restrictive specification automatically discards detector-current copier topologies sensitive to technology mismatching [91, 88], forcing direct I_{dark} subtraction to be achieved by the controlled current source of Fig. 2.8(a) afore integration.

2.3.2 Compact CMOS Implementation

Parasitic Capacitance Compensation

The CMOS input capacitance compensation circuit is implemented through the OpAmp negative-feedback topology of Fig. 2.9. In this circuit, the DPS

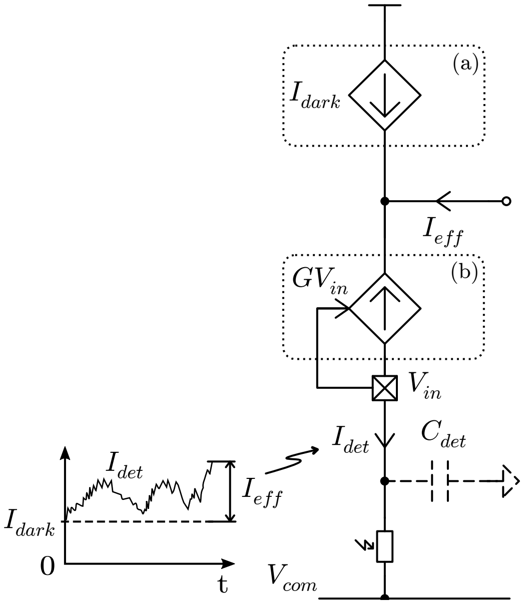


Figure 2.8 Linear model of the DPS input stage proposal with dark current cancellation (a) and input capacitance compensation (b) for the frame-based Smart imager of Fig. 2.1.

input impedance is basically controlled by M5 together with its active regulated control M1-M4. With proper matching between M3-M5 devices, the latter differential amplification stage offers wide dynamic range with minimum area requirements. Furthermore, the low-voltage gain contribution of the M5 stage to the loop transfer function avoids the necessity of any frequency compensation capacitor.

According to the Enz-Krummenacher-Vittoz (EKV) small signal model [96], the transfer function of the amplifier is

$$\frac{v_{oa}}{v_{in}} \simeq g_{mg_{1,2}} \left(r_{01,2} \parallel r_{03,4} \right) = \frac{g_{mg_{1,2}}}{g_{md1,2} + g_{md3,4}} \tag{2.1}$$

Neglecting channel-length modulation in M5 thanks to the low input impedance

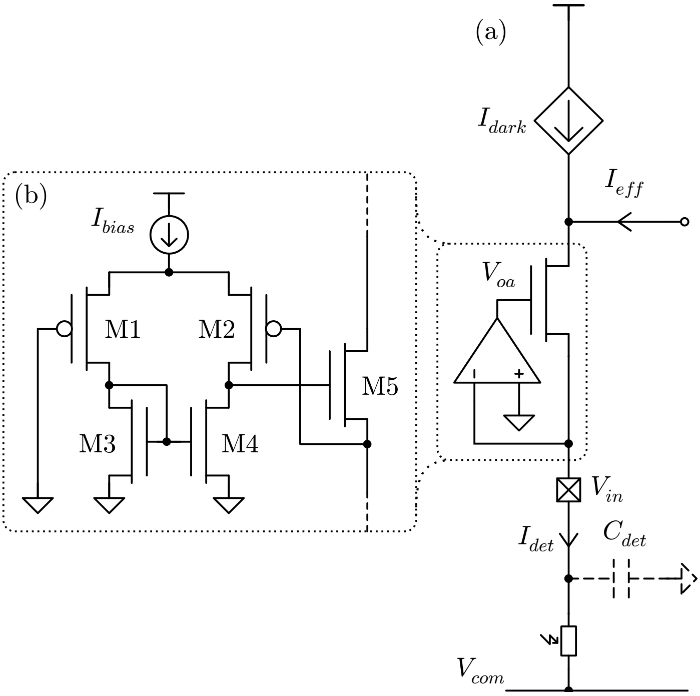

(a)
I_{dark}
I_{eff}
(b)
I_{bias}
M1
M2
M5
M3
M4
V_{oa}
-
+
V_{in}
I_{det}
C_{det}
V_{com}

Figure 2.9 DPS parasitic capacitance compensation circuit (a) and detailed CMOS implementation for Fig. 2.8(b).

of the current-ADC of Fig. 2.1, I_{det} can be expressed as

$$i_{det} \simeq g_{mg_5} \left(v_{oa} - n_N v_{in}\right) \tag{2.2}$$

where n_N is the n-channel metal-oxide-semiconductor (NMOS) subthreshold slope. The equivalent input resistance is then

$$r_{in} = -\frac{v_{in}}{i_{det}} \simeq \frac{1}{g_{mg_5}\left(\frac{g_{mg_{1,2}}}{g_{md_{1,2}}+g_{md_{3,4}}} + n_N\right)} \tag{2.3}$$

Simplifying for all devices operating in weak inversion saturation:

$$r_{in} \simeq \frac{g_{md1,2} + g_{md3,4}}{g_{mg5} g_{mg1,2}} \simeq \frac{n_N n_P U_t^2}{I_{det}} \left(\lambda_N + \lambda_P \right), \qquad \frac{g_{mg1,2}}{g_{md1,2} + g_{md3,4}} \gg 1 \tag{2.4}$$

where n_P, U_t and λ stand for the PMOS subthreshold slope, the thermal potential and the channel length modulation, respectively. In practice, resistance values below kΩ can be easily obtained, increasing the upper limit of C_{det} above several pF to satisfy the PbSe detector bandwidth of Fig. 1.6(b).

Offset cancellation

Fig. 2.10 schematizes the two offset cancellation approaches studied in this work: In (a) offset compensation is auto-adjusted to an internally measured detector dark current; (b) takes advantage of in-pixel I/O digital interface to allow for an external tuning of this value. In practice, offset analog self-calibration is achieved by the switched current (SI) copier as depicted in Fig. 2.11: during calibration (`cal` $= 1$ and no IR radiation) I_{dark} is sampled and dynamically stored in the M1 non-linear gate capacitance C_{dark}; this same I_{dark} is subtracted along acquisition (`cal` $= 0$). Such a circuit presents the advantage to be completely insensitive to technology mismatching, since the same M1 device performs both memorization and cancellation tasks. In order to improve the output impedance of the SI copier, the cascode M2-M4 of Fig. 2.11(a) is added.

The regulated cascode M2-M3 of Fig. 2.11(b) presents a wider dynamic range variant of the same concept. Its operation procedure can be easily understood referring to Fig. 2.11(b) and Fig. 2.15. Low bias currents force M3 (Fig. 2.11(b)) and M1 (Fig. 2.15) to operate in weak inversion forward saturation. Thus, M2 drain-to-source voltage can be expressed as

$$V_{DS2} = \left[V_{DD} - n_P U_t \ln\left(\frac{I_{bias}}{I_{S3}} \right) \right] - \left[V_{DD} - n_P U_t \ln\left(\frac{I_{bias}}{I_{S1}} \right) \right], \quad I_S = 2 n_N \beta U_t^2 \tag{2.5}$$

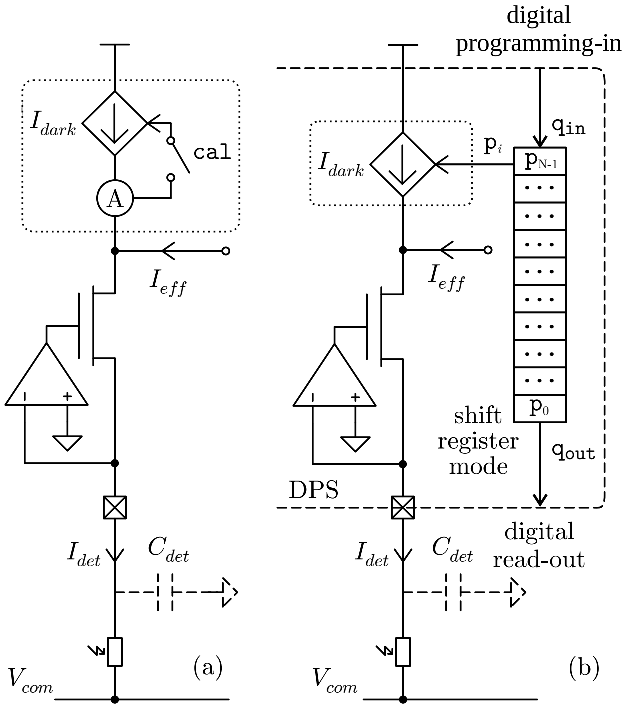

digital
programming-in
I_{dark}
cal
A
I_{eff}
q_{in}
p_i
I_{dark}
p_{N-1}
p_0
I_{eff}
shift
register
mode
q_{out}
DPS
I_{det}
C_{det}
I_{det}
C_{det}
digital
read-out
V_{com}
(a)
V_{com}
(b)

Figure 2.10 DPS offset cancellation schemes: analog self-calibration (a) and digital external tuning (b).

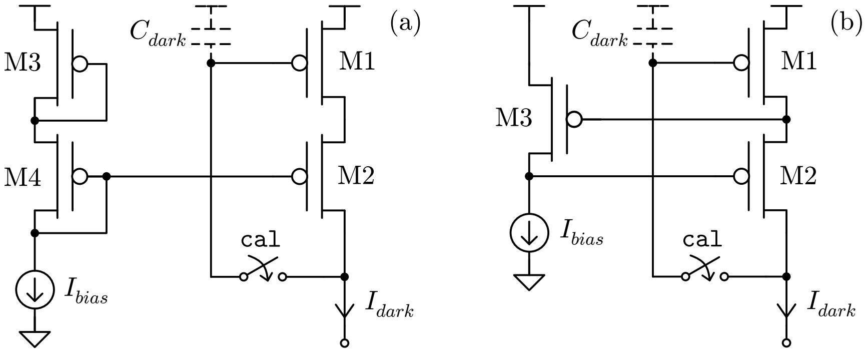

M3
C_{dark}
(a)
M1
M4
M2
cal
I_{bias}
I_{dark}
C_{dark}
(b)
M1
M3
M2
I_{bias}
cal
I_{dark}

Figure 2.11 CMOS circuit implementation of the DPS offset self-calibration scheme of Fig. 2.10 with simple (a) and regulated (b) cascode toppologies.

where V_{DD}, I_S and β stand for the supply voltage, the specific current and the current factor, respectively. Simplifying:

$$V_{DS2} = n_P U_t \ln\left(\frac{I_{S3}}{I_{S1}}\right) \tag{2.6}$$

Provided that M2 operates close to subthreshold, saturation ($V_{DS2} > 3(5)U_t$) is achieved by proper transistor dimensioning:

$$(W/L)_3 > e^{\frac{3(5)}{n_P}}\,(W/L)_1 \simeq 10(50)\,(W/L)_1\,, \qquad n_P \simeq 1.3 \tag{2.7}$$

where W, L are, in that order, the transistor-channel width and length. I_{dark} self-compensation is subject to leakage in sample-and-hold switches, and such currents can easily reach pA-range values in CMOS submicron technologies. This strategy requires the DPS to be periodically calibrated under zero-illumination conditions which are, in fact, hard to grant. The circuits of Fig. 2.12 adapt the cascoded topology of Fig. 2.11(a) to overcome this problem by providing offset external tuning in both voltage (a) and current (b) domains. In these two schemes, corrections can be serially programmed at each frame through the N-bit I/O interface configured as shift register. A non-overlapping clock (i.e. `clks` and `clkh`) is mandatory to provide proper isolation between sample and hold capacitances along programming.

In the circuit of Fig. 2.12(a) the analog memory of M1 is periodically refreshed by means of a switched-cap DAC [106] in three phases: reset (`edac` = 0 and `count` = 0), conversion (`edac` = 1 and `count` = 0) and acquisition (`edac` = 1, `count` = 1 and `count` = 0). During the programming phase, C_{samp} is sequentially precharged to a V_{samp} voltage, synchronously with the sample clock signal `clks`, and according to the input code $\mathtt{p_i}$:

$$V_{samp} = \mathtt{p}_i V_{DD} \tag{2.8}$$

In order to minimize any undesired injection to C_{samp}, charge in this node is added or removed through the direct path composed by minimum-size M5-M6 transistors. These devices are controlled by the corresponding logical

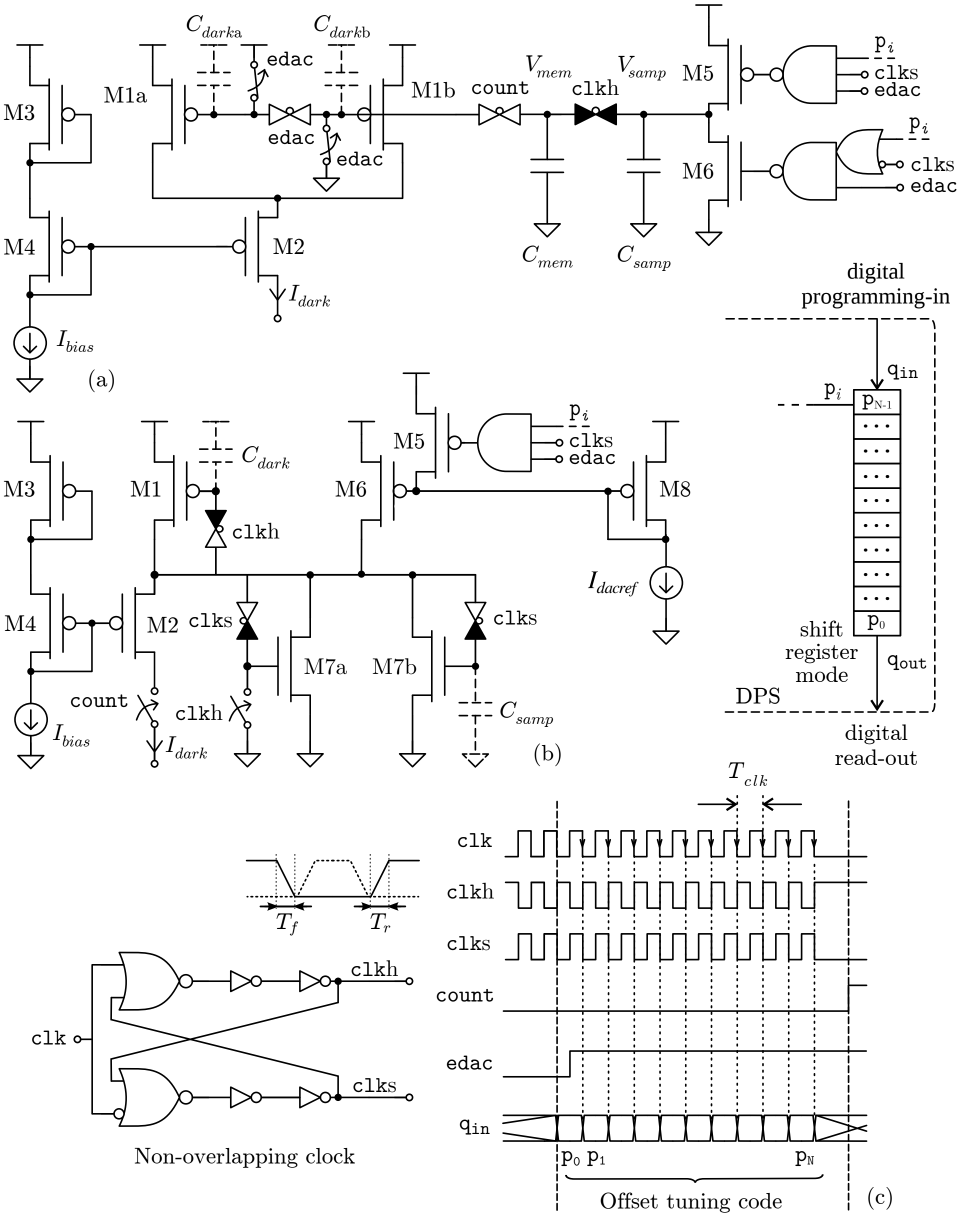

C_{dark}a
C_{dark}b
edac
M3
M1a
M1b
count
V_{mem}
clkh
V_{samp}
M5
p_i
clks
edac
M6
p_i
clks
edac
M4
M2
I_{dark}
C_{mem}
C_{samp}
I_{bias}
(a)
digital
programming-in
q_{in}
p_i
p_{N-1}
p_0
shift
register
mode
q_{out}
DPS
digital
read-out
M3
M1
C_{dark}
clkh
M6
M5
p_i
clks
edac
M8
I_{dacref}
M4
M2
clks
M7a
M7b
clks
count
clkh
I_{bias}
I_{dark}
C_{samp}
(b)
T_{clk}
T_f
T_r
clk
clkh
clks
count
edac
q_{in}
clk
clkh
clks
Non-overlapping clock
p_0 p_1
p_N
Offset tuning code
(c)

Figure 2.12 DPS input stage offset cancellation with external tuning for Fig. 2.10(b): CMOS DAC implementation in voltage (a) and current (b). Non-overlapping clock circuit and chronogram used in both schemes (c). Black filling in transmission gates indicates side includes a dummy device. All signals are active high.

function between `p_i`, `clks` and the enable `edac` signal. For every positive semiperiod of `clkh`, this charge is recombined with the one previously stored in C_{mem} generating an instantaneous voltage value

$$V_{mem(i)} = \frac{C_{samp}\mathtt{p}_i V_{DD} + C_{hold} V_{mem(i)}}{C_{samp} + C_{mem}} \tag{2.9}$$

$$V_{mem(i)} = \frac{\mathtt{p}_i V_{DD} + V_{mem(i)}}{2}, \qquad C_{dac} \doteq C_{samp} \equiv C_{mem} \tag{2.10}$$

Both capacitances are interconnected through dummy-switch devices so as to compensate for both clock feedthrough and charge injection effects. Thus, the final converted level at the end of the program-in cycle is

$$V_{mem(\mathrm{N})} = V_{DD} \sum_{i=0}^{N-1} \frac{\mathtt{p}_i}{2^{N-i}} \tag{2.11}$$

Voltage at M1 gate is also initialized along this same programming phase. Once in acquisition, charge redistribution causes:

$$\begin{aligned} V_{GB1} = V_{DD} \left[\frac{C_{dark\mathrm{a}}}{C_{dark} + C_{DAC}} \left(1 + \frac{C_{DAC}}{C_{dark\mathrm{a}}} \sum_{i=0}^{N-1} \frac{\mathtt{p}_i}{2^{N-i}} \right) - 1 \right], \\ C_{dark} = C_{dark\mathrm{a}} + C_{dark\mathrm{b}}; \\ C_{DAC} = C_{mem} + C_{samp} \end{aligned} \tag{2.12}$$

In practice, M1a/b sizing is two-fold. On the one hand, the jointed M1 device should grant enough tunable current excursion so as to cover estimated I_{dark} variances. On the other hand, the sum $C_{dark\mathrm{a}}$+$C_{dark\mathrm{b}}$ should suffice to make coupling and leakage effects at the tunable V_{G1} node unnoticeable. The higher the M1 gate capacitance C_{dark}, the lesser the DAC-programmed voltage range at this node, and the larger the needed transconductance to cover the desired dark current range. Chosen a long channel transistor (i.e. low channel-length modulation) saturated M1 device - and provided linearity in I_{dark} programming is not required - the moderate-inversion region of operation offers a promising trade-off between voltage headroom, g_{mg} and capacitance per unit area. V_{DS1} can take values below M1 threshold voltage while remaining in saturation, and g_{mg1} can be easily adjusted to satisfy both I_{dark} range and noise requirements. The PMOS nature of all offset-compensating topologies explained in this chapter facilitates achieving this last objective. Appropriate dimensioning and matching between $C_{dark\mathrm{a}}$ and $C_{dark\mathrm{b}}$ is mandatory to precharge the gate of M1 to its threshold voltage at the positive edge of `edac`.

Fig. 2.12(b) implements dark current cancellation following the same three phases (reset, conversion, acquisition) and chronogram of Fig. 2.12(a), in this case through SI techniques based on current copiers. Along conversion (`edac` $= 1$), the digital bits are sequentially fed to set the state of the PMOS switch M5. I_{dacref} provides a reference current value. When `clks` $= 1$, M6 is either switched to mirror I_{dacref} or cut off depending on the particular value of the digital bit being processed. Transistors M7 copy the sum of both M1 and M6 currents. At the succeeding semiperiod (`clkh` $= 1$), this additive current is memorized by M1 through C_{dark}. If transistors M7a and M7b are equally sized and well-matched, and equivalently to (2.10), the drain current of M1 at the end of the conversion is

$$I_{D1} = I_{dacref} \sum_{i=0}^{N-1} \frac{\mathtt{p}_i}{2^{N-i}} \tag{2.13}$$

The resulting current can be subtracted during acquisition (`count` $= 1$), and is reset while `edac` $= 0$ activates M5 and switches M6 to off. Using the same conversion procedure described above, this quasi-null current value is sampled and stored in M1. The SI-copier DAC is specially indicated in cases where a high-resolution gain tuning is not required. Using it instead of the switched-capacitor (SC)-DAC allows to save pixel area and to highen robustness to technological corners in exchange for higher sensitivity to transistor mismatch than its SC counterpart.

2.4 Asynchronous ADC with CDS

2.4.1 Motivation and Design Proposal

As explained in the state-of-the-art study of Section 1.5.1, traditional pixel sensors are current-integration cells that convert the input photogenerated signal into voltage during a certain acquisition time. When this information is directly output from the pixel, analog-only implementations suffer of acute crosstalk sensitivity between neighboring pixels and signal degradation may be significant. Under the concrete low-noise and high-speed demands of this work, the benefits of implementing A/D conversion and memory inside each pixel are copious: it reduces crosstalk, eliminates read-related column FPN and column readout noise, permits minimum equivalent noise bandwidth and provides a mechanism to digitally correct pixel performance.

Predictive A/D encoders - and specially sigma-delta modulators ($\Sigma\Delta$Ms) - are widely acknowledged in literature due to their low implementational requirements in terms of area, bandwidth and power. In general, $\Sigma\Delta$Ms are built from a pulse modulator in cascade with a digital filter. The pulse modulator quantizes (typically at resolutions as low as 1-bit) the amplitude of an error signal given by the difference between the input level and a prediction updated by a feedback DAC. Such quantization is performed at large oversampling ratios compared to Nyquist converters. As a result, the quantization error in the pulse stream is pushed to higher frequencies out of the interest band. The low-pass digital filter can then easily cut these frequency components and complete the discretization of the signal in time as a digital output word at Nyquist rate.

In its simplest form of first-order architecture, the pulse modulator is mainly resolved in two circuital approaches: PWM or PDM. PWM, a.k.a. time-to-first-spike, is equivalent to a classic single or double ramp integrating ADC and requires the use of external clock signaling for the conversion. PDM, also called integrate-and-fire or spike-counting, differentiates from the previous method in that it is a fully asynchronous approach [107, 108]. In this case, modulation is achieved as depicted in Fig. 2.13(a): The input sensor signal I_{eff} is first compared to its prediction and error is amplified by the high-gain but band-limited stage; the result is codified at 1-bit by the quantizer and the output pulse stream `dADC` and re-converted to the analog domain so as to complete closed-loop operation. As a result of its full independence on external clocking, PDM presents the advantage of adapting power consumption to input signal amplitude. Concerning noise, PDM also lowers switching activity during A/D conversion, causing less digital noise injection in the FPA. Switching noise mainly arises in the substrate and propagates through circuit asymmetries over the pixel sensor [109]. The presence of perturbations on power supply nodes, either at routing or substrate level, are reflected in higher $\sigma^2_{integ,ir}$ and $\sigma^2_{ADC,ir}$ values of (1.14). They are mostly noticeable in the quantizer stage as comparator jitter noise and can severely limit the performance of the system in terms of NETD.

In the context of circuit design for DPS cells, this predictive ADC is simplified to Fig. 2.13(b). Here, the high-gain and band-limited stage is replaced by a first order integrator, which amplifies low I_{eff} frequencies into V_{int}. The integrated signal is quantified at a given threshold V_{th} by a comparator, and the resulting `dADC` is fed back to the reset of the analog integrator, so performing the same effect that the negative feedback from the single-bit DAC of Fig. 2.13(a). Concerning the low-pass digital output filter, this block is implemented by a simple integrator (i.e. counter) whose losses are controlled by the frame initialization signal `init`.

Fig. 2.14 shows a classic implementation of such simplified PDM modulator. The analog integrator is composed here of the C_{int}-based CTIA. Apart from integrating I_{eff} into V_{int}, the CTIA compensates parasitic C_{par} effects by keeping the IR detector biased at a constant potential V_{ref}. Due to small C_{int} values, an extra capacitor (C_{CDS}) is usually added to implement CDS over the low-frequency noise generated by the CTIA stage.

However, this standard topology needs the use of two capacitors: C_{int} and C_{CDS}, reducing the pixel cell area available for other tasks. In order to improve Si-area saving, the novel single-capacitor integration/CDS scheme of Fig. 2.14(b) is proposed. The circuit operates as follows: during frame initialization (`init` $= 1$), the virtual short-circuit at inputs of the amplifier forces its low-frequency noise components to be stored in $C_{int/CDS}$; once in acquisition (`init` $= 0$), the detector quasi-static effective current I_{eff} is integrated in reverse $C_{int/CDS}$ polarization so as to remove the M1-noise charge previously accumulated in the capacitance. The comparator gen-

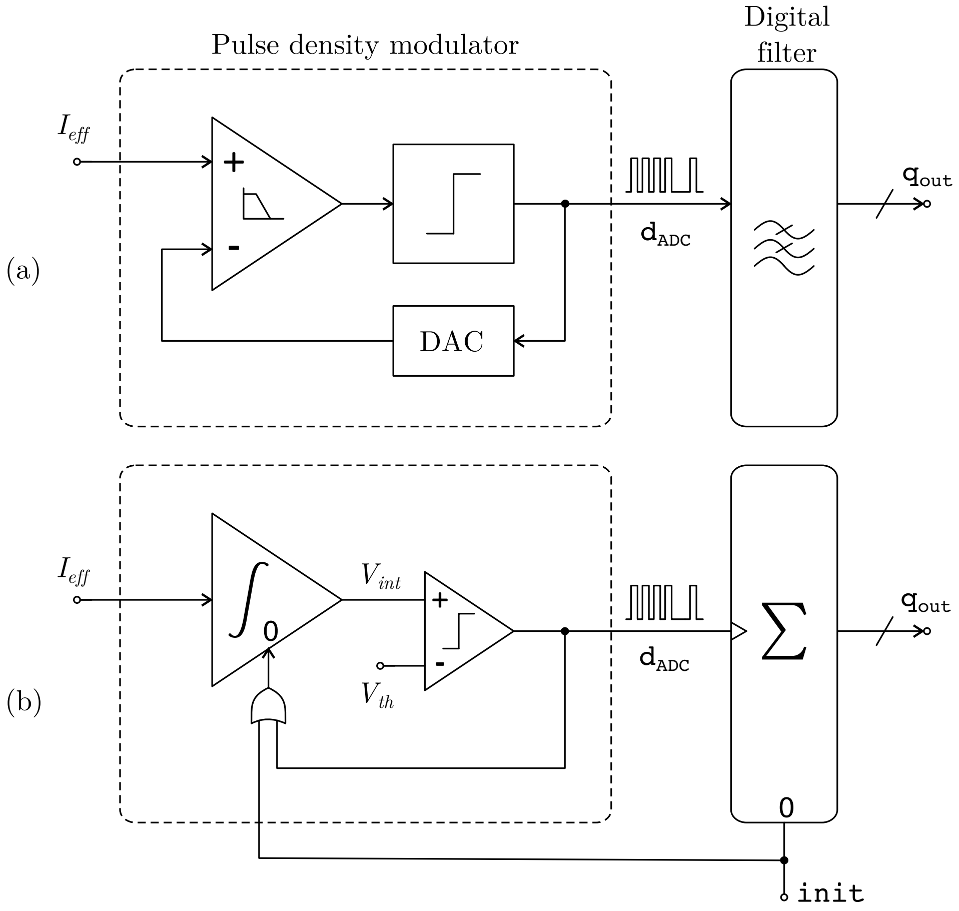

Pulse density modulator
Digital filter
I_{eff}
+
-
DAC
$\mathtt{d_{ADC}}$
$\mathtt{q_{out}}$
(a)
I_{eff}
$\int$
0
V_{int}
+
-
V_{th}
$\mathtt{d_{ADC}}$
Σ
$\mathtt{q_{out}}$
0
init
(b)

Figure 2.13 | General scheme of a first-order PDM predictive ADC (a) and adaptation to frame-based DPS cells (b).

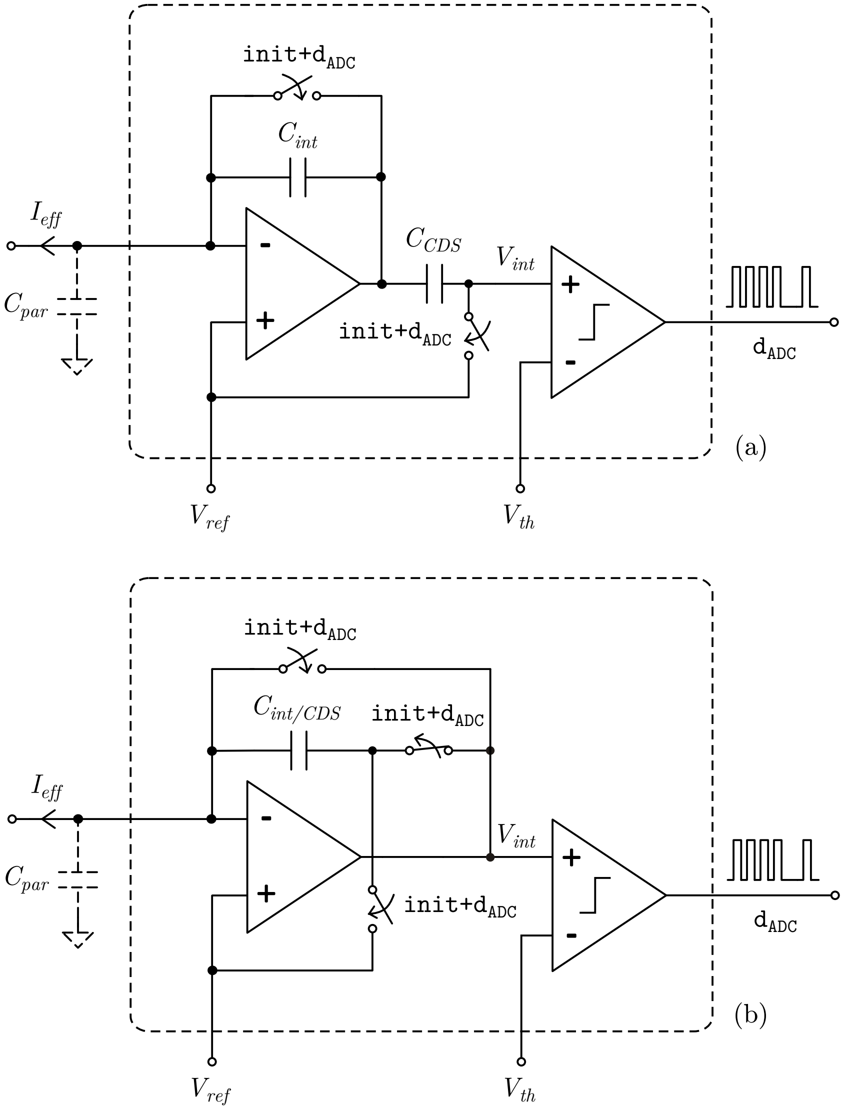

init+d_ADC
C_int
I_eff
C_par
-
+
C_CDS
V_int
init+d_ADC
+
-
d_ADC
(a)
V_ref
V_th
init+d_ADC
C_int/CDS
init+d_ADC
I_eff
C_par
-
+
V_int
init+d_ADC
+
-
d_ADC
(b)
V_ref
V_th

Figure 2.14 Classical scheme (a) and single-capacitor integration/CDS proposal (b) for the PDM part of the in-pixel integrate-and-fire ADC ($I_{eff} > 0$ case) of Fig. 2.13.

erates a new pulse or event in $\mathtt{d_{ADC}}$ every time the integrated signal V_{int} reaches a fixed threshold V_{th}. Events are sent back as reset signal for the first stage.

Considering CTIA noise and offset as effectively canceled, V_{int} in both figures can be described as

$$V_{int} = V_{th} + \frac{1}{C_{int}} \int_0^{T_{acq}} I_{eff} dt \simeq V_{th} + \frac{T_{acq}}{C_{int}} I_{eff}, \qquad BW_{eff} T_{acq} \ll 1 \quad (2.14)$$

where BW_{eff} refers to the I_{eff} bandwidth. Considering CTIA reset time (T_{res}), the closed-loop operation of Fig. 2.14 generates a spiking signal of frequency

$$f_{event} = \frac{1}{T_{res} + \frac{C_{int}(V_{th} - V_{ref})}{I_{det} - I_{dark}}} \quad (2.15)$$

Events generated during T_{acq} are counted and stored as $\mathtt{q_{out}}$ by in-pixel digital registers as detailed in Sec. 2.2. Thus, the digital inter-frame counted word takes the value

$$\mathtt{q_{out}} = f_{event} T_{acq} = \left\lfloor \frac{T_{acq}}{T_{res} + \frac{C_{int}(V_{th} - V_{ref})}{I_{eff}}} \right\rfloor \quad (2.16)$$

The resulting ADC architecture opens the possibility of pixel area optimization against KTC noise, since both capacitance of the analog integrator and capacity of the digital integrator play an equivalent role, up to the limits imposed by T_{res} and the noise floor. For (2.16) to preserve linearity, the former should be kept negligible in front of the ideal conversion frequency set by C_{int} and V_{th} at maximum I_{eff}.

2.4.2 Compact CMOS Implementation

The single-transistor M1 CTIA of Fig. 2.15(a) is proposed as the analog integrator of Fig. 2.14(b). This topology offers:

- Large resolution of the offset cancellation described in Sec. 2.3.2, since voltage variations are minimized in the input block terminal.
- Improved I_{dark} analog memory retention due to the same effect, as the calibration switch is barely affected by V_{int}.
- Low static-power consumption due to the class-AB M1 configuration: low I_{bias} levels (typically nA), that yield to a good resolution for small I_{eff} values, are made compatible with high full-scale ($\sim \mu$A) values.
- Better control over the physical design of the sub-pF floating integration capacitor C_{int}, as it can be isolated from parasitic capacitances present in other nodes (e.g. ground).
- Larger dynamic range of V_{int} and simpler implementation since ground is used as V_{ref}.
- Fast reset times under low-power operation by using a novel 3-switch scheme.

The triple switch operates as follows: during reset phase ($\mathtt{d_{ADC}} = 1$), M1 is configured as an active load following Fig. 2.15(b) in order to auto-bias its gate according to I_{bias}, the incoming signal I_{eff} and any possible input voltage offset of M1 itself; once in integration phase ($\mathtt{d_{ADC}} = 0$), the same device is operated as an inverter amplifier following Fig. 2.15(c), resulting on the V_{int} waveform depicted in the same figure. The proposed reset network also implements correlated double sampling (CDS) by copying the output noise of M1 in C_{int} during the reset phase.

After preamplification, signal V_{int} is quantified at 1-bit by the comparator M1-M10 of Fig. 2.16 according to a given threshold V_{th}. Due to the individual tuning of V_{th} discussed later on in Sec. 2.5, the topology of this comparator is optimized for high input and output ranges, as well as for low-power consumption. The circuit combines a very low static current I_{bias} with the dynamic high-current bias supplied by M7 due to the positive feedback of M8 during pulse transitions. As a result, low-power operation together with fast reset times can be obtained in practice. Once the event is generated, the $\mathtt{d_{ADC}}$ feedback to the CTIA of Fig. 2.15(a) causes the comparator to return to its previous state.

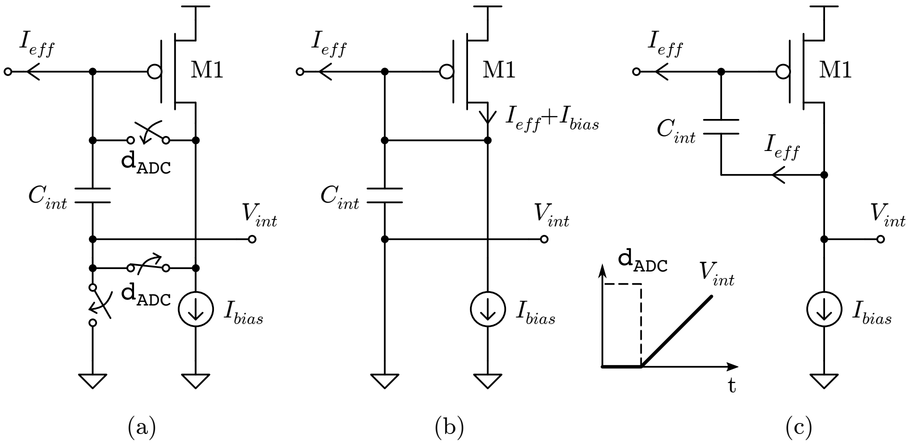

I_{eff}
M1
d_{ADC}
C_{int}
V_{int}
d_{ADC}
I_{bias}
$I_{eff}+I_{bias}$
I_{eff}
t
(a)
(b)
(c)

Figure 2.15 DPS CMOS implementation of the analog integrator (a) in Fig. 2.14(b) and operation in reset (b) and acquisition (c) phases.

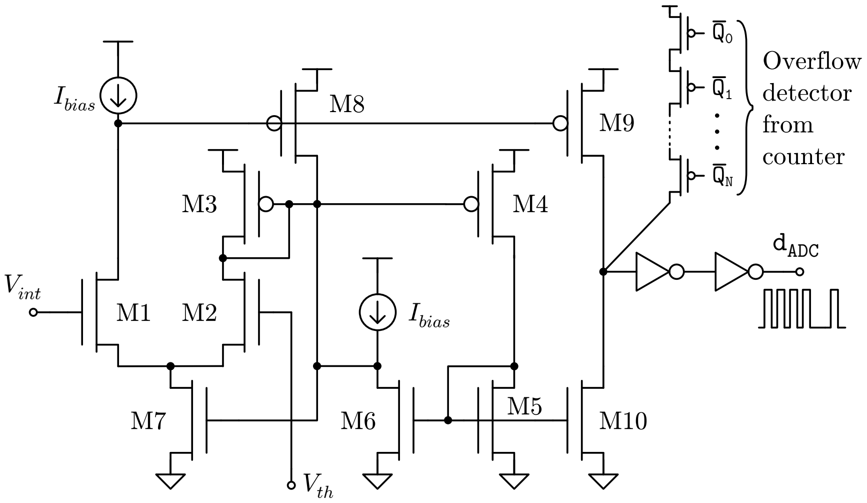

I_{bias}
M8
M9
M3
M4
$\overline{Q}_0$
$\overline{Q}_1$
$\overline{Q}_N$
Overflow detector from counter
V_{int}
M1
M2
I_{bias}
d_{ADC}
M7
M6
M5
M10
V_{th}

Figure 2.16 DPS CMOS comparator implementation as part of the PDM modulator of Fig. 2.14(b).

Fig. 2.17(a) shows main DPS noise contributions up to the preamplification stage. Quantizer noise adds as comparator jitter, but is considered to be of much lower magnitude that its preceding counterparts. In the analysis we assume all parasitic circuit capacitors to be negligible in front of C_{gs4} and C_{det} seen at the input V_x node of the M4 common-source preamplifier. The C_{det}-compensation stage amplifies the detector impedance by $G_{oa}g_{mg3}r_{03}$ to

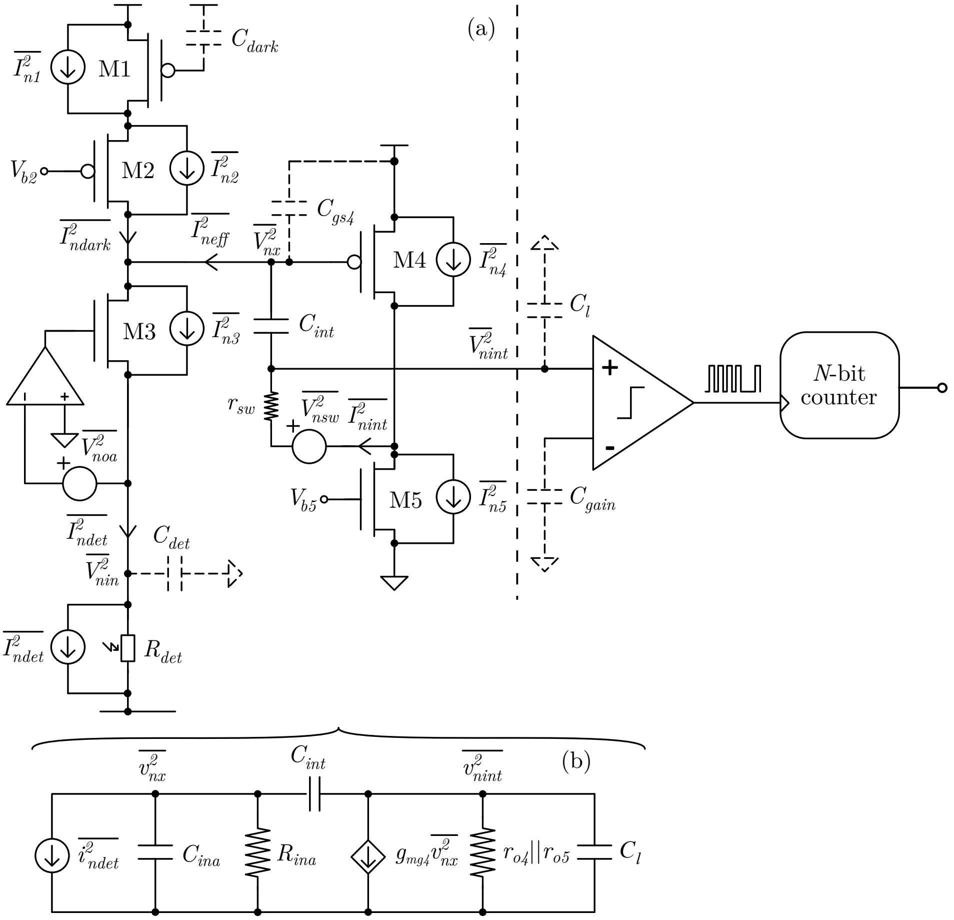

(a)
C_dark
I²_n1
M1
V_b2
M2
I²_n2
C_gs4
I²_ndark
I²_neff
V²_nx
M4
I²_n4
M3
I²_n3
C_int
C_l
V²_nint
r_sw
V²_nsw
I²_nint
+
-
N-bit counter
V²_noa
V_b5
M5
I²_n5
C_gain
I²_ndet
C_det
V²_nin
R_det
(b)
v²_nx
C_int
v²_nint
i²_ndet
C_ina
R_ina
g_mg4 v²_nx
r_o4||r_o5
C_l

Figure 2.17 Complete asynchronous ADC signal path of frame-based DPS cells during acquisition phase. Input charge integrating scheme including noise sources (a) and equivalent small-signal noise model (b).

$$Z_{inad} = \frac{G_{oa} g_{mg3} r_{03} R_{det}}{R_{det} C_{det} s + 1} \tag{2.17}$$

where G_{oa} is the gain of the OpAmp. The real part of this impedance becomes negligible when disposed in parallel with the M1-M2 cascode resistance

$$R_{ina} = g_{mg2} r_{02} r_{01} \tag{2.18}$$

Assuming

$$\frac{T_{acq}}{\pi (r_{04} || r_{05}) C_l} \gg 1 \tag{2.19}$$

open-loop preamplification gain can be estimated as

$$G_a \simeq g_{mg4} (r_{04} || r_{05}) \tag{2.20}$$

and input gain evaluated as

$$G_{ina} = G_{oa} g_{mg3} r_{03} \tag{2.21}$$

In this scenario, both C_{gs4} and C_{det}/G_{in} add up as the C_{ina} capacitance depicted in the simplified circuit equivalent of Fig. 2.17(b). Thus, the total impedance seen from the negative input of the CTIA amplifier can be approximated as

$$Z_{ina} = \frac{R_{ina}}{R_{ina} (G_a C_{int} + C_{ina}) s + 1} \tag{2.22}$$

C_{int} is amplified by $1+G_a$ due to the Miller effect, but this additive unitary factor can be disregarded due to the G_a,$G_{in} \gg 1$ expected in practice. The integrator signal transfer function (STF) STF_{int} is, accordingly,

$$STF_{int} \doteq \frac{\sqrt{\overline{v_{nint}^2}}}{\sqrt{\overline{i_{neff}^2}}} = \frac{R_{ina}G_a}{R_{ina}G_aC_{int}s+1} \tag{2.23}$$

and the noise transfer function (NTF) of the analog integrator (NTF_{int}) takes the form of

$$NTF_{int} \doteq \frac{\sqrt{\overline{v_{nint}^2}}}{\sqrt{\overline{i_{n4}^2}}} = \frac{r_{04}||r_{05}}{(r_{04}||r_{05})C_{int}s+1} \tag{2.24}$$

The $\overline{i_{neff}^2}$ source of this same figure contains all noise contributions referred to $\overline{v_{nx}^2}$ as

$$\overline{i_{neff}^2} = \overline{i_{n1,ir}^2} + \overline{i_{n2,ir}^2} + \overline{i_{n3,ir}^2} + \overline{i_{n4,ir}^2} + \overline{i_{n5,ir}^2} + \overline{i_{noa,ir}^2} + \overline{i_{nsw,ir}^2} \tag{2.25}$$

where all noise sources are stated as average spectral densities. Concretely, in the band of interest:

$$\overline{i_{n1,ir}^2} \simeq \overline{i_{n1}^2}\left(\frac{g_{ms2}+g_{md2}}{g_{ms2}+g_{md2}+g_{md1}}\right)^2 \simeq \overline{i_{n1}^2} \tag{2.26}$$

$$\overline{i_{n2,ir}^2} \simeq \overline{i_{n2}^2}\left(\frac{g_{md1}}{g_{ms2}}\right)^2 \tag{2.27}$$

$$\overline{i_{n3,ir}^2} \simeq \overline{i_{n3}^2}\left(R_{det}G_{oa}g_{mg3}\right)^2 \tag{2.28}$$

$$\overline{i_{noa,ir}^2} \simeq \frac{\overline{v_{noa}^2}}{R_{det}^2} \tag{2.29}$$

$$\overline{i_{ndet,ir}^2} \simeq \overline{i_{ndet}^2}\left(\frac{G_{oa}g_{mg3}+g_{md3}}{G_{oa}g_{mg3}+g_{md3}+1/R_{det}}\right)^2 \simeq \overline{i_{ndet}^2} \tag{2.30}$$

which is telling that $\overline{i^2_{n2,ir}}$, $\overline{i^2_{n3,ir}}$ and $\overline{i^2_{noa,ir}}$ contribute marginally into (2.25). Concerning noises generated by M4 and M5, both are attenuated as expected into $\overline{i^2_{neff}}$ as

$$\begin{aligned}\overline{i^2_{n4,ir}} &= \overline{i^2_{n4}}\left|\frac{NTF_{int}}{STF_{int}}\right|^2 \\ &= \overline{i^2_{n4}}\frac{(r_{04}||r_{05})^2}{R^2_{ina}G^2_a}\left|\frac{R_{ina}G_aC_{int}s+1}{(r_{04}||r_{05})C_{int}s+1}\right|^2\end{aligned} \tag{2.31}$$

$$\begin{aligned}\overline{i^2_{n5,ir}} &= \overline{i^2_{n5}}\left|\frac{NTF_{int}}{STF_{int}}\right|^2 \\ &= \overline{i^2_{n5}}\frac{(r_{04}||r_{05})^2}{R^2_{ina}G^2_a}\left|\frac{R_{ina}G_aC_{int}s+1}{(r_{04}||r_{05})C_{int}s+1}\right|^2\end{aligned} \tag{2.32}$$

Taking into account that the flicker noise corner frequencies (f_{nc}) of both detector and modern CMOS technologies lie beyond the kHz-range Nyquist frequency $1/(2T_{acq})$ of in-pixel A/D conversion,

$$\overline{i^2_{ndet}} \underset{2f_{acq}<f_{nc}}{\simeq} \overline{i^2_{ndet,BLIP}} + \overline{i^2_{ndet,1/f}} \tag{2.33}$$

$$\overline{i^2_{n1}} \underset{2f_{acq}<f_{nc}}{\simeq} \overline{i^2_{n1,1/f}} \tag{2.34}$$

$$\overline{i^2_{n4}} \underset{2f_{acq}<f_{nc}}{\simeq} \overline{i^2_{n4,1/f}} \tag{2.35}$$

$$\overline{i^2_{n5}} \underset{2f_{acq}<f_{nc}}{\simeq} \overline{i^2_{n5,1/f}} \tag{2.36}$$

$$\overline{i^2_{nsw}} \simeq \overline{i^2_{nsw,th}} \tag{2.37}$$

In this last equation, $BLIP$ subindex indicates background-limited infrared performance due to shot noise in the detector, and $1/f$ and th mean flicker and thermal inputs. Thus, total input-referred noises integrate across the band to

$$\overline{i^2_{ndet,irtot}} = \overline{i_{det}} + \int_0^{\frac{1}{2T_{acq}}} K_{FK_{det}}\frac{1}{f}df \tag{2.38}$$

$$\overline{i^2_{n1,irtot}} = \int_0^{\frac{1}{2T_{acq}}} \frac{K_{fkP} g^2_{mg1}}{(WL)_1} \frac{1}{f} df \tag{2.39}$$

$$\begin{aligned}\overline{i^2_{n4,irtot}} &= \int_0^{\frac{1}{2T_{acq}}} \frac{K_{fkP}}{(WL)_4 R^2_{ina}} \frac{R^2_{ina} G^2_a C^2_{int} 4\pi^2 f^2 + 1}{(r_{04} || r_{05})^2 C^2_{int} 4\pi^2 f^2 + 1} \frac{1}{f} df \\ &\simeq \int_0^{\frac{1}{2T_{acq}}} \frac{K_{fkN} g^2_{mg4}}{(WL)_4} \frac{1}{f} df, \qquad G_a \gg \frac{g_{mg4}}{4\pi C_{int}}\end{aligned} \tag{2.40}$$

$$\begin{aligned}\overline{i^2_{n5,irtot}} &= \int_0^{\frac{1}{2T_{acq}}} \frac{K_{fkN} g^2_{mg5}}{(WL)_5 R^2_{ina} g^2_{mg4}} \frac{R^2_{ina} G^2_a C^2_{int} 4\pi^2 f^2 + 1}{(r_{04} || r_{05})^2 C^2_{int} 4\pi^2 f^2 + 1} \frac{1}{f} df \\ &\simeq \int_0^{\frac{1}{2T_{acq}}} \frac{K_{fkN} g^2_{mg5}}{(WL)_5} \frac{1}{f} df, \qquad G_a \gg \frac{g_{mg4}}{4\pi C_{int}}\end{aligned} \tag{2.41}$$

where $\overline{i_{det}}$ is the mean small-signal output current of the detector, K_{FKdet} is the flicker constant for a given geometry of the detector, and K_{fkP} and K_{fkN} are the process-dependent flicker factors of PMOS and NMOS devices, respectively.

Noise in reset switches follows the kT/C rule of SC circuits. This component is oversampled at a ratio $\mathtt{q_{out}}$ and low-pass filtered by the digital counter of Fig. 2.17. Hence, total KTC noise is trimmed to

$$\overline{i^2_{nsw,irtot}} \simeq \frac{3kTC_{int}}{T_{acq} \mathtt{q_{out}}} \tag{2.42}$$

being k the Boltzmann constant and T the temperature of operation. Acccording to (2.42), KTC noise is achieved under full-scale counts of value $2^{N_{cnt}} - 1$, where N_{cnt} are the number of bits of the digital integrator.

Now, taking into account the noise sources of Fig. 2.17 and remembering from (1.12) that

$$NETD_{img} \propto \frac{1}{SNR_{img}} \tag{2.43}$$

the equivalent SNR_{img} of the thermal imaging device is found to be

$$SNR_{img} = \frac{\sqrt{\overline{i^2_{eff}}}}{\sqrt{\overline{i^2_{neff,tot}}}} \simeq \frac{\sqrt{\overline{i^2_{eff}}}}{\sqrt{\overline{i^2_{n1,irtot}} + \overline{i^2_{n4,irtot}} + \overline{i^2_{n5,irtot}} + \overline{i^2_{nsw,irtot}}}} \tag{2.44}$$

The following conclusions can be argued in base of the previous equations:

- The NETD of the imager can be substantially enhanced by optimizing the STF_{int} of the CTIA amplification core. As the noise contributions of M2 and M3 are insignificant along the band of interest, the intrinsic gain of this two transistors should be raised by using long channel and aspect ratios, together with subthreshold biasing.

- If area restrictions concur, a cascode stage for M4 and M5 would boost G_a thus effectively maximize STF_{int}. In such high-gain cases, $\overline{i^2_{n4,ir}}$ approaches $\overline{i^2_{n4}}$ and transistor sizing should considerate the direct contributions of g_{mg4} and g_{mg5} into $\overline{i^2_{neff}}$. For lower G_a values (i.e. non-cascode CTIA), the DC noise response of M5 is improved by increasing M4 transconductance g_{mg4} without degrading the noise performance of the second device. As the CDS filters out this very-low noise frequencies, the previous measure can be accommodated to curtailing signal losses at M4 gate capacitance by use of moderate-inversion biasing.

- Because major flicker noise contributions of M4 and M5 are removed by CDS, the size of these two devices can be economized to leave room for the offset cancellation stage. M1 should be dimensioned generously - specially in terms of channel length - so as to increase the amplifier input impedance and minimize its flicker contributions. Low g_{mg1} transconductances are also desirable in this case.

- KTC noise can be diminished by compacting C_{int} while increasing the capacity of posterior low-pass filtering provided by the counter. C_{int} values can be lowered down to the limits imposed by the signal losses introduced by small G_aC_{int}/C_{ina} ratios. Furthermore, in order to maximize SNR_{img} all C_{int}, V_{th} and N-bit counter capacity need to be scaled accordingly to input I_{eff} range, circuit noise levels, and the maximum event frequency limited by T_{res} in (2.15).

- If KTC noise is kept below flicker levels, restricting the noise bandwidth by the use of longer acquisition times results in $\overline{i^2_{neff,tot}}$ improvement at an approximate rate of 3dB/dec. Moreover, and because the equivalent integrated signal increases proportionally to exposure time, SNR_{img} may be simultaneously risen to 11.5dB/dec (and $NETD_{img}$ analogously decreased) by tuning each pixel gain in order to avoid saturation.

2.5 Individual Gain Tuning

2.5.1 Motivation and Design Proposal

While offset compensation allows to increase the number of effective photogenerated carriers integrated in acquisition and exploit the dynamic range of pixels along the focal plane, gain corrections are also needed in practice to:

- Avoid responsivity variances on the imager caused by geometrical, electrical and thermal mismatching in both pixel detectors and readout circuits.

- Adjust conversion sensitivity to DPS noise floor.

- Provide a mechanism for automatic gain control (AGC) at specific regions of interest (ROIs) in the image (e.g. the typical scenario of a dark tunnel seen from the bright outside).

Optimizing the dynamic range of the imager means adapting ADC resolution. In the case A/D conversion schemes based on asynchronous PDM, the

1-bit quantification level (V_{th}) has to be fixed in accordance to

$$\frac{V_{th}^2}{STF_{int}^2} \equiv 2\overline{i_{neff,tot}^2} \tag{2.45}$$

Under ideal integration conditions ($G_a \to \infty$), the signal transfer function of the entire preamplification stage behaves as the wanted continuous-time integrator and the minimum quantification level V_{thmin} can be approximated as

$$V_{thmin}^2 \equiv 2\frac{\overline{i_{neff,tot}^2}T_{acq}}{C_{int}^2} \tag{2.46}$$

Provided V_{th} is a gain-tunable value, C_{int} should be dimensioned to satisfy the preceding equation, and N_{cnt} be made large enough to fit full-scale effective detector signal. In this case, V_{th} configurability can be mostly devoted to FPN cancellation and AGC tasks. As with I_{dark}, V_{th} programming codes can be entered through the digital interface of Sec. 2.2 as depicted in Fig 2.18.

If V_{th} D/A conversion is designed linear and rail-to-rail range, gain corrections can be serially programmed at every other frame according to the equation

$$V_{th} = V_{DD}\frac{1-2^{-N_{prog}}}{2^{N_{prog}}-1}\mathtt{q_{in}} \doteq G_{DAC}\mathtt{q_{in}} \tag{2.47}$$

where G_{DAC} and N_{prog} stand for the DAC conversion gain and the number of effective bits used for programming, respectively. Under negligible reset times, substituting V_{th} by (2.47) in (2.16) results in the tuning characteristic

$$\mathtt{q_{out}} = \frac{T_{acq}}{C_{int}G_{DAC}\mathtt{q_{in}}}(I_{det} - I_{dark}) \tag{2.48}$$

inversely proportional to the input gain programming code.

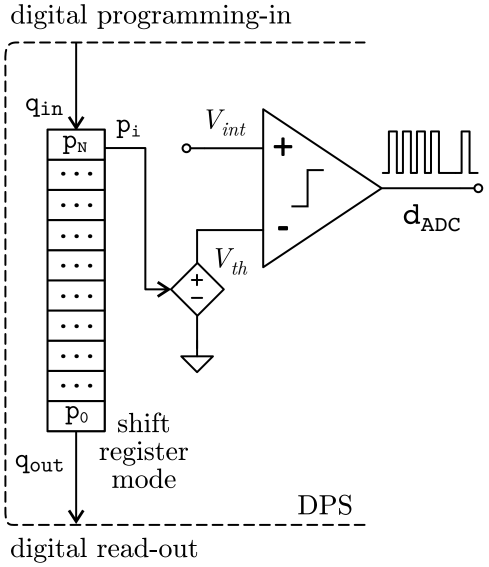

digital programming-in
qin
pN
pi
Vint
+
-
dADC
Vth
p0
shift register mode
qout
DPS
digital read-out

Figure 2.18 General scheme of the individual gain tuning proposal for the in-pixel PDM ADC of Fig. 2.14(b).

2.5.2 Compact CMOS Implementation

In order to compact circuital design to pixel-pitch restrictions, V_{th} programming can be achieved by reusing the SC-DAC circuit of Fig. 2.12(a) as depicted in Fig. 2.19. An additional signal `cal` would multiplex the D/A converter as explained in Sec. 2.1. The suggested scheme effortlessly disables gain tuning by fixing $\texttt{q}_{\texttt{in}}$ to ‘1’ and limiting `edac` pulse duration to the last programming clock cycle (i.e. by performing 1-bit programming to mid scale). Both DAC design constraints and operation are alike to those detailed in Sec. 2.3.2, with the additional demand of a high-excursion comparator as resolved in Fig. 2.16.

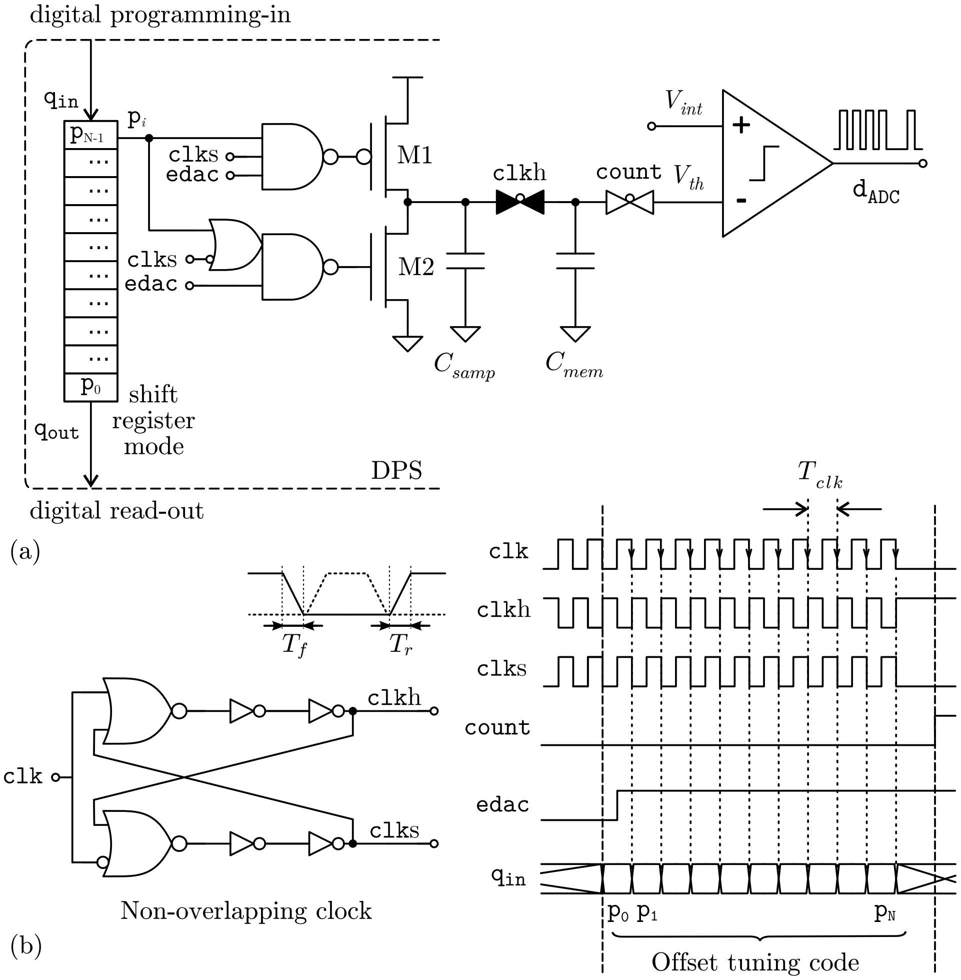

digital programming-in
q_{in}
p_i
p_{N-1}
...
p_0
clks
edac
clks
edac
M1
M2
clkh
count
V_{int}
V_{th}
+
-
d_{ADC}
C_{samp}
C_{mem}
q_{out}
shift register mode
DPS
digital read-out
(a)
T_f
T_r
clk
clkh
clks
Non-overlapping clock
(b)
T_{clk}
clk
clkh
clks
count
edac
q_{in}
p_0 p_1
p_N
Offset tuning code

Figure 2.19 CMOS DAC implementation of the DPS individual gain tuning circuit for frame-based imagers reusing the SC-DAC of Fig. 2.12 (a). Non-overlapping clock circuit and operational chronogram (b). Black filling in transmission gates indicates side includes a dummy device. All signals are active high.

2.6 Local Bias Generation

2.6.1 Motivation and Design Proposal

Whereas most of the DPS realizations reported in literature generate analog I/V references at system level, the DPS system architecture addressed in this chapter delivers all biasing levels and signal references locally in each pixel sensor. Advantages are alluring:

- Crosstalk avoidance in common biasing lines between DPS cells.
- Relaxation of inter-pixel connectivity at focal plane level (e.g. number of metal layers employed in routing).
- Narrowing of possible technology mismatching sources.
- Simplification of external resources needed to operate the imager.

On the other hand, in-pixel biasing imposes serious challenges in terms of topology compactness and standard CMOS compatibility, which need to be overcome without endangering the overall reliability of the sensor matrix.

Many CMOS-compatible bandgap low-voltage references have been published in research [110–116]. Nonetheless, some of them are not suitable to be implemented in modern CMOS processes due to the use of parasitic bipolar junction transistors [110] or diodes [113]; other MOSFET-based solutions require the integration of linear resistors [111], mismatch-sensitive multithreshold processes [112, 115, 116] or complex, area-consuming circuitry [114]. The proposal of Fig. 2.20 is conceived to exploit the exponential dependence of subthreshold MOSFET transistors on both inter-terminal (V_{ref}) and thermal (U_t) voltages, so as to generate single-threshold all-MOS proportional to absolute temperature (PTAT) voltage references as well as bias currents based on their specific current (I_S).

The basic idea consists in describing the PTAT voltage generator as a current-mode amplifier (G) within a constant attenuation feedback ($1/P$) as illustrated in this same Fig. 2.20. The feedback loop sets the stable operating point by imposing $GP = 1$. As I_{out} is proportional to e^{V_{ref}/U_t}, the temperature-proportional voltage reference V_{ref} can be controlled in the compressed domain:

$$x_{ref} = \ln(P) \tag{2.49}$$

where x_{ref} is the normalized factor V_{ref}/U_t. Low voltage operation is achieved by its log compression with respect to circuit currents. The corresponding bias current takes the value of I_{in}, the current flowing through the input impedance of the amplifier. Linearity in this load element is only necessary in case of additional PTAT specifications for I_{in}. Concerning bias accuracy, the main source of uncertainty in (2.49) comes from the resolution of the P factor. Hence, it is convenient to express the relative accuracy on x_{ref} in terms of

$$\left(\frac{\Delta x_{ref}}{x_{ref}}\right) = \frac{\ln(1+\frac{\Delta P}{P})}{\ln(P)} \simeq \frac{1}{\ln(P)}\left(\frac{\Delta P}{P}\right), \qquad \Delta P \ll P \tag{2.50}$$

Due to the log dependence on P, maximum x_{ref} sensitivity occurs at $P \to 1+$, whereas x_{ref} robustness increases with this same P variable. Thus, high

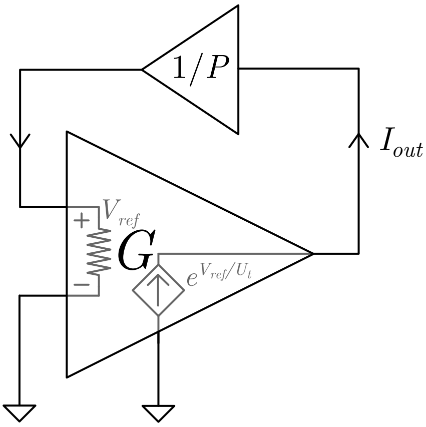


Figure 2.20 PTAT reference architecture proposal for the local bias generation in frame-based DPS of Fig 2.1.

sensitivity should be avoided in favor of high P ratios and larger x_{ref} values. In implementations of Fig. 2.20, ΔP is typically associated to technology mismatching at transistor level and must be taken into account during the design process as described downwards.

2.6.2 Compact CMOS Implementation

From a circuit viewpoint, fixed feedback $1/P$ can be obtained by simple geometry scaling (i.e. current mirroring), and the exponential gain G procured through Gate Driven - Source Controlled (GD-SC) topologies. The compact CMOS circuit of Fig. 2.21 operates the MOSFET devices in weak inversion in order to bias low-power static consumption [117].

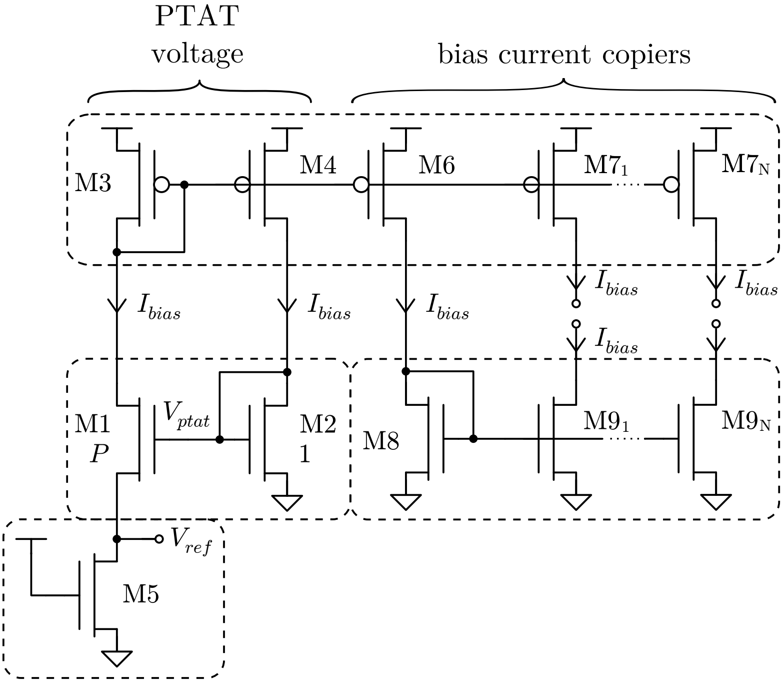

PTAT
voltage
bias current copiers
M3
M4
M6
M7$_1$
M7$_N$
I_{bias}
I_{bias}
I_{bias}
I_{bias}
I_{bias}
I_{bias}
I_{bias}
M1
P
V_{ptat}
M2
1
M8
M9$_1$
M9$_N$
V_{ref}
M5

Figure 2.21 CMOS implementation of the DPS PTAT local bias generator based on the log companding architecture of Fig. 2.20.

The core of this circuit is composed of M1-M5, while M6-M8 supplies copies of the resulting I_{bias} current to bias the pixel where necessary. Supposing weak inversion, direct saturation operation [96] of M1 and M2 (GD-SC cell) and no noticeable channel length modulation effects, the symmetry of the current mirror M3-M4 forces drain currents in both devices to be

$$I_{D1} = I_{S1} e^{\frac{V_{ptat} - V_{TO}}{n_N U_t}} e^{-\frac{V_{ref}}{U_t}} = I_{S2} e^{\frac{V_{ptat} - V_{TO}}{n_N U_t}} = I_{D2}, \tag{2.51}$$

where V_{TO} stands for the threshold voltage. Based on the previous equation, the exponential gain expression is straightforward:

$$G = \frac{I_{S1}}{I_{S2}} = e^{-\frac{V_{ref}}{U_t}} \tag{2.52}$$

Accordingly, and due to the P scaling ratio, the source voltage of M1 follows the PTAT law

$$V_{ref} = U_t \ln P \tag{2.53}$$

that illustrates the direct dependence between P and V_{ref} at ambient temperature. Sub-100mV are in practice achievable for $P > 10$.

M5 generates I_{bias} operating in strong inversion conduction as an equivalent non-linear load attached to V_{ref}. According to [96]:

$$I_{bias} = I_{D5} = \beta \left(V_{DD} - V_{TO} \right) V_{ref}, \qquad V_{ref} \ll V_{DD} - V_{TO} \tag{2.54}$$

The circuit of Fig. 2.21 provides low current (nA) bias values to the analog cells while keeping pixel static power consumption below the μW. Additionally, and thanks to the high overdrive of M7, the absolute process variations of I_{bias} are reduced to β, while technology mismatching is mainly caused by P through V_{ref}. In modern CMOS technologies, transistor mismatching is dominated by V_{TO} over β for a wide range of drain current levels, and its relative effect on drain current is maximum in weak inversion. Therefore, mismatch sensitivity basically depends on the M1-M2 PTAT core threshold voltage mismatching. From (2.54):

$$\Delta I_{bias} \propto \Delta V_{ref} \tag{2.55}$$

Considering also (2.54):

$$\Delta V_{ref} = U_t \ln\left(1 + \frac{\Delta P}{P}\right) \simeq U_t \left(\frac{\Delta P}{P}\right), \qquad \Delta P \ll P \tag{2.56}$$

According to Pelgrom's law [118], the standard deviation of the P ratio due to the theshold voltage mismatching is

$$\sigma\left(\frac{\Delta P}{P}\right) \simeq \frac{\sigma\left(V_{TO}\right)}{n_N U_t} = \frac{1}{\sqrt{(WL)_{1,2}}} \frac{A_{V_{TO}}}{n_N U_t} \tag{2.57}$$

where $A_{V_{TO}}$ stands for the threshold voltage mismatching constant. Therefore, absolute and relative mismatching inherit the proportionality

$$\sigma\left(\Delta I_{bias}\right) \equiv \sigma\left(\Delta V_{ref}\right) \propto \frac{1}{\sqrt{(WL)_{1,2}}} \frac{A_{V_{TO}}}{n_N} \tag{2.58}$$

$$\sigma\left(\frac{\Delta I_{bias}}{I_{bias}}\right) \equiv \sigma\left(\frac{\Delta V_{ref}}{V_{ref}}\right) \propto \frac{1}{\sqrt{(WL)_{1,2}}} \frac{A_{V_{TO}}}{n_N U_t} \tag{2.59}$$

In consequence, absolute variance only depends on the device area (WL), whereas relative is inversely proportional to P as foreseen in 2.6.1. Such sensitivity can be improved by both choosing higher V_{ref} values $(P \gg 1)$ and larger M1, M2 devices.

3

Frame-Free Compact-Pitch IR Imagers

3.1 Imager Architecture and Operation Proposal

As monolithic VPD PbSe-CMOS integration develops, initial process uniformity concerns become more relaxed and pitch is considerably reduced. This second line of research is intended to offer a second architecture adapted to these new requirements, and aims to exploit both pixel compactness and wide bandwidth of mature MWIR detectors. For such a purpose, the vision sensors presented in this chapter maintain the specs of being low-power, self-biased, and providing a low-crosstalk digital-only I/O interface, together with offset PVT-compensation and internal PDM, adding up the functionality of delivering asynchronous frame-free readout together with memoryless ADC. These last two inclusions overcome size constrains in the ADC block of Chapter 2, and output bandwidth (BW) limitations at its synchronous readout when upscaling the FPA size in high-speed applications with sparse activity in the focal plane. In this sense, a promising workaround is the use of address event representation (AER) communication protocols at pixel level [119] which, besides simplifying A/D conversion by moving part of its signal processing outside the pixel, also adapt transmission capacity to visual contents themselves.

In the proposed architecture of Fig. 3.1, DPS cells are accessed at column and row levels. Every pixel makes use of the integrate-and-fire principle seen in Sec. 2.4 to generate positive and negative events, which are translated by the in-pixel AER interface into or-wired `col` and `row` communication requests. Peripheral readout circuitry receives all the resulting $\texttt{col}_{\texttt{io}}$ and $\texttt{row}_{\texttt{io}}$ access petitions and may avoid collision by selecting which one to attend returning an active acknowledge at both buses (grey and dashed input arrows). This digital pulse is sent back to the internal pixel AER interface, and managed at this module to finish the readout in each selected DPS: event polarity is transmitted together with its corresponding address in the FPA and the communication cycle restarted. In this scheme, direct offset programming is substituted by the dynamic tuning through `tune` of the high-pass corner at which low frequencies are filtered out. Low-frequency currents are reused for self-biasing purposes. As depicted in Fig. 3.1(a,b), such strategy not only allows to cancel offset FPN, but also to optimize output traffic (i.e. offers programmable data compression) by extracting only the temporally-relevant vision contents of the MWIR scene.

3.2 Event-Driven Communications

3.2.1 Motivation and Design Proposal

Frame-based devices have been the dominant imaging method from the earliest days of human-made cameras. Supported by more than half a century of standard machine vision algorithms, such vision systems have evolved into high-speed high-resolution FPA imagers - massively sampled at context-independent rates - that generate extensive amounts of output data. Consequence of this traditional fixed-readout time paradigm, outcoming data heavily loads output channel capacity, consumes high power in video processing and difficults real-time operation. Moreover, DR in these systems is limited by the finite pixel integration capacity and the common acquisition time shared over the focal plane; dependency on the former also plays against pixel-pitch compaction.

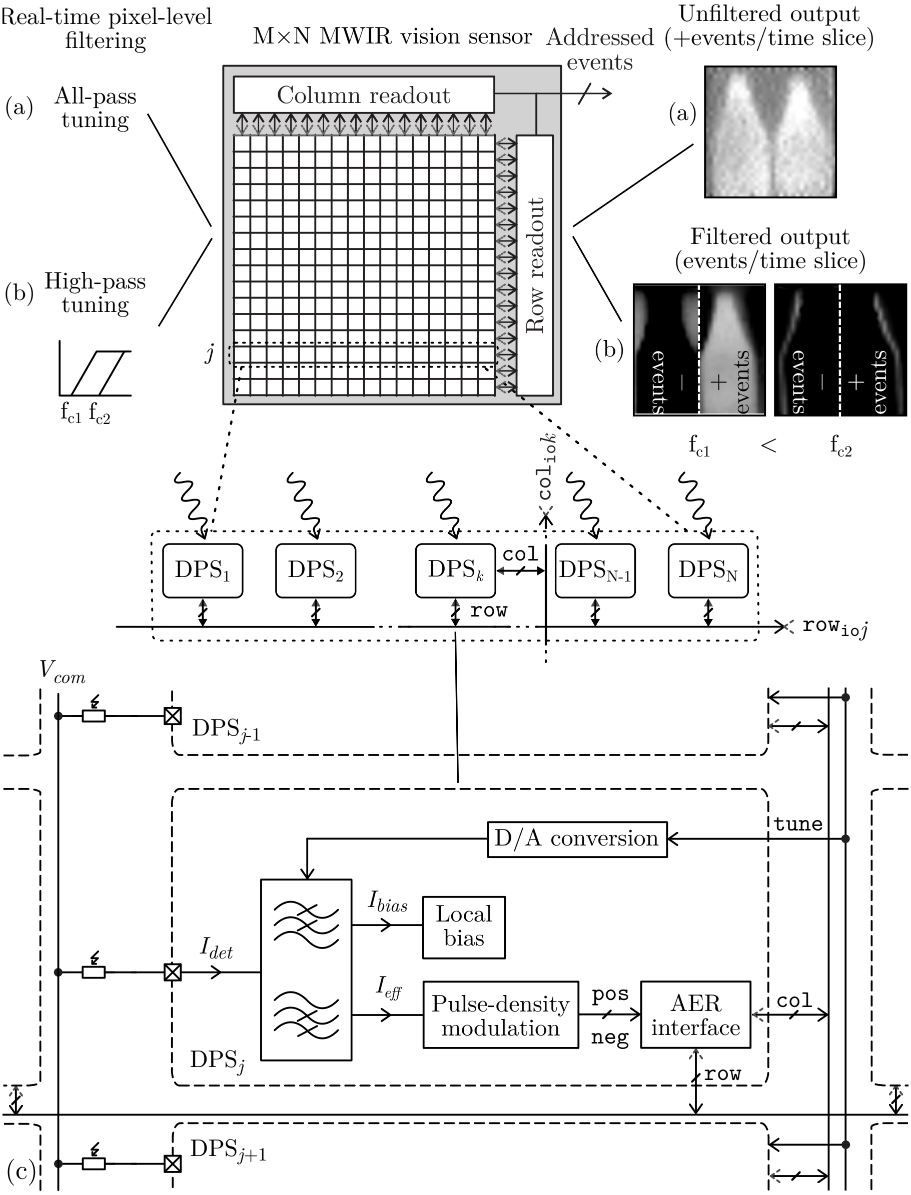

Real-time pixel-level filtering
M×N MWIR vision sensor
Addressed events
Unfiltered output (+events/time slice)
(a)
All-pass tuning
Column readout
Row readout
(a)
(b)
High-pass tuning
Filtered output (events/time slice)
(b)
j
f_{c1} f_{c2}
− events
+ events
− events
+ events
f_{c1} < f_{c2}
col_{iok}
DPS_1
DPS_2
DPS_k
col
DPS_{N-1}
DPS_N
row
row_{ioj}
V_{com}
DPS_{j-1}
tune
D/A conversion
I_{bias}
Local bias
I_{det}
I_{eff}
Pulse-density modulation
pos
neg
AER interface
col
DPS_j
row
DPS_{j+1}
(c)

Figure 3.1 Frame-free Compact-pitch IR imager proposal. Practical examples of raw (a) and low-pass filtered output imaging (b). General DPS architecture (c). Figure not in scale.

Event-based pixel sensors asynchronously output adressed events (AEs) when they detect a meaningful occurrence in the visual scene. Episodes and regions of interest vary with the sensor, covering a wide spectrum of classes: foveated sensors [120, 121], simple luminance-to-frequency sensors [66], luminance-time-to-first spike (TFS) coding sensors [122, 74], temporal contrast detectors [123, 124, 90], spatial contrast sensors [68, 125], smart motion sensors [126, 127], and spatio-temporal filtering sensors [128, 129, 72]. All previous systems, however, share one common trait: photo-generated events are usually much sparser for typical visual input than in fixed sampling-rate systems.

The practical totality of frame-free video acquisition systems use the bioinspired AER communication protocol [130, 131]. AER clusterizes spiking elements in high-frequency row or column-wise activity blocks. Transmission with a receiver is established by packet switching which, contrary to circuit-switched networks, allows to access shared interfacing resources on the fly. This characteristic avoids any latency associated to hard-switching the network, and is specially effective when the communication takes place between two end points in small bursts of data. If spike delays are kept at lower orders of magnitude than mean cluster-level inter-spike intervals, AER time represents itself, and active pixels can be encoded as row-column addresses plus one polarity-signaling bit.

Under the scenario of activity-only full-scale spike generation (i.e. null static-signal conversion), squared N_{pix}-by-N_{pix}-pixels FPAs, and N_{out} I/O available pin-out, AER vision sensors transmit data at a frequency

$$f_{outff,ev} = \overline{r_a} N_{pix}^2 f_{fs} \left\lceil \frac{\lceil \log_2(N_{pix}^2 + 1) \rceil}{N_{out}} \right\rceil \tag{3.1}$$

where $\overline{r_a}$ is the mean active population ratio and f_{fs} is the sampling frequency of full-scale changing inputs. The term $\lceil \log_2(N_{pix}^2 + 1) \rceil$ stands for the number of outputs needed to address all DPSs in the focal plane. In contrast, serial-readout systems with a fixed scanning-time (i.e. the frame-based architecture of the previous chapter) must be able to deliver all data in an insignificant fraction (ordinarily 1/10) of the acquisition time. In other words:

$$f_{outfb} = 10 f_{acq} N_{pix} \left\lceil \frac{N_{pix}}{N_{out}} \right\rceil \left\lceil \log_2 \left(\frac{f_{fs}}{f_{acq}} + 1 \right) \right\rceil \tag{3.2}$$

Let's suppose N_{out} is larger enough to fit all necessary address-encoding bits (usually the case of contemporary CMOS technologies). Equaling (3.1) to (3.2) and simplifying, full-scale event-based sampling produces lower readout rate than frame-based approaches if

$$\overline{r_a} < \frac{10 f_{acq}}{N_{pix} f_{fs}} \left\lceil \frac{N_{pix}}{N_{out}} \right\rceil \left\lceil \log_2 \left(\frac{f_{fs}}{f_{acq}} + 1 \right) \right\rceil \tag{3.3}$$

Or, equivalently:

$$\overline{r_{amax,ev}} = \frac{10}{N_{pix}} \left\lceil \frac{N_{pix}}{N_{out}} \right\rceil \frac{\lceil \log_2 (N_{evfs} + 1) \rceil}{N_{evfs}} \tag{3.4}$$

where N_{evfs} is the number of events generated during an acquisition cycle, in frame-based imagers, for full-scale input signaling. Assuming base 2 values of both N_{pix} and N_{out} jointly with $N_{pix} > N_{out}$, (3.4) turns out to be

$$\overline{r_{amax,ev}} = \frac{10}{N_{out}} \frac{\lceil \log_2 (N_{evfs} + 1) \rceil}{N_{evfs}}, \qquad N_{pix} = k N_{out}; \quad k \in \mathbb{N} \tag{3.5}$$

that is, independent of N_{pix} and downscaled by a factor N_{out}. To decrease sparsity requirements, another frame-free strategy is to substitute column-address encoding by the simultaneous readout of all positive and negative pixel outputs at column level. This proposal is very appealing in imaging scenarios like Fig. 3.1(b), where events are frequently aligned in one of the dimensions of the array. In this case,

$$f_{outff,col} = \overline{r_a} N_{pix} f_{fs} \left\lceil \frac{\lceil \log_2(N_{pix}) \rceil + 2N_{pix}}{N_{out}} \right\rceil \tag{3.6}$$

and

$$\overline{r_{amax,col}} = \frac{N_{pix}}{\left\lceil \frac{\lceil \log_2(N_{pix}) \rceil + 2N_{pix}}{N_{out}} \right\rceil} \overline{r_{amax,ev}} \tag{3.7}$$

Fig. 3.2 shows $\overline{r_{amax}}$ dependency on both number of events and pixels in the focal plane. Requirements on $r_{amax,col}$ relax as the FPA gets larger and saturate assymptotically to

$$\overline{r_{amax,col}} \underset{N_{pix} \to \infty}{=} \frac{N_{out}}{2} \overline{r_{amax,ev}} \tag{3.8}$$

when $\log_2(N_{pix})$ values become negligible in front of N_{pix}. Succeding sawteeth indicate 1-bit increases of the in-pixel digital integrator's capacity of frame-based schemes. For full 10-bit excursion (i.e. 1023 full-scale events) and all the FPA sizes selected in the graph, channel loading is optimized if the mean active fraction $\overline{r_a}$ is lower than 0.31% in column-address encoding and 4.89% in direct readout. This same value decreases to 0.01% and 0.23%, respectively, if a frame resolution of 15 bits is desired. Once again, sparsity appears as an essential characteristic of event-driven communication systems. This subject will be addressed in detail in Sec. 3.3.

Because events are generated asynchronously in the focal plane, potentially simultaneous pulses are likely to collide in a shared output bus. When this phenomenon occurs, events can be either discarded or queued following an specific arbitration rule. The former strategy minimizes transmission latency at the cost of higher loss rates, which limit maximum throughput to 18% of output channel's capacity; the latter offers 95% capacity with higher latencies of a few % of the inter-spike intervals [132]. If arbitration is only performed in one dimension of the array, the total delay of

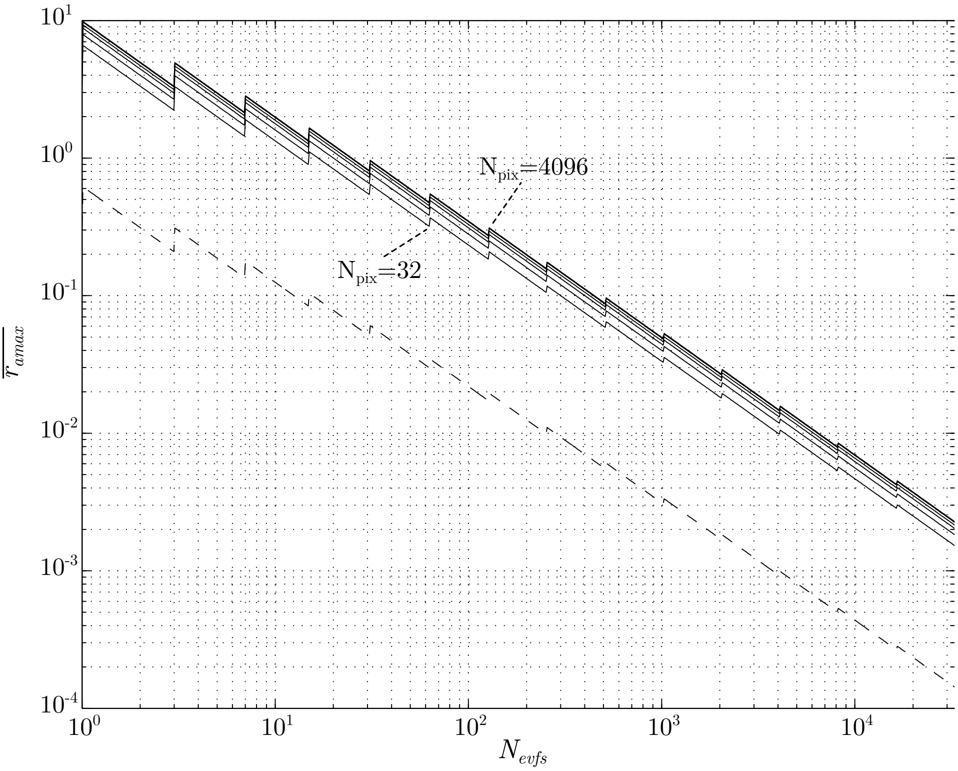


Figure 3.2 r_{amax} vs. N_{evfs} from 32 to 2048-pixel binary FPA sizes and $N_{out} = 32$ pads. Direct readout (solid line) and column encoding (dashed line).

transfers can be minimized by using burst-mode schemes like [133, 134], which allow transmitting selected row/column-events at the time the next cluster is being selected. Since $N_{pix} > 256$ pixels are not foreseen at this stage of research, and considering substantial event clustering is expected in one of the dimensions of the array for the target applications of Sec. 1.6.1, the communication strategy of Fig. 3.3 is proposed. Compared to other sparse-oriented fully-arbitrated designs (e.g. [66, 133]), the adopted scheme enhances both throughput and latency by implementing row-address encoding together with direct column readout. Thus, the `row` bus of Fig. 3.1 is substituted by the i/o signals `ack` and `req`, and `col` takes the form of an unidirectional bus composed of `outp` and `outn`. Internal AE interfacing blocks are detailed in Sec. 3.2.2, whereas peripheral transmission circuitry is explained in Sec. 3.6.

Asynchronous transmission executes by a four-phase handshaking cycle: As soon as any positive or negative event is generated, pixels pull up the request signal $\texttt{req}_k$ - shared at row level - where k is the active row. `req` signals travel through the arbiter and are output as a `reqo` handshaking signal to establish communication with an external receiver. In case this device is listening and ready, the cycle is closed by asserting an `acki` acknowledge to the ROIC. Upon reception of this signal, the arbiter selects a row and propagates the acknowledge back to the FPA. All active DPS cells in the chosen row pull up `outp` or `outn` signals, depending on polarity, and transmit the logic state to communication logic. This digital block synchronizes with `acki` so as to select the columns to be multiplexed and transmitted to the receiver jointly to the row addresses encoded at the time of acknowledgement. In order to facilitate an appropriate readout, event-buses can be complemented with an output ready `rdy` signal matched to worst-case delays. Data at both ports is hold until communication is finished by return of `acki` to its resting '0' state. Fig. 3.4(c) depicts the whole transmission sequence for the adopted in-pixel CMOS interface outlined below.

3.2.2 In-pixel compact CMOS Implementation

In-pixel event addressing is achieved by the CMOS implementation of Fig. 3.4. The high-pass filtered photocurrent is integrated and compared at two levels in order to generate both polarities of the system. Although communication is immediately reset, DPS cells hold on to the row request until they are reset by row acknowledging. For this reason, and because pixels might cross the threshold at an arbitrarily slow pace, each comparator incorporates an internal positive feedback loop M1-M3 as seen in Fig. 3.4(a). This scheme not only avoids metastability issues by cleaning up pulse transitions under low-power operation, but also generates the non-overlapped reset signals of Fig. 3.4(c). Concerning the AER interface of Fig. 3.4(b), a dynamic bus driver is implemented following M4 to ensure secured data transmission during the acknowledge window (t_{ack}). `req`, `outp` and `outn` wired-OR lines

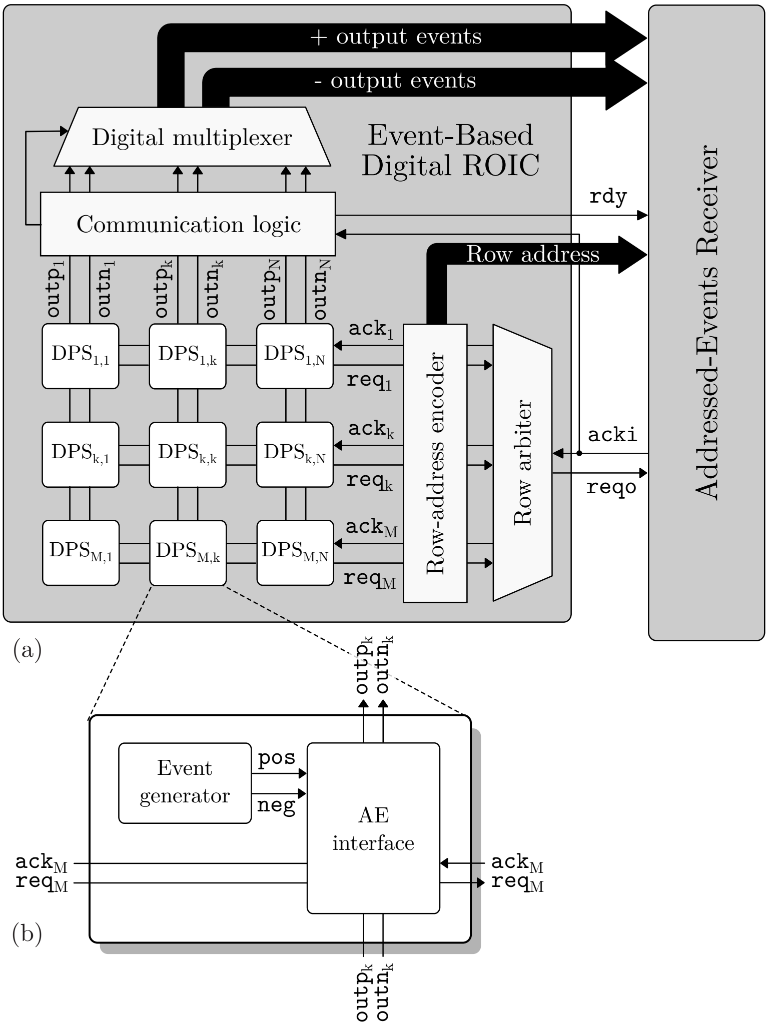

+ output events
- output events
Digital multiplexer
Event-Based Digital ROIC
Communication logic
rdy
Row address
Addressed-Events Receiver
outp1
outn1
outpk
outnk
outpN
outnN
DPS1,1
DPS1,k
DPS1,N
DPSk,1
DPSk,k
DPSk,N
DPSM,1
DPSM,k
DPSM,N
ack1
req1
ackk
reqk
ackM
reqM
Row-address encoder
Row arbiter
acki
reqo
(a)
outpk
outnk
Event generator
pos
neg
AE interface
ackM
reqM
ackM
reqM
(b)
outpk
outnk

Figure 3.3 Row-addressed parallel column-readout block diagram for the M×N MWIR imager of Fig. 3.1 (a) and in-pixel signaling detail (b).

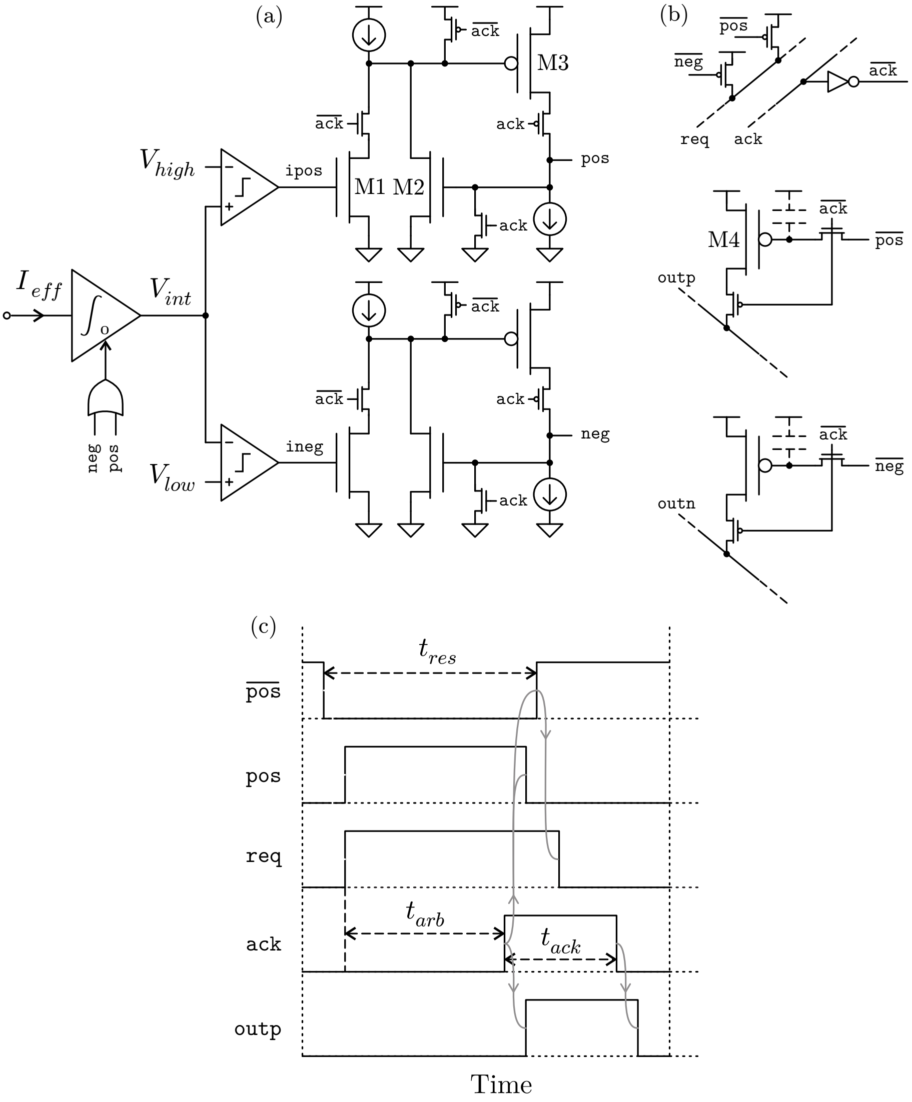

(a)
I_{eff}
V_{int}
V_{high}
V_{low}
o
neg
pos
-
+
ipos
ineg
M1 M2
M3
$\overline{\mathtt{ack}}$
ack
pos
neg
(b)
$\overline{\mathtt{pos}}$
$\overline{\mathtt{neg}}$
req
ack
M4
outp
outn
(c)
t_{res}
t_{arb}
t_{ack}
req
outp
Time

Figure 3.4 CMOS implementation of the in-pixel AER communication interface depicted in Fig. 3.3: high-speed state-holding comparator (a), pull-up handshaking circuit (b) and operation for $I_{eff} < 0$ (c). Small MOSFET symbols correspond to minimum size devices. Chronogram not in scale.

have single NMOS pull-down transistors which return them to gnd when pixels have no events calling request or output transmission. PMOS bus driving transistors need to be sized in such way that the transitioning order of signals is preserved. As the load of communication buses increases with FPA size, both power consumption and buffer dimensions can be optimized by use of staticizer-based [133] or actively-reset [135] keepers instead of static pull-ups. In these cases, pulling MOS devices are also driven by a peripheral handshaking circuit.

3.3 Self-Biasing and Temporal-Difference Filtering

3.3.1 Motivation and Design Proposal

The first stage of the DPS is intended to fulfill two key specs of frame-free compact-pitch pixel architectures: To provide internal generation of all pixel references by dark current reuse, and to supply high-pass filtering at the very low-corner frequencies (i.e. large time constants) required to suppress the dominant DC constituents of the detector current. Whereas present approaches are based on external biasing and fixed temporal and spatial contrast [64, 72, 136], the adopted externally-linear internally-nonlinear (ELIN) design of Fig. 3.5 implements in-line digital tuning capabilities so as to adapt temporal difference (TD) filtering to scene contents and minimize channel load during communication. Such functionality is achieved through adjustment of a dominant pole resistance R_{bias} by including compact D/A conversion inside each pixel. The resulting I_{bias} cancellation current is recycled for biasing purposes saving area and power consumption in every DPS.

Because quasi-DC filtering requires large-R_{bias} trimmers, and this devices have to be integrated in the limited area available inside pixel cells, a log-domain current-controlled MOS implementation in subthreshold is chosen [137]. In particular, the first-order low-pass filter prototype operates in agreement with the equivalent current-domain ordinary differential equation (ODE)

$$\frac{dI_{bias}}{dt} = 2\pi f_c \left(I_{det} - I_{bias}\right) \tag{3.9}$$

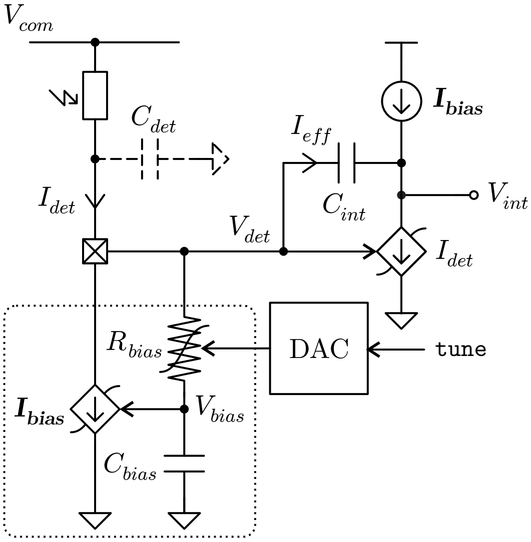


Figure 3.5 General scheme of the self-biasing and TD filtering proposal for the frame-free Compact-pitch imager of Fig. 3.1.

where I_{bias} includes all the non-desired low-frequency components of the incoming signal I_{det}, such as the PbSe detector dark current, and f_c stands for the corner frequency of this TD filtering. Applying the chain rule to the previous equation results in

$$\frac{\partial I_{bias}}{\partial V_{bias}} \frac{\partial V_{bias}}{\partial t} = 2\pi f_c \left(I_{det} - I_{bias}\right) \tag{3.10}$$

Taking benefit of the inherent log-companding $I_D = F(V_{GB}, V_{SB})$ function of the MOSFET biased in weak inversion forward saturation [96]

$$I_D = I_S e^{\frac{V_{GB} - V_{TO}}{nU_t}} e^{-\frac{V_{SB}}{U_t}} \tag{3.11}$$

the two I_{bias} and I_{det} voltage-controlled non-linear current sources of Fig. 3.5 can be replaced by NMOS devices with gates driven by V_{bias} and V_{det}, respectively. In this scenario, the equivalent non-linear ODE in the voltage-domain rewrites to

$$\frac{dV_{bias}}{dt} = 2\pi f_c \frac{nU_t}{I_{bias}} \left(I_{det} - I_{bias}\right) \tag{3.12}$$

that can be equivalently described as a non-linear transconductance controlled by I_{tune} driving a grounded capacitor C_{bias}:

$$\underbrace{C_{bias}\frac{dV_{bias}}{dt}}_{I_{cap}} = \underbrace{2\pi f_c n U_t C_{bias}}_{I_{tune}} \left(e^{\frac{V_{det}-V_{bias}}{nU_t}} - 1\right) \tag{3.13}$$

3.3.2 Compact CMOS Implementation

Fig. 3.6 presents a compact proposal for the CMOS realization of this block. This solution reuses M1 from the analog integrator that will be explained in Sec. 3.5.2 for the log-domain input compression $V_{det} = F^{-1}(I_{det})$, while M2 plays the role of the corresponding output expander $I_{bias} = F(V_{bias})$. Gate-driven (GD) and source-driven (SD) implementations of the non-linear transconductor driving C_{bias} are also depicted in Fig. 3.6(b) and (c), respectively.

The GD log filter is resolved by operating all transistors in the differential amplifier of Fig. 3.6(b) in weak inversion saturation following (3.11) except for M10, that can be in conduction. As a result, M8-M9 obey the particular equations:

$$I_{D8} = I_{tune} = I_S e^{\frac{V_{bias}-V_{TO}}{nU_t}} e^{-\frac{V_x}{U_t}} \tag{3.14}$$

$$I_{D9} = I_{tune} - I_{cap} = I_S e^{\frac{V_{det}-V_{TO}}{nU_t}} e^{-\frac{V_x}{U_t}} \tag{3.15}$$

Solving for I_{cap} results in the pursued non-linear transconductance of (3.13). The SD filter of Fig. 3.6(c) is realized by M6 operating in weak inversion

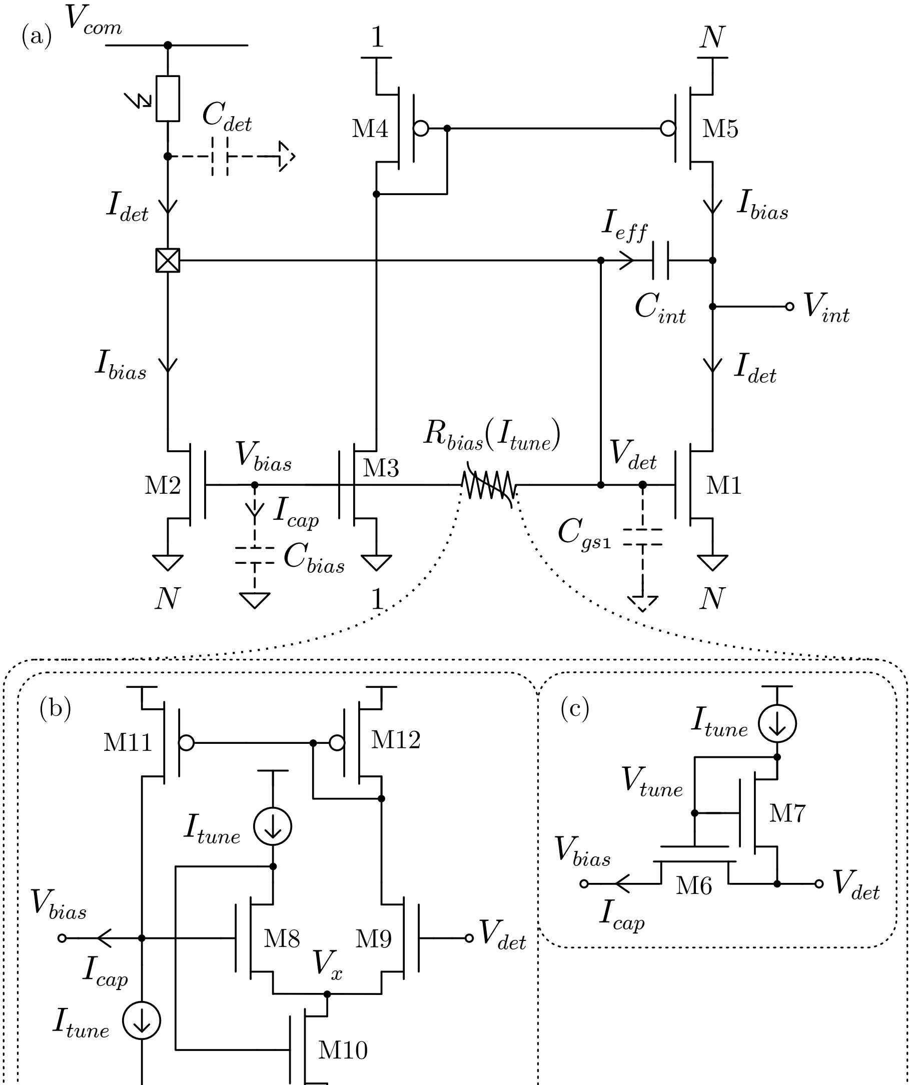

(a)
V_{com}
C_{det}
I_{det}
1
N
M4
M5
I_{bias}
I_{eff}
C_{int}
V_{int}
I_{bias}
I_{det}
$R_{bias}(I_{tune})$
V_{bias}
M2
M3
V_{det}
M1
I_{cap}
C_{bias}
C_{gs1}
N
1
N
(b)
M11
M12
I_{tune}
V_{bias}
I_{cap}
M8
M9
V_{det}
V_x
I_{tune}
M10
(c)
I_{tune}
V_{tune}
M7
V_{bias}
M6
V_{det}
I_{cap}

Figure 3.6 Simplified CMOS schematic of the proposed circuit for DPS self-biasing and TD filtering of Fig. 3.5 (a). GD (b) and SD (c) implementations for the non-linear resistor R_{bias}.

conduction [96] according to

$$I_D = I_S e^{\frac{V_{GB}-V_{TO}}{nU_t}} \left(e^{-\frac{V_{SB}}{U_t}} - e^{-\frac{V_{DB}}{U_t}} \right) \tag{3.16}$$

The matched device M7 operating in saturation supplies the required gate voltage tuning V_{tune} according to I_{tune}. In this case, the non-linear R_{bias} arises from the system of equations

$$I_{D6} = I_{tune} = I_S e^{\frac{V_{tune}-V_{TO}}{nU_t}} \left(e^{-\frac{V_{bias}}{U_t}} - e^{-\frac{V_{det}}{U_t}} \right) \tag{3.17}$$

$$I_{D7} = I_{cap} = I_S e^{\frac{V_{tune}-V_{TO}}{nU_t}} e^{-\frac{V_{det}}{U_t}} \tag{3.18}$$

which leads to an equivalent transconductance

$$I_{cap} = I_{tune} \left(e^{\frac{V_{det}-V_{bias}}{U_t}} - 1 \right) \tag{3.19}$$

The resulting voltage compression obtained by the log-domain processing is also exploited here to reuse the parasitic non-linear MOS capacitance of the expander transistor M2 as C_{bias}. Although the proposed circuit of Fig. 3.6(c) misses the subthreshold slope factor n of (3.13), no significant distortion is expected as this variable comes nearer to 1 in modern submicron technologies. In exchange, the SD cell offers larger area compaction and better matching than its GD counterpart. The digital tuning of this log-domain filter through I_{tune} is fully addressed in Section 3.4. Finally, the self-biasing capability of the DPS is obtained simply by mirroring the I_{bias} current level available in M3 and M5 to the other circuit blocks of the pixel.

Fig. 3.7 shows the small-signal circuit equivalent of the temporal-difference filtering stage when considering its main poles. Drain-to-source and integrator-load capacitances have been ignored because they are significantly lower than Miller C_{int} input and output analogues. Also, $R_{det} \ll 1/g_{md2}$ and $g_{mg1} \simeq g_{mg2}$. Under this conditions,

$$C_{in} = C_{det} + C_{gs1} \tag{3.20}$$

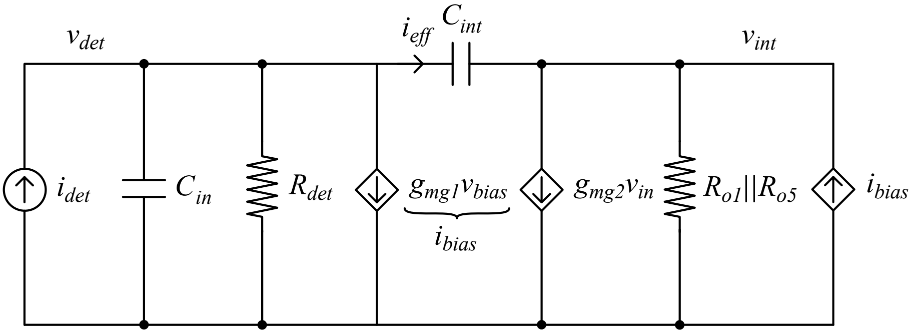


Figure 3.7 | Simplified small-signal model of the log-domain filtering circuit of Fig. 3.6(a).

The log-domain filter equation is

$$v_{bias} = \frac{v_{det}}{R_{bias}C_{bias}+1} \tag{3.21}$$

Applying Kierchoff's current law at v_{det} and v_{int} nodes,

$$\frac{v_{det}\left(1+R_{det}C_{in}s\right)}{R_{det}} = i_{det} - g_{mg2}v_{bias} - i_{eff} \tag{3.22}$$

$$2g_{md1}v_{int} = g_{mg2}v_{bias} - g_{mg1}v_{det} + i_{eff} \tag{3.23}$$

Finally, by simple Ohm's law

$$i_{eff} = C_{int}s\left(v_{det} - v_{int}\right) \tag{3.24}$$

To investigate alternating current (AC) signal performance, one can define the time constants

$$\begin{aligned} \tau_b &\doteq R_{bias}C_{bias}; & \tau_i &\doteq R_{det}C_{in}; \\ \tau_c &\doteq R_{det}C_{int}; & \tau_o &\doteq \frac{C_{int}}{g_{md1}+g_{md5}}; \end{aligned} \tag{3.25}$$

and DC gains

$$G_{in} \doteq g_{mg2} R_{det}; \qquad G_{out} \doteq \frac{g_{mg1}}{g_{md1} + g_{md5}}; \tag{3.26}$$

Solving for

$$\begin{aligned} \frac{i_{bias}}{i_{det}} &= g_{mg1} \frac{v_{bias}}{i_{det}} \\ &= \frac{G_{in}(\tau_o s+1)}{G_{in}(\tau_o s+1)+(\tau_b s+1)((\tau_i+\tau_c)s+1)(\tau_o s+1)-\tau_c s[\tau_o s(\tau_b s+1)-G_{out}\tau_b s]} \end{aligned} \tag{3.27}$$

Provided that $\tau_i \ll \tau_c$ (i.e. $C_{in} \ll C_{int}$), the former equation can be simplified to the second-order low-pass filter function

$$\frac{i_{bias}}{i_{det}} = \frac{G_{in}}{G_{in}+1} \frac{(\tau_o s + 1)}{\frac{\tau_b}{G_{in}+1}\left[(G_{out}+1)\tau_c + \tau_o\right] s^2 + \left(\tau_o + \frac{\tau_c + \tau_b}{1+G_{in}}\right) s + 1} \tag{3.28}$$

In order to avoid ringing, the root polynomial in (3.28) should contain two non-complex conjugated poles, that is

$$((G_{out}+1)\tau_c + \tau_o)^2 > 4\left(\tau_o + \frac{\tau_c + \tau_b}{G_{in}+1}\right) \tag{3.29}$$

Given G_{in},$G_{out} \gg 1$ and $\tau_b \gg \tau_c$ (3.29) simplifies to

$$\left(\tau_o + \frac{\tau_b}{G_{in}}\right)^2 > 4 \frac{\tau_b}{G_{in}} \left(G_{out}\tau_c + \tau_o\right) \tag{3.30}$$

which, for

$$\frac{\tau_b}{\tau_c} \gg G_{out} \tag{3.31}$$

furtherly shortens to

$$\frac{\tau_b}{R_{det}^2 C_{int}} > 4\frac{g_{mg1}^2}{g_{md1} + g_{md5}} \tag{3.32}$$

Summing up all previous conditions to the prior equation leads to some interesting results:

- In order to dodge the stability issues of introducing a third-order response in (3.28), both C_{det} and C_{gs1} need to take values markedly lower that C_{int}. Considering the detector capacitive values plotted in Fig. 1.7(a) makes the use of an input compensation stage mandatory. The compact topology described in 2.9 can be adapted for this purpose, in provision of Fig. 1.7(b) and the farther operational restrictions of the filtering loop.

- The product of g_{mg1} and g_{mg2} with their respective resistive loads at v_{det} and v_{int} need to provide sufficient gain to fix the dominant pole to v_{bias} and skip noticeable degeneration of the integrator response. These two transconductances are optimized against power consumption as M1 and M2 operate in subthreshold.

- Overshooting can be avoided by detaching the poles introduced by C_{int} from the main low-pass filtering one. The particular conditions to accomplish are stated in (3.31), (3.32) and extend to $\tau_b \gg \tau_c$. Because implementations of R_{bias} and C_{bias} are respectively limited by transistor leakage and pixel pitch, this last spec translates in practice into limited gain values in the CTIA and input compensation stages.

3.4 Digital Contrast Tuning

3.4.1 Motivation and Design Proposal

The log-domain filter of Sec. 3.3 demands a robust mechanism capable to deliver the low-current tuning levels that fix its dominant pole continuously in time. Because such low-noise levels are hardly achievable if this signal is not generated internally in the pixel, and because the frame-free pixel is intrinsically tied to compact-pitch constrains, the design of such circuitry represents a research challenge on itself. State-of-the-art neuromorphic solutions implement compact current DACs made with calibratable MOS ladder structures [138, 139]. These designs, however, rely on the generation of a reference current, either externally or internally to the cell, that make them not suitable for sub-nA current calibration.

The phase-locked loop (PLL) scheme of Fig. 3.8 represents an attractive candidate for the cited objectives of this sub-chapter: Firstly, it can be easily tuned with external digital programming trains inheriting the well-known noise robustness of binary signaling; secondly, due to the internal generation of the I_{tune} signal, this electrical variable is adjusted in the feedback loop so configured independently to device mismatch along the focal plane; finally, due to the low-current values pursued in the block, tuning signals are presumed to be of low-frequency and introduce limited disturbance to in-pixel event generation.

The PLL illustrated in Fig. 3.8 consists of four fundamental components: a phase-frequency detector (PFD), a charge pump (CP), a loop filter (Z) and a voltage-controlled oscillator (VCO). The PFD compares the frequency and phase of the control signal `tune` with a reference feedback signal `vco` to produce the reciprocal error signals `slow` and `fast`. The Z impedance filters the error injected by the CP so as to deliver a low-frequency signal V_{ctrl}, which is converted to I_{tune} in the transconductance that composes the first stage of the VCO block. The current-controlled oscillator (CCO) closes the loop by generating a pulsating `vco` signal of frequency proportional to I_{tune}. The latter can be easily copied to the temporal-difference filter by the use of simple current-mirroring techniques.

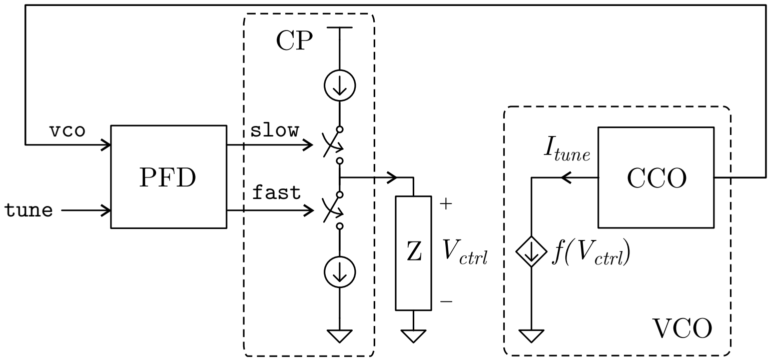


Figure 3.8 PLL-based proposal for the dynamical tuning of the log-domain filter in the frame-free Compact-pitch imager of Fig. 3.1.

3.4.2 Compact CMOS Implementation

The proposed locked-loop syntonization is integrated into the compact implementation of Fig. 3.9(a), which includes a digital PFD, a low-leakage CP and a minimalist VCO. In this figure, V_{ctrl}-to-I_{tune} conversion is achieved by the output-current source M1, and the external-reference frequency is unfolded into `tune1` and `tune2`, the former being used as pulse reset inside the VCO. The error signals `slow` and `fast` are in this case filtered by C_{ctrl} and fed back according to Fig. 3.9(b) to ensure that the regenerative oscillator M2-M4 locks at

$$f_{tune} = \frac{I_{tune}}{2V_{thvco}C_{vco}} \quad \text{where} \quad V_{thvco} = nU_t \ln\left(\frac{1+Y}{1+1/X}\right) \tag{3.33}$$

where V_{thvco} is the equivalent threshold voltage of the comparator if M4 and M5 are working in weak inversion; M6,M10-M11 provide enough positive feedback to avoid metastability in the rising and falling edges of `vco`. Following (3.13), a linear tuning of the TD corner frequency is achieved according to:

$$f_c = \frac{1}{\pi}\frac{C_{vco}}{C_{bias}} \ln\left(\frac{1+Y}{1+1/X}\right) f_{tune} \tag{3.34}$$

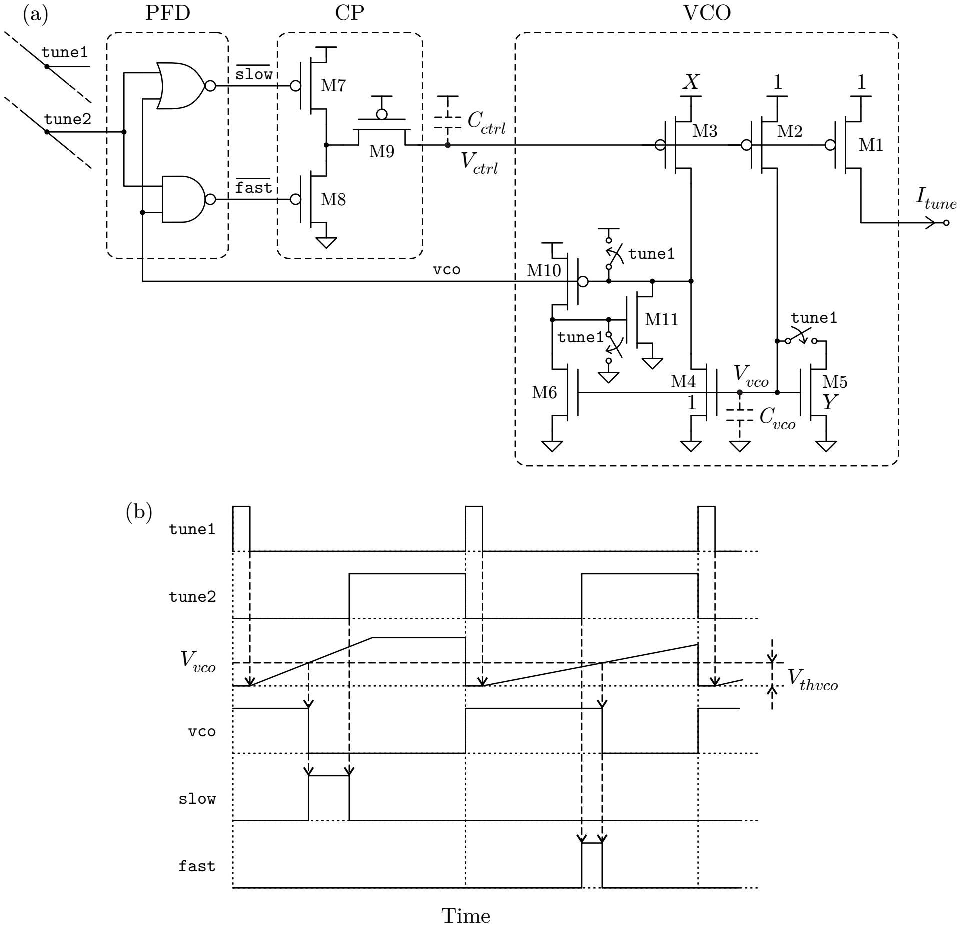

(a)
PFD
CP
VCO
tune1
tune2
$\overline{\texttt{slow}}$
$\overline{\texttt{fast}}$
M7
M8
M9
C_{ctrl}
V_{ctrl}
X
1
1
M3
M2
M1
I_{tune}
vco
M10
tune1
M11
tune1
tune1
M6
M4
1
V_{vco}
C_{vco}
M5
Y
(b)
tune1
tune2
V_{vco}
vco
slow
fast
V_{thvco}
Time

Figure 3.9 Simplified CMOS schematic (a) and operation (b) for the PLL-based tuning of the log-domain low-pass filter used in Fig. 3.8.

The triple-PMOS CP topology illustrated in Fig. 3.9(a) is made of two PMOS switches so as to equal charge injection into V_{ctrl}, and attenuates the pulsating phase error seen in this same node in order to avoid charge coupling into the integrating `vco` reference. Biasing M1-M3 in strong inversion by providing long channels and low aspect ratios reduces noise contributions at V_{vco}, and avoids unstability by reducing the VCO gain via increasing C_{ctrl} and lessening g_m in these transistors. Larger C_{ctrl} values also lead to lower KTC noise in the loop filter.

Apart from the higher robustness of distributing a digital kHz-range frequency reference `tune1,2` instead of an analog pA-range current reference I_{tune} along the FPA, the in-pixel tuning circuit of Fig. 3.9 also compensates for PVT circuit dependencies by adapting I_{tune} value to the particular technological parameters of each DPS. Such an external digital control allows to adjust the TD of the DPS on-the-fly.

3.5 Reset-Insensitive Spike-Counting ADC

3.5.1 Motivation and Design Proposal

Most spike-counting pixel designs in literature are implemented by means of feedback and hard-reset, and dominate the current AER DPS scene [124, 90, 70]. Nonetheless, this technique suffers from an intrinsic limitation: the impossibility of integrating I_{eff} during the non-zero reset time (T_{res}) of C_{int} in its analog integrator, which generally results in higher power consumption and imposes an important limitation in the final event rate for fast imaging applications. Considering ideal pixel current-to-frequency conversion for event requests:

$$f_{req} = \frac{|I_{eff}|}{C_{int}V_{th}} \tag{3.35}$$

As advanced by (2.15), CTIA-based PDMs like the topologies presented in

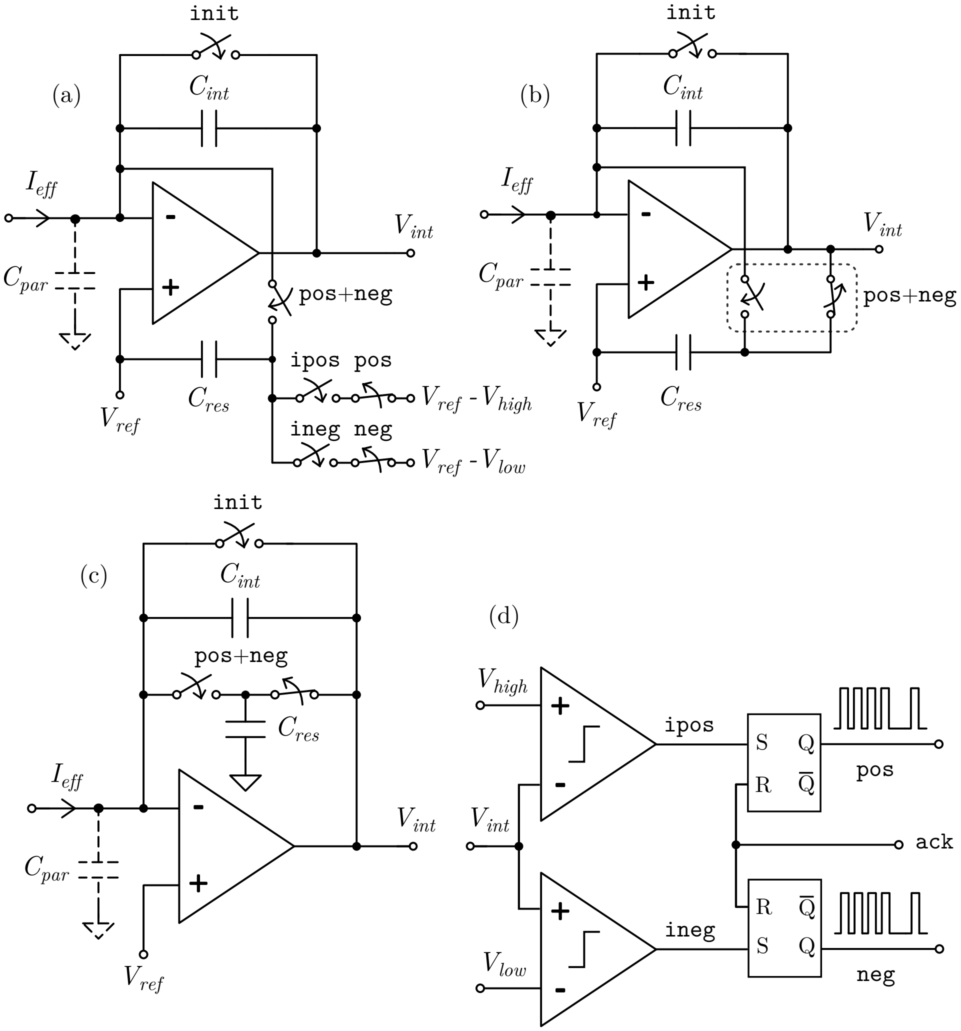
Sec. 2.4 display in practice dead times that cause the non-linear saturation

$$f'_{req} = \frac{f_{req}}{1 + T_{res} f_{req}} \tag{3.36}$$

Obviously, this curve saturation is especially noticeable for high-speed imagers, when T_{res} is comparable to the spike period itself. Nevertheless, the dead time can also play an important role in AER imagers already at low frequencies due to the variability of the arbitration delay (t_{arb}) of Fig. 3.4. The above issue is addressed here by proposing the three high-speed analog integrator topologies of Fig. 3.10(a, b and c), where $V_{th} = V_{high} - V_{ref} = V_{ref} - V_{low}$.

In all cases, the main idea is not to block the integration of I_{eff} during T_{res} but to reset C_{int} injecting a controlled charge by means of a matched capacitor (C_{res}). The CTIAs of Fig. 3.10(b,c) operate as follows: during initialization (`init` $= 1$), the analog integrator is reset, while C_{res} remains connected to V_{int}; once in acquisition (`init` $= 0$), C_{int} integrates the detector current I_{eff} while C_{res} tracks the offset, the low frequency noise and the output signal itself of the first stage; finally, when any of the fixed thresholds V_{high} or V_{low} is reached, the circuit of Fig. 3.10(d) generates a spike (`pos` $= 1$ or `neg` $= 1$), which causes C_{res} to be connected to the input of the analog integrator. As a result, the charge stored in C_{int} is compensated by C_{res} and the reset is performed. Since C_{res} is continuously sampling the offset and the low frequency noise of the analog integrator, it also implements the CDS function. The CTIA of Fig. 3.10(a) executes the same function by pre-charging C_{res} at a fixed differential voltage during the propagation delay between the signals `ipos-ineg` and their latched complementaries `pos-neg`. The table shown in this same Fig. 3.10 also cross-compares all three schemes in terms of dead-time insensitivity, CDS capabilities and number of needed low-impedance voltage sources. By including (c), the adopted double-threshold level PDM topology avoids dead integration times, attenuates 1/f noise, and has no low output-impedance source requirements.

Fig. 3.11 depicts PDM operation for all ideal, hard-reset and lossless-reset variants. Due to low-current biasing levels in the analog integrator and the comparator blocks, or due to low-voltage supply operation for the switching devices, the event duration of classical feedback-and-reset circuits cannot


(a)
init
C_{int}
I_{eff}
C_{par}
-
+
V_{int}
pos+neg
C_{res}
V_{ref}
ipos pos
V_{ref} - V_{high}
ineg neg
V_{ref} - V_{low}
(b)
init
C_{int}
I_{eff}
C_{par}
-
+
V_{int}
pos+neg
C_{res}
V_{ref}
(c)
init
C_{int}
pos+neg
C_{res}
I_{eff}
C_{par}
-
+
V_{int}
V_{ref}
(d)
V_{high}
+
-
ipos
S Q
R $\overline{Q}$
pos
V_{int}
ack
+
-
V_{low}
ineg
R $\overline{Q}$
S Q
neg

CTIA	Dead time	CDS	Voltage sources
(a)	✓	×	××
(b)	✓	✓	×
(c)	✓	✓	✓

Figure 3.10 Proposed lossless-reset integrate-and-fire ADC architectures and comparative performance: hard-fixed charge subtraction (a), and differential (b) and absolute (c) OpAmp-charged subtraction. Window detection part common to all three schemes (d).

be null in practice. As depicted in Fig. 3.11(b), some time is lost to reset C_{int} at each spike generation. According to this same figure, no integration is possible during this event time, so the resulting spike frequency in Fig. 3.11(b) is decreased compared to Fig. 3.11(a). In contrast, Fig. 3.11(c) linearly combines the integration of both the charge coming from I_{eff} and from C_{res} in C_{int} during the reset phase. The spike frequency is no longer dependent on the reset time and matches the ideal target of Fig. 3.11(a). In fact, just a minimum event time is required to ensure complete charge redistribution between C_{res} and C_{int}. Its particular value is not relevant at this point.

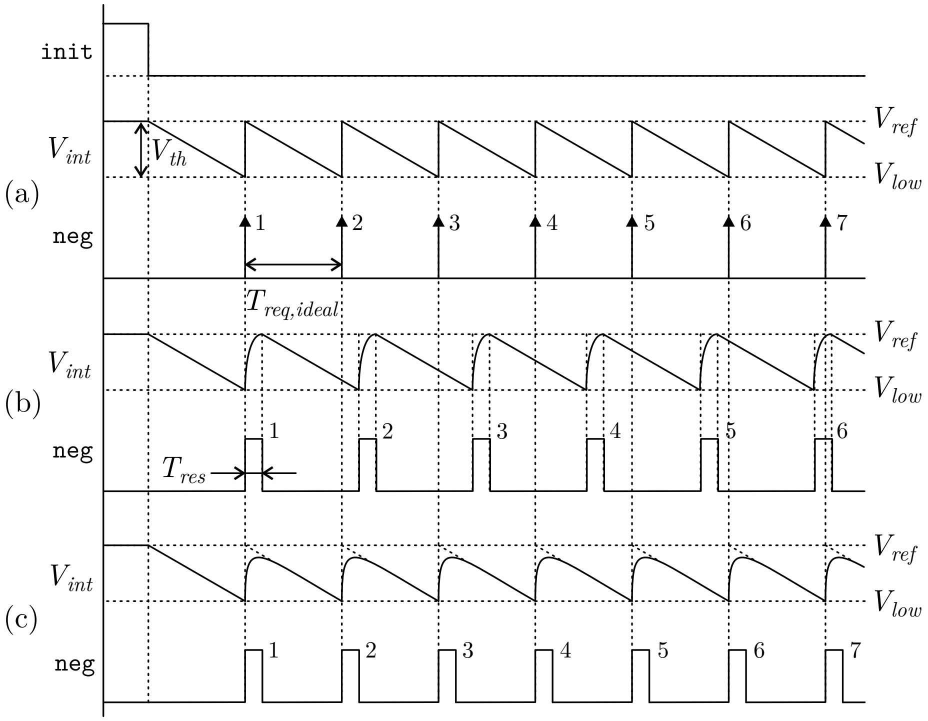

init
(a)
V_{int}
V_{th}
V_{ref}
V_{low}
neg
1
2
3
4
5
6
7
$T_{req,ideal}$
(b)
V_{int}
V_{ref}
V_{low}
neg
T_{res}
1
2
3
4
5
6
(c)
V_{int}
V_{ref}
V_{low}
neg
1
2
3
4
5
6
7

Figure 3.11 Integrate-and-fire operation according to the ideal (a), classical (b) and proposed (c) reset schemes ($I_{eff} > 0$ case) of Fig. 3.10. In this example, classical operation losses the charge equivalent to 1 spike compared to ideal behavior. Figure not in scale.

As shown in Fig. 3.12, reset losses are specially important at the highest request frequencies, where the spike period is comparable to the reset time, and cause saturation of the ADC curve. Deviations can already exceed 10% for a defined range of three decades of f_{req} and a $T_{res}/T_{req4\sigma}$ of 0.1%, forcing to increase biasing in the analog blocks of the DPS in order to achieve the desired fast frame-rate performance. Thanks to this circuit strategy, ADC linearity is no longer dependent on the reset time, making low-power and low-voltage operation compatible with high event rates.

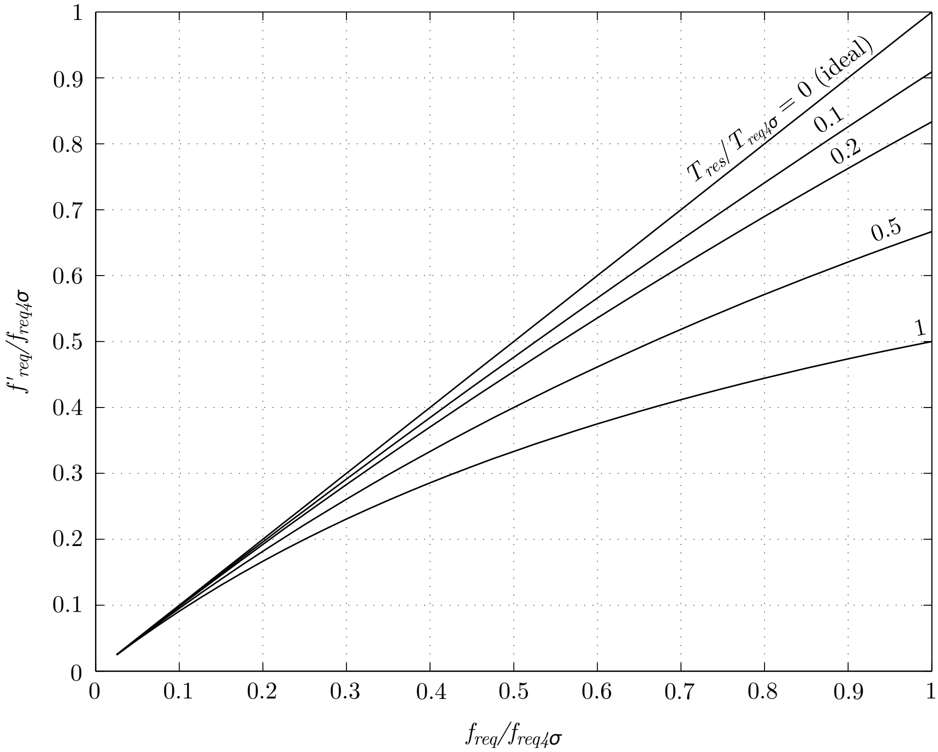


Figure 3.12 Event request frequency dependency on reset time as described in (3.36). Values normalized to an expected maximum request frequency value $f_{req4\sigma} = \overline{f_{req}} + 4\sigma(f_{req})$.

3.5.2 Compact CMOS Implementation

Attending the considerations of Sec. 2.4.2, the circuit implementation of Fig. 3.13(a) is introduced as compact CMOS solution for the initial PDM stage of Fig. 3.10(c). In this schematic `init` stands for the imager general initialization trigger. Supposing weak inversion forward saturation for M1-M3, the equivalent quantization level of the window comparator is

$$V_{th} = nU_t M \ln(P) \tag{3.37}$$

As it can be seen, threshold is increased by scaling up the ratio $1 < M < 2$ between reset and integrating capacitors. In order to save extra area and power in the design, V_{low} threshold level can also be set by lowering the biasing of M3 to I_{bias}/P. In practice, technology mismatching between C_{int} and C_{res} causes a small offset in V_{th}, but the resulting gain errors are negligible compared to the process deviations of the C_{int} absolute values. Furthermore, charge injection is similar to conventional spiking due to the fact that the `init` switch is not operated during A/D conversion and other reset switches work complementary. Switches are implemented using minimum size transistors for minimum charge injection.

When T_{res} becomes comparable to inter-spike intervals, the generation of a second event while awaiting the acknowledge signal would surpass the reset charge level. As a result, V_{ref} levels would be unrecoverable by this method. The digital circuit of Fig. 3.13(a) allows to overcome such risk by detecting second events when both `pos` and `neg` signals are still being latched by the memory cells of Fig. 3.4(a). The double-inverter delays stored events so as to avoid spurious transitions of the `init` signal at the start of the reset phase.

Sizing of M1 attends a criteria alike to the one highlighted in Sec. 2.4.2. Thanks to the new reset scheme adopted in the CTIA, the limited slew-rate obtained from low-power biasing has little effect on the linearity of the integrate-and-fire stage. The comparison level V_{th} should be programmed according to circuit noise levels as explained in this same Sec. 2.4.2. Because the noise bandwidth can be now controlled externally, it can be extended up to f_{req} beyond noise corner frequencies. In this cases, thermal noise becomes the dominant component of readout circuitry, and proportional to g_{mg1}. Thanks to the operational flexibility of frame-free imagers, the predominant high-frequency noise of temporal-difference filtering and CTIA blocks can be shrunk with a rate close to the square-root of AER-monitoring frequency reduction.

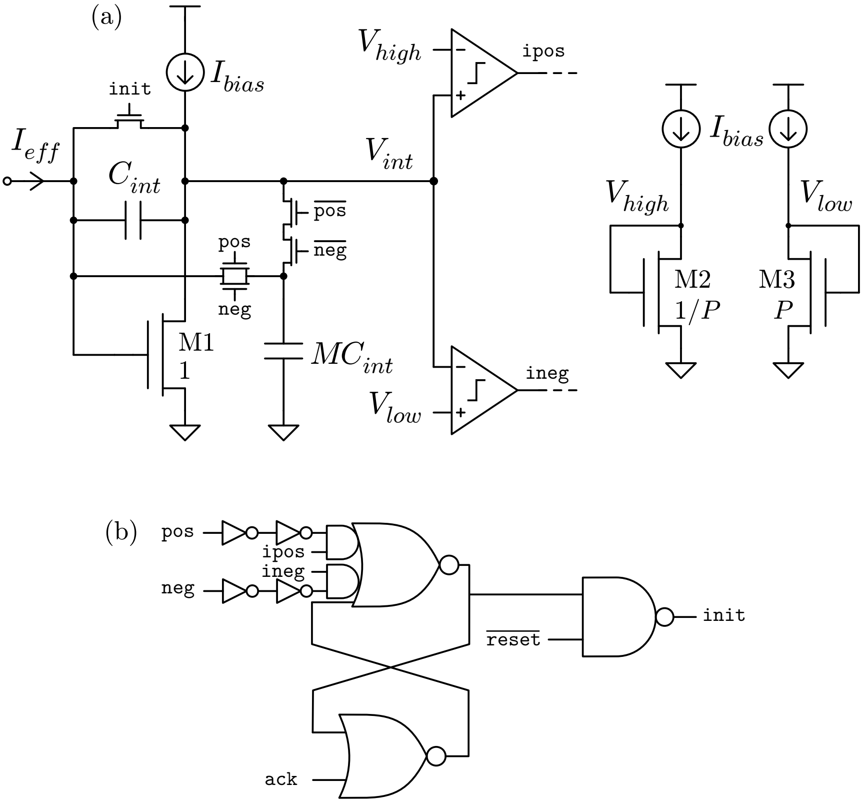

(a)
I_{bias}
init
I_{eff}
C_{int}
V_{int}
$\overline{\text{pos}}$
$\overline{\text{neg}}$
pos
neg
M1
1
MC_{int}
V_{high}
ipos
ineg
V_{low}
I_{bias}
V_{high}
V_{low}
M2
1/P
M3
P
(b)
pos
neg
ipos
ineg
$\overline{\text{reset}}$
init
ack

Figure 3.13 | CMOS implementation of the lossless-reset integrate-and-fire ADC of Fig. 3.10(c) (a) and overintegration-guarding circuit (b).

3.6 Fair AE Arbitration

3.6.1 Motivation and Design Proposal

The AER communication blocks of this section are conceived with two key requirements in mind: minimizing transmission latency and maximizing throughput in front of event collisions. Provided AER systems access randomly to a shared output channel, they are almost unavoidably tied to include some form of arbitration. Sec. 3.2.1 analyzed the trade-offs and considerations that must be taken into account when designing event-based ROICs. The proven inefficiency of first unfettered channel protocols like additive links on-line Hawaii area (ALOHA) has been progressively translated into more efficient arbiter-tree designs: The classical arbiter circuit [140] organizes in $\log_2(N)$ binary selection stages. As every level introduces an equivalent delay, and queued events are not processed until the whole `req-ack` cycle is finished, these circuitry introduces a time penalty proportional to $\log_2(N)$. Such value can become considerably large when the number of pixels being handled also becomes copious. The greedy arbiter [132] optimizes the arbiter tree to handle simultaneous requests locally in each binary cell. In the case of event collision, the non-prioritary input is processed once its colliding counterpart is handled. When more than two events collide, the order of attendance is defined by their location in the hierarchy of the tree. One disadvantage of this arbitration circuit resides in its "unfairness" i.e. highly active rows tend to hold on the bus in detriment of quieter emitting clusters. More recent implementations like [133, 141, 142] provide fair arbitration by collision-only toggling while keeping simultaneous request propagation to minimize delays.

Once access has been granted to a specific row or column, its position is encoded into a compact address code for the AER output channel. Conventional AER encoding topologies [66] employ a logarithmic encoder to codify the location, adding up to a total amount of $N_{pix} \log_2(N_{pix})$ transistors (i.e. $\log_2(N_{pix})$ devices per acknowledge line). Because each level of the tree can be used, in fact, to select the value of address bits, more compact alternatives distribute address encoding along the arbiter to a total transistor count of N_{pix} with reduced capacitive loads [143]. The approach of Fig. 3.14 extends previous solutions by implementing a novel binary tree for

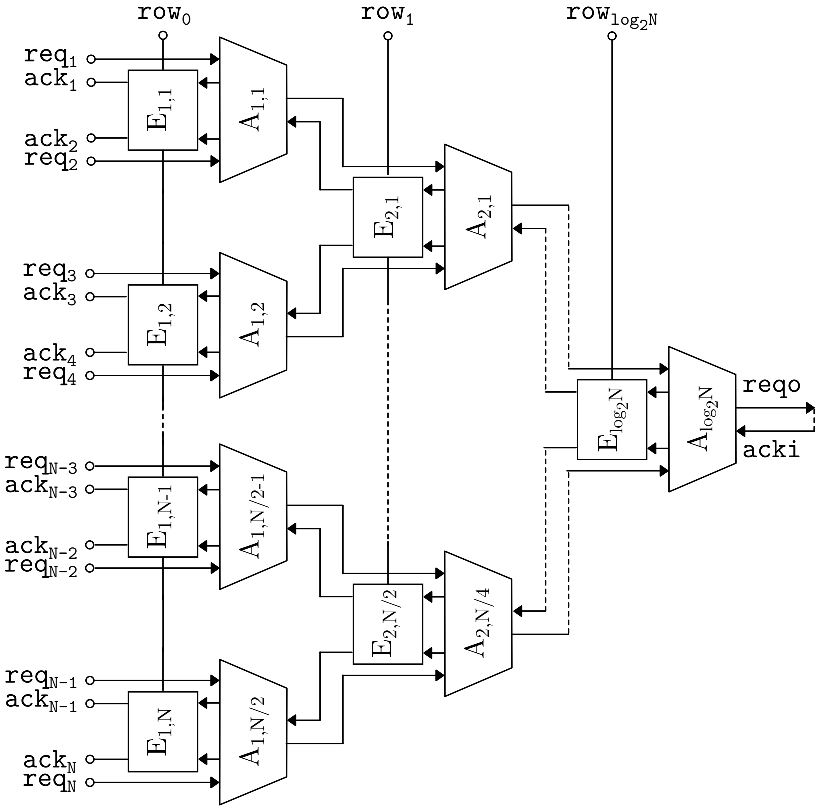

row0
row1
rowlog2N
req1
ack1
ack2
req2
req3
ack3
ack4
req4
reqN-3
ackN-3
ackN-2
reqN-2
reqN-1
ackN-1
ackN
reqN
E1,1
A1,1
E1,2
A1,2
E1,N-1
A1,N/2-1
E1,N
A1,N/2
E2,1
A2,1
E2,N/2
A2,N/4
Elog2N
Alog2N
reqo
acki

Figure 3.14 Binary arbiter tree and distributed row encoding proposal for the frame-free Compact-picth MWIR vision architecture of Fig. 3.1.

fair arbitration at row level together with a distributed minimalist output encoder. In this topology, all row-wise asynchronous requests are successively arbitered in pairs (A cells) throughout the tree until obtention of a unique request `reqo` output. The acknowledge feedback loop can be directly controlled by an external AER receiver, allowing to investigate the resilience of the frame-free architecture to large arbitration delays. E cells encode the row address at the returning `ack` path, as this signal progresses from higher to lower levels of the tree.

Fig. 3.15 illustrates the behavior of three different arbiters: unfair, fair with collision-only toggling, and this scheme. The first rule uses a fixed priority thus one input is always handled before the other, whereas the second circuit commutes priority every time two simultaneous requests are risen. In the proposed arbiter, the priority allocation is not fixed, random or simply toggled at collision but toggled between last attended requests. Compared to other fair arbitration schemes, this new algorithm unmasks less active spiking groups by dynamically assigning a higher access priority as their frequencies fade in front of other requests. In this way, visual representation is granted to all busy areas of the focal plane.

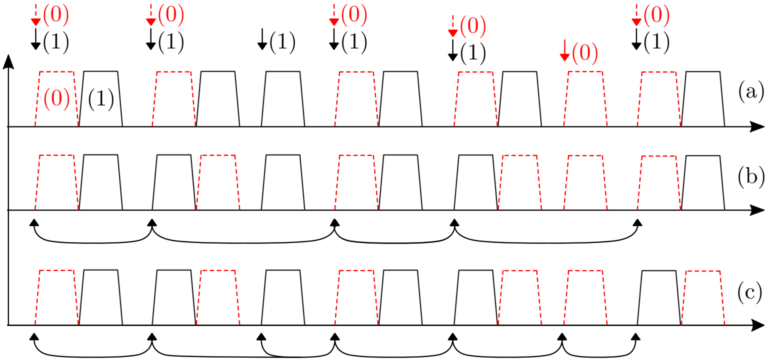


Figure 3.15 Comparative chronogram showing event acknowledgement between alternative arbitration strategies: fixed priority [132] (a), collision-only priority toggling [133] (b) and last-attended priority toggling (this work, c). Top arrows indicate event collision, double arrows causality in priority switching.

3.6.2 Compact CMOS Implementation

The basic arbitration-encoding module is illustrated in Fig. 3.16. Each arbitration cell is composed of three functional units: arbitration with priority selection, request propagation and acknowledge propagation. The arbitration unit of Fig. 3.16(b) is constituted of two SR latches composed of two cross-coupled NAND gates each. The NANDs of the first SR latch have programmable pulling-down capabilities as shown in Fig. 3.16(c), and their outputs correspond to the priority signals $\overline{\texttt{prty<0>}}$ and $\overline{\texttt{prty<1>}}$. The binary level of these last two signals is assigned taking advantage of the prohibited state of the SR latch, by means of dinamically biasing the NAND gates that compose them. Thus, `f<0>` and `f<1>` outputs of the second SR latch are fed back to the NAND elements of the former, which are conceived to speed up the propagation of logic zeros in those who receive this input at high level. In other words, a '0' logic is fixed as long as the previous state of the priority signal has been '1'. Table 3.1 summarizes the circuit operation of this element.

`reqin<0>`	`reqin<1>`	$\overline{\texttt{prty<0>}}$	$\overline{\texttt{prty<1>}}$	`f<0>`	`f<1>`
0	0	1	1	`f<0>`*	`f<1>`*
0	1	1	0	0	1
1	0	0	1	1	0
1	1	0 if `f<0>`* = 0, `f<1>`* = 1	1	1	0
		1 if `f<0>`* = 1, `f<1>`* = 0	0	0	1

Table 3.1 Truth table of the arbitration unit depicted in Fig. 3.16. * means current state.

The OR gate propagates the request to the next A cell toward the output of the tree at the same time acknowledge assignment is being processed. The two NAND gates of the acknowledge unit distribute this signal toward the pixel in those branches with active request (`reqin<i>` = 1) and priority conceded ($\overline{\texttt{prty<0>}} = 0$).

Concerning row encoding, every E cell is synthesized following the schematic of Fig. 3.16(a). Even though this topology includes more devices than other distributed encoding circuits [143], it does so in the periphery of the ROIC, usually a region with relaxed sizing constrains. In exchange, it provides glitch protection by using both acknowledge lines of the A cell to codify the addresses, and balances the loads seen at acknowledge lines to inverter inputs. This last feature equalizes the propagation delay of all returning `ack` signals, improving the overall fairness of the AER module.

When defining the physical layout of all CMOS A and E cells, special attention has to be focused on balancing minimal delays at the multiple `ack` and `req` nodes of the tree. This can be achieved by two means: the definition of symmetrical designs while avoiding the presence of parasitics over the use of top metals for inter-cell connectivity and multiple contacts in the routing; and the employment of compact MOSFET devices to drive the lines already optimized in the previous action. The number of encoding and arbitrating devices scale up exponentially with the number of spiking clusters to process, and so does power consumption. Furthermore, load inequalities along both ways of the arbiter manifest in the form of fixed-pattern jitter σ^2_{arb} that adds as equivalent input noise leveraging NETD as pointed out in (1.6). To ensure an adequate operation of the arbitration unit, differences between pull-up times in the dynamically-biased NAND of Fig. 3.16 must be larger than temporal jitter components at this point.

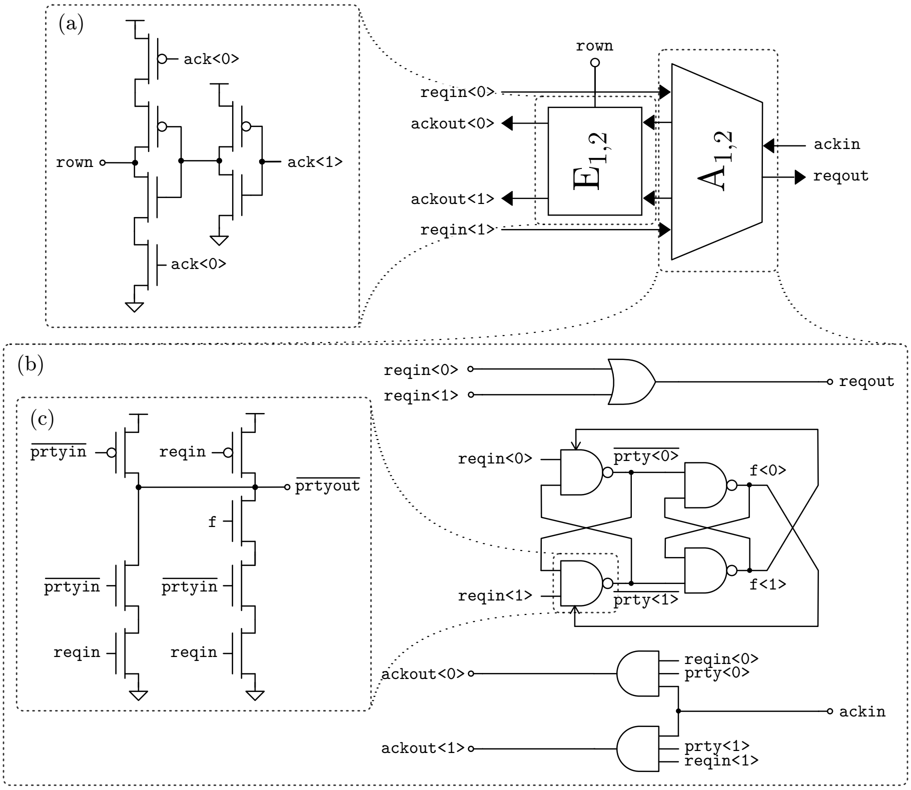

(a)
ack<0>
rown
ack<1>
ack<0>
rown
reqin<0>
ackout<0>
$E_{1,2}$
$A_{1,2}$
ackin
reqout
ackout<1>
reqin<1>
(b)
reqin<0>
reqin<1>
reqout
reqin<0>
$\overline{\text{prty<0>}}$
f<0>
reqin<1>
$\overline{\text{prty<1>}}$
f<1>
ackout<0>
reqin<0>
prty<0>
ackin
ackout<1>
prty<1>
reqin<1>
(c)
$\overline{\text{prtyin}}$
reqin
$\overline{\text{prtyout}}$
f
$\overline{\text{prtyin}}$
$\overline{\text{prtyin}}$
reqin
reqin

Figure 3.16 | CMOS implementation of the basic row-encoder (a) and arbiter (b) cells, and the programmable pull-down NAND gate used in the design of the latter (c).

4

Pixel Test Chips in 0.35μm and 0.15μm CMOS Technologies

The next two chapters report the development of both frame-based and frame-free vision sensor cores for uncooled MWIR fast imaging as concrete application examples for the FPA architectures presented in Chapter 2 and Chapter 3. At present, three main layout realizations of the frame-based Smart digital pixel sensor (DPS-S) and one version of the frame-free Compact-pitch digital pixel sensor (DPS-C) have been integrated in 0.35μm 2P4M and 0.15μm 1P6M CMOS technologies, respectively. They are introduced in this chapter. A test vehicle was created for each version, and experimental characterization was performed at every stage so as to identify critical design issues and address them in succeeding full-custom implementations.

The imagers of Chapter 5 were fabricated to validate both research lines at focal-plane level. During their design, special attention was devoted on providing electrical test ICs independent of the PbSe detector for first pixel prototypes. For this purpose, an ASIC test platform was investigated as well, and fabricated in the in-house low-cost 2.5 μm 2P1M CMOS technology of the IMB-CNM(CSIC).

4.1 A 100μm-Pitch Smart Pixel with Offset Auto-Calibration and Gain Programming

Like all posterior implementations of the frame-based DPS, the 100μm-pitch frame-based Smart digital pixel sensor (DPS-S100) incorporated the functionality of Sec. 2.1 to fulfill the practical specifications of Table 4.1. This first chip was conceived as a concept demonstrator of the fully-digital FPN-compensated self-biased architecture of Fig. 4.1(a), including the dark current self-cancellation scheme of Fig. 2.11(b), the SC-DAC of Fig. 2.19, a 10-bit version of the ripple-counter based digital interface presented in Fig. 2.7 and the simplified PDM CMOS implementation of Fig. 4.1(b). A basic double-switch reset scheme and the regenerative comparator M14-M17 were employed in this pixel.

Parameter	**Value**	**Units**
Dark current range	0.5 to 2	μA
Effective current range	1 to 1000	nA
Maximum input capacitance	15	pF
Frame time	1	ms
Supply voltage	3.3	V
Maximum power consumption	10	μW
Pitch	200×200	μm
Minimum readout resolution	8	bit

Table 4.1 | Operational specifications of the industrial DPS prototypes for frame-based Smart imagers.

The DPS cells of this library are controlled through the I/O signals of Table 4.2 and the chronogram of Fig. 4.2, where `X`, `p` and `w` stand for the number of serially-connected DPSs, typically the width or height of the FPA, the length of the programming word and the read-out word, respectively.

Besides row I/O and power supply connections, 5 global signals are used to control the DPS: `cal` enables dark current self-calibration during a dummy integration period with no illumination; `edac` activates gain tuning, `count` selects between acquisition or communication mode, `ninit` initializes acquisition and `clk` synchronizes digital program-in/read-out communications. The imager operates in the two main modes of Fig. 4.2: acquisition and

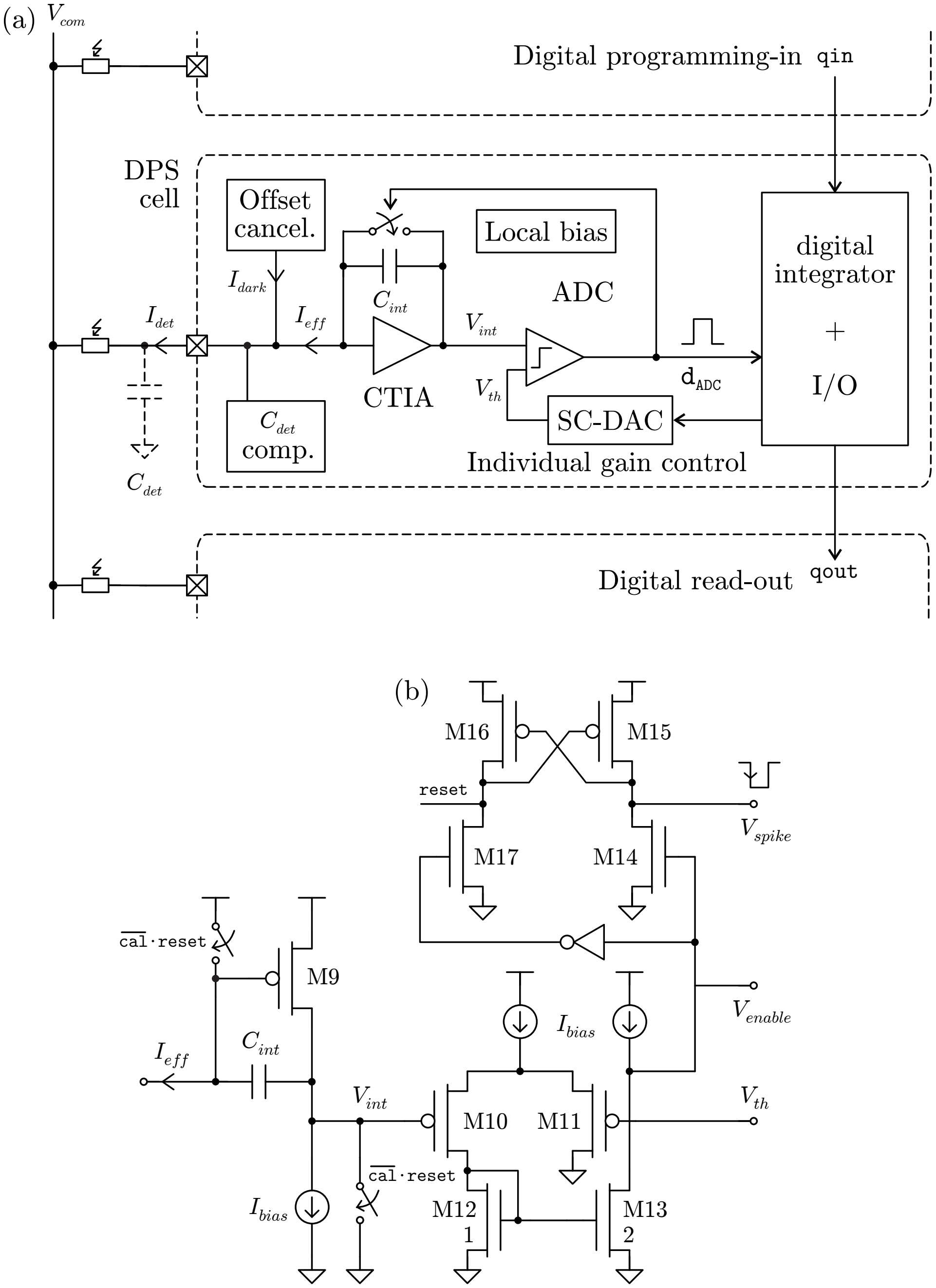

(a)
Vcom
Digital programming-in
qin
DPS cell
Offset cancel.
Local bias
Idark
Cint
ADC
digital integrator
+
I/O
Idet
Ieff
Vint
CTIA
Vth
dADC
SC-DAC
Cdet comp.
Individual gain control
Cdet
Digital read-out
qout
(b)
M16
M15
reset
Vspike
M17
M14
cal·reset
M9
Venable
Ibias
Ieff
Cint
Vint
M10
M11
Vth
cal·reset
M12
1
M13
2
Ibias

Figure 4.1 General architecture of the DPS-S100 cell (a) and detail of simplified CMOS PDM implementation (b).

Name	Type	Direction	Comments
`vdda`	P	-	Analog supply
`vddd`	P	-	Digital supply
`gnda`	P	-	Analog ground
`gndd`	P	-	Digital ground
`cal`	D	I	I_{dark} calibration enable
`clk`	D	I	Read-out clock (at falling edge)
`count`	D	I	Acquisition/$\overline{\text{communication}}$ selection. Analog integration reset
`edac`	D	I	V_{th} programming enable
`ninit`	D	I	Digital integration initialization (active low)
`qin`	D	I	Serial communications input
`qout`	D	O	Serial communications output

Table 4.2 I/O diagram of the initial DPS-S100 cell for frame-based Smart imagers ((P)ower, (D)igital, (I)nput, (O)utput) of Fig. 4.1.

communication. In the first case, `clk` remains silent, `count` is set to high, and the pixel integrates the effective input current value to a digital output code. When communicating, the opposite occurs: `clk` is activated, `count` driven to low, in-pixel acquisition is suspended and pixel digital I/O modules are reconfigured as shift registers to allow the serial read-out and program-in of the row binary data. `edac` is finally fixed to high enabling digital-to-analog conversion of the input gain codes during the last n communication cycles (with $n \leq N_{cnt}$). `ninit` is activated one clock cycle at the end of each communication phase. Calibration has to be repeated recurrently with a periodicity that depends on both, leakages and subthreshold conduction at the internal memory C_{dark} of the cancellation circuit, and temperature drifts.

4.1.1 Full-Custom ASIC Design

All DPS-S prototypes were integrated in 0.35μm 2P4M CMOS technology. In the concrete case of the DPS-S100, the design conformed to the design parameters of Table 4.3. The pixel layout is shown in Fig. 4.4.

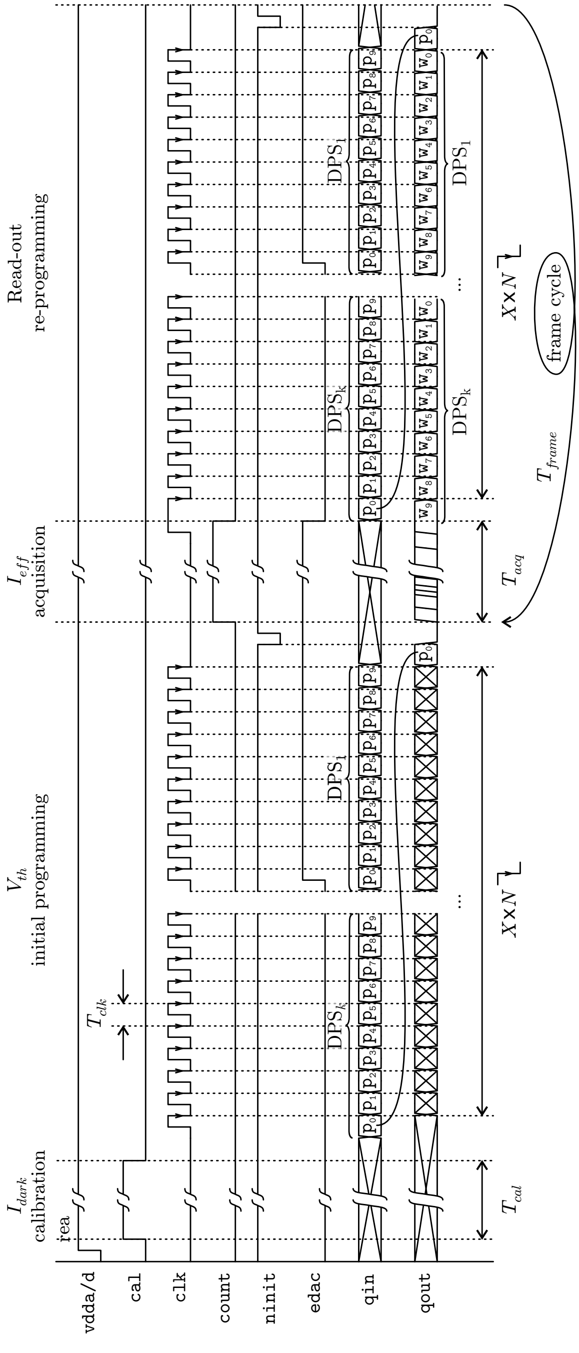

vdda/d
cal
clk
count
ninit
edac
qin
qout
rea
I_{dark} calibration
V_{th} initial programming
I_{eff} acquisition
Read-out re-programming
T_{clk}
T_{cal}
T_{acq}
$X{\times}N$
T_{frame}
frame cycle
DPS_k
DPS_1
p_0 p_1 p_2 p_3 p_4 p_5 p_6 p_7 p_8 p_9
w_9 w_8 w_7 w_6 w_5 w_4 w_3 w_2 w_1 w_0
...

Figure 4.2 | Operational chronogram of the DPS-S100 cell for the frame-based Smart imager of Fig. 4.1.

Variable	**Value**	**Units**
I_{bias}	60	nA
C_{int}	0.5	pF
$C_{mem,samp}$	0.1	pF
N_{cnt}	10	bit
PTAT multiplicity (P)	12	-

Table 4.3 Design parameters of the initial DPS-S100 cell for frame-based Smart imagers of Fig. 4.1.

The physical implementation of the DPS cells followed the layout recommendations of Fig. 4.3. All designs pursued to bound electrical variances in analog circuits to process and local technological mismatching [102]. Special emphasis was devoted to curtail the strong influence that threshold voltage mismatch has over the FPN of the imagers when MOSFETs are biased in subthreshold. As area availability was severely conditioned by pixel pitch, devices were sized according to the influence of their variances and noise on overall system performance. Transistor perimeter, substrate orientation, surrounding layers and assembly gradients were considered too. Signal routing also avoided switching-noise coupling, especially in high-impedance analog nodes. Such undesired effects were minimized through use of guard rings, generous inter-path distance between analog and digital blocks, and independent analog and digital power supply lines.

Because VPD PbSe post-processing was not yet mature at this time, this early implementation was oriented to hybridization. Hence, the last metal did not define the MWIR detector polarization contacts of Fig. 1.5(a) allowing its use as detector interfacing pad and as inter-pixel routing path. The entire design was integrated to obtain a minimum working pixel pitch so as to examine both area requirements and performance of the conceived FPA architecture. Final pixel dimensions were slightly smaller than $100\times100\mu$m.

All frame-based DPS-S generations were incorporated in preliminary test chips, where they were characterized as isolated cells and mini-FPA constituents. As VPD PbSe is not available at dice level, the input current equivalent to I_{det} in Fig. 4.1 was emulated by means of the integrated NMOS current sink shown in Fig. 4.5(a), whose drain was connected to the input pad of each corresponding pixel. Contacting the DPSs internally in the

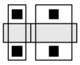
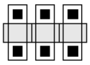
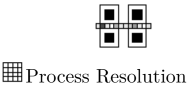
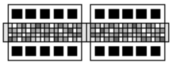
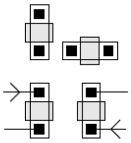
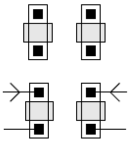
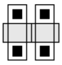
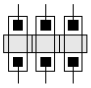
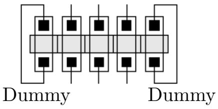
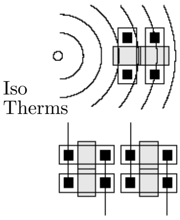
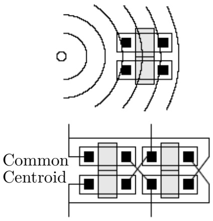
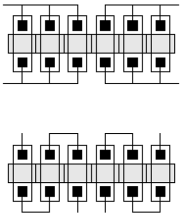
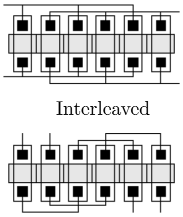
Layout Rule	Bad	Good
Unitary Elements		
Large Area	 Process Resolution	
Same Orientation		
Minimum Distance		
Same Sorround		 Dummy Dummy
Same Symmetry		 Common Centroid
$(W/L) \gg 1$ Examples $(W/L) \ll 1$		 Interleaved

Figure 4.3 General recommendations for CMOS device matching. Reprinted with permission from [95].

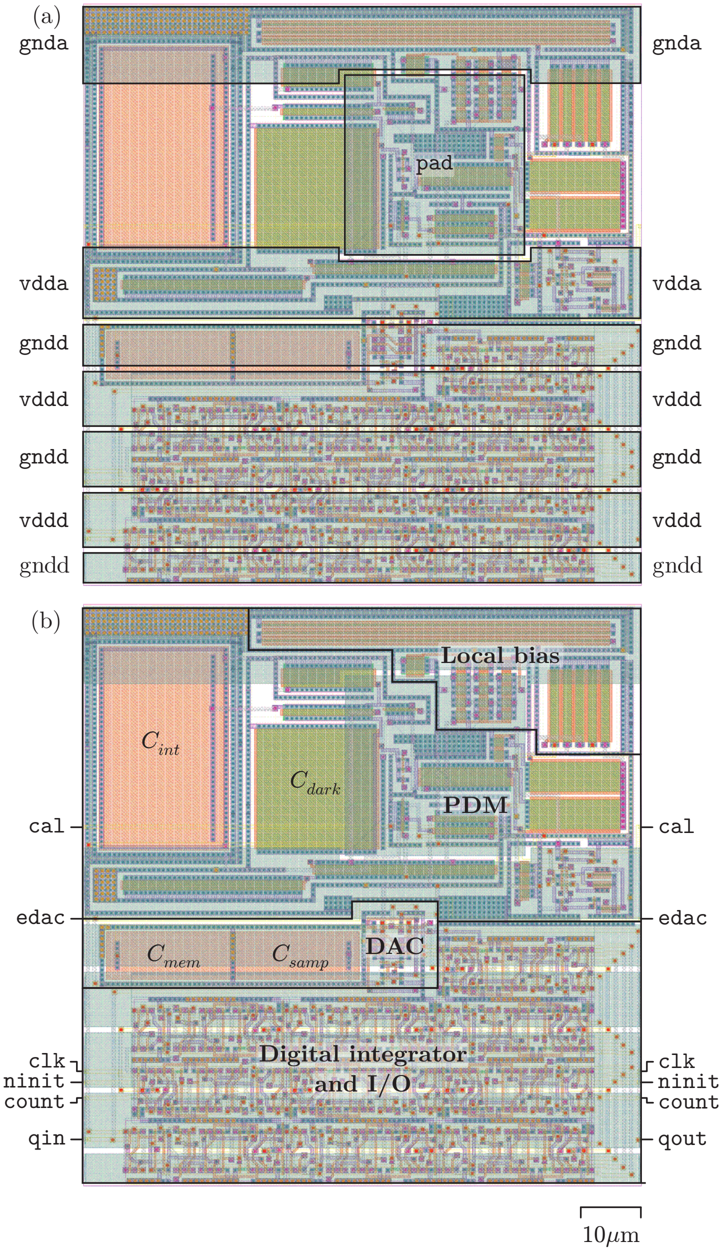

(a)
gnda
gnda
pad
vdda
vdda
gndd
gndd
vddd
vddd
gndd
gndd
vddd
vddd
gndd
gndd
(b)
Local bias
C_{int}
C_{dark}
PDM
cal
cal
edac
edac
C_{mem}
C_{samp}
DAC
Digital integrator and I/O
clk
ninit
count
clk
ninit
count
qin
qout
10μm

Figure 4.4 Physical CMOS layout of the DPS-S100 for frame-based Smart imagers. Metal-4 power-line routing (a); metal-3 routing of control signals and main block allocation (b).

IC allowed to avoid I/O-pad and wire-bonding parasitic capacitances. All transistor sources were biased to an external voltage $V_{com} = -100$mV. Such a low-voltage value makes both parasitic substrate currents and latch-up effects unnoticeable. Designed with long aspect ratios, emulation devices operated in strong inversion conduction. Fig. 4.6(a,b) shows the response of the selected $W = 10\mu$m and $L = 100\mu$m NMOS devices, with good linearity in the μA region and transconductance corner values of 1-2 nA/mV. The gate control (V_{ctrl}) of each NMOS device covers the expected photogenerated current range of the PbSe detector.

In order to minimize the total number of output pads, IR emulation control followed the distribution of Fig. 4.5(b), sharing two possible values: V_{ctrlA} and V_{ctrlB}. Copies of both I_{refA} and I_{refB} were accessible externally for evaluation purposes. Since I_{det} values are distributed alternatively, high-contrast, chess-board luminance patterns can be generated to evaluate inter-pixel crosstalk. The DPS-S100 test chip is shown in Fig 4.6(c).

4.1.2 Experimental Results

The different implementations of the DPS-S were characterized using the testbench of Fig. 4.7. The logic analyzer Tektronix TLA720 generated all control signals and reading out all pixel acquisition data following the communication protocol of Fig. 4.2. The Keithley 6487 picoammeter/voltage source controlled and sensed the emulated photocurrents, while the HP 8904A multifunction synthesizer fixed any other stable analog reference needed in the chip. All instrumentation but the logic analyzer were interconnected via the general purpose interface bus (GPIB) and automatically managed through a laptop computer powered by the LabView software.

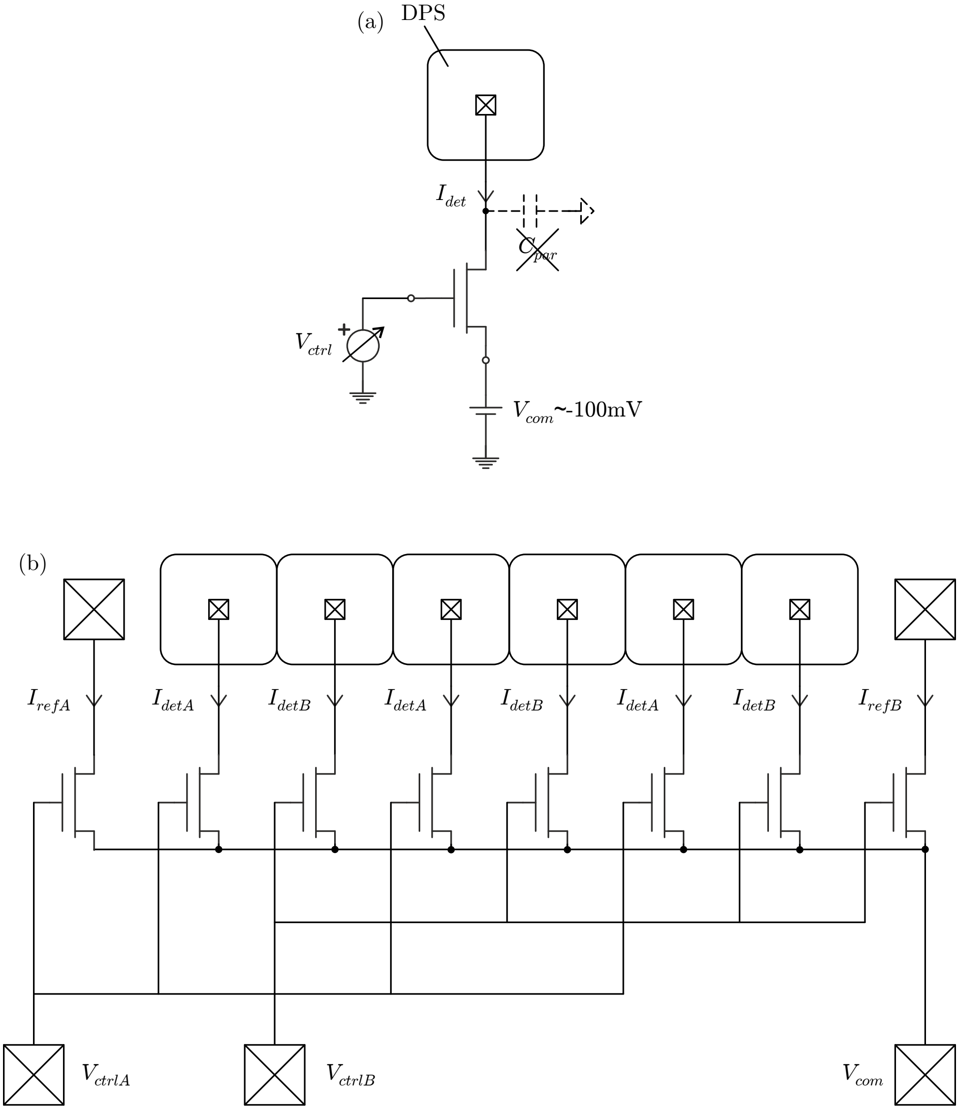

(a)
DPS
I_{det}
C_{par}
+
V_{ctrl}
V_{com}~-100mV
(b)
I_{refA}
I_{detA}
I_{detB}
I_{detA}
I_{detB}
I_{detA}
I_{detB}
I_{refB}
V_{ctrlA}
V_{ctrlB}
V_{com}

Figure 4.5 Basic scheme of the IR detector emulation circuit employed in the characterization of Smart DPS cells (a) and stimulus distribution in the mini-FPA (b).

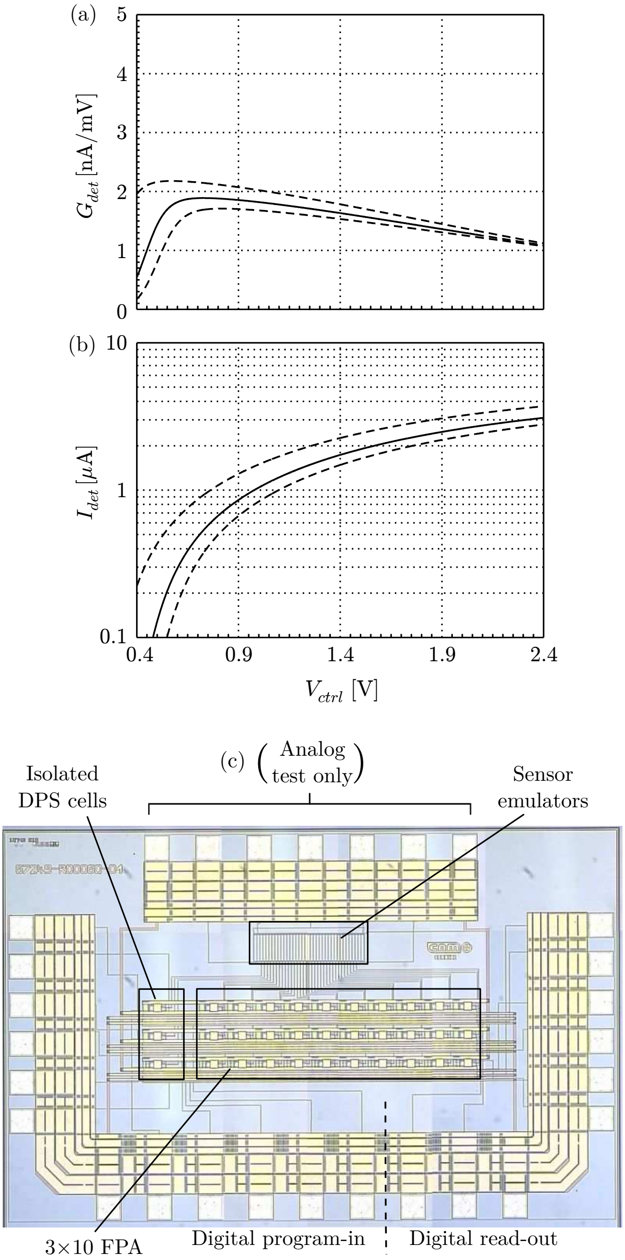


Figure 4.6 Experimental sensitivity (a) and absolute current levels (b) of the NMOS detector emulator included in test chips (dashed lines indicate process corners). Micrograph of the test chip fabricated to characterize DPS-S100 cells (c).

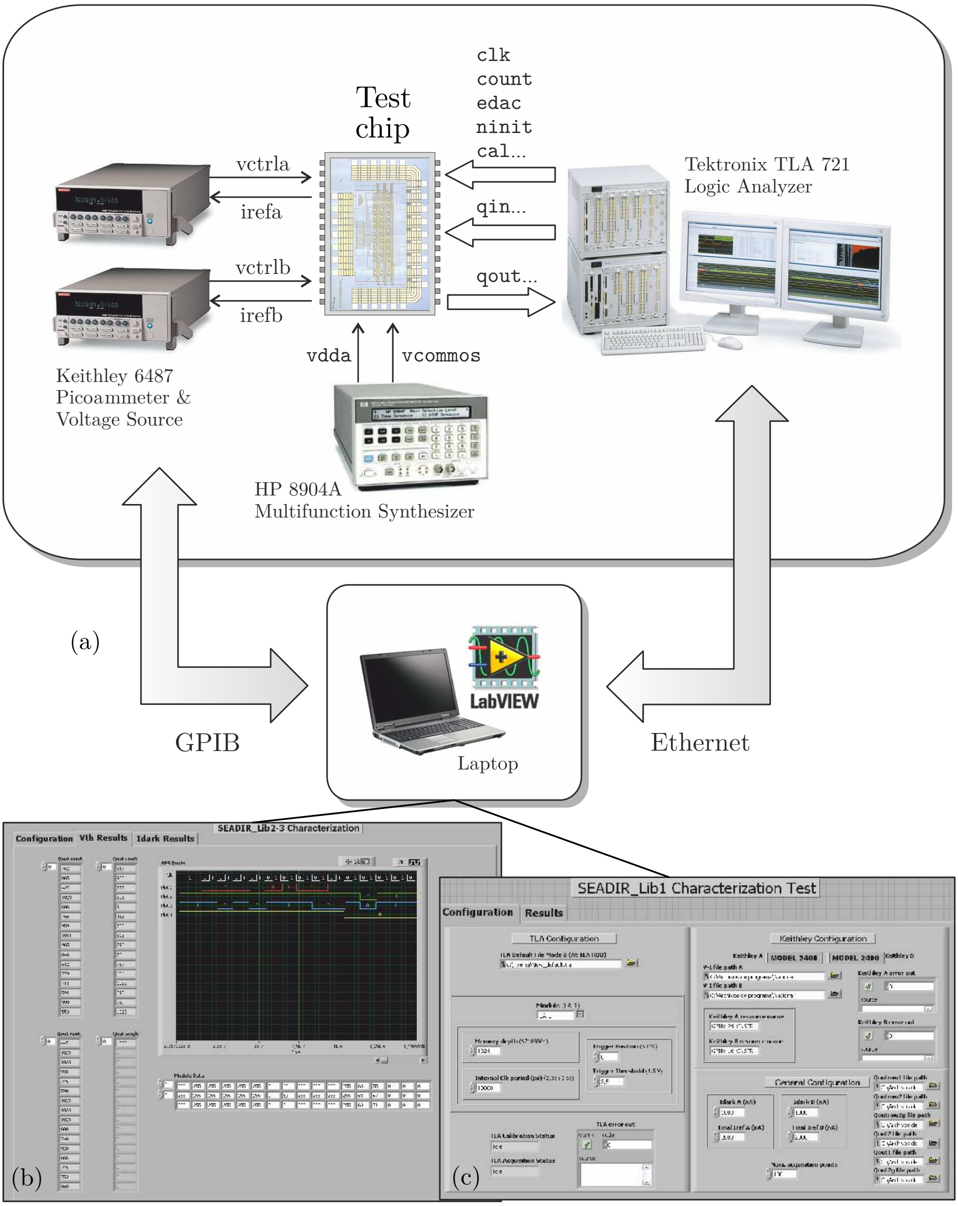

Test chip
clk
count
edac
ninit
cal...
qin...
qout...
vctrla
irefa
vctrlb
irefb
vdda
vcommos
Tektronix TLA 721
Logic Analyzer
Keithley 6487
Picoammeter &
Voltage Source
HP 8904A
Multifunction Synthesizer
(a)
GPIB
Ethernet
LabVIEW
Laptop
SEADIR_Lib2-3 Characterization
Configuration
Vth Results
Idark Results
(b)
SEADIR_Lib1 Characterization Test
Configuration
Results
TLA Configuration
Keithley Configuration
General Configuration
(c)

Figure 4.7 Simplified scheme of the electrical testbench deployed for the electrical characterization of DPS-S cells (a). Read-out captures (b) and Labview interface front panel (c).

Test chips were validated considering the following characteristics:

IR detector emulation: The first procedural step, previous to any other analyses. The I/V response of photocurrent emulation devices was characterized in order to control in-pixel IR equivalent excitation. As shown in Fig. 4.6(a,b), experimental results on tuning margin and control sensitivity were close to those obtained by electrical simulation. The acquired data was used as look-up table for the automatic adjustment of both I_{dark} and I_{eff} parameters during the test.

I_{eff}-`qout` transfer curve: The core basic test. It characterized the main function of internal DPS processing. Using the related IR detector emulators, an equivalent input current sweep was executed under fixed I_{dark} and V_{th} programmed levels. Considering V_{ctrl} as the superposition of an AC over a DC offset component, and fixing the alternate component during acquisition, it is possible to cyclically generate a large variety of I_{det} values in order to perform the measurements. Fig. 4.8(a) exemplifies a transfer curve data characterization, where the initial calibration cycle is followed by a succession of N_{acq} acquisition cycles, depending on the desired extracted curve resolution (normally $N_{acq} = 100$). The output code was read and post-processed using Matlab scripts.

Analog memory retention: This experiment was intended to evaluate the degradation of internal DPS analog memory, for a particular I_{dark} calibration value and a programmed V_{th} level. An indirect measure of this effect can be performed if digital read-out variations are acquired for a fixed I_{det} (i.e. programming of a constant value in the IR emulation device). Under this conditions:

$$\Delta\texttt{qout} \propto \begin{cases} -\Delta I_{dark} \equiv I_{eff} \\ -\Delta V_{th} \end{cases} \tag{4.1}$$

Taking into account that analog integration is only valid for positive I_{eff} values, it is necessary to set up a high enough initial I_{det} value so as to detect positive variations of I_{dark}. Based on this idea, the test procedure started with an initial calibration phase under $I_{det} = I_{dark}$, and continued by the successive standard acquisition cycles of Fig. 4.8(b) with a known $I_{det} = I_{dark} + I_{eff}$.

Individual programmability: This test stage was devoted to digital, individual offset and/or gain programming. In this sense, the transfer curve characterization sweep was repeated for every desired code. Larger V_{th}s led to higher transfer function slopes, whereas the larger the programmed I_{dark} code, the less the dark current flowing through the cancellation circuit, and the higher the I_{det} to activate PDM.

Crosstalk: The remaining analysis aimed to measure coupling effects between adjacent pixels by fixing one V_{ctrl} to full-scale, while the remaining DPSs received null excitation. The latter was monitored to detect any induced event, either due to spatial proximity or temporal immediacy of perturbing signals.

Experimental results are summarized in Table 4.4; electrical performance is detailed in Table 4.5. The test proved the architectural feasibility of the DPS-S100 and the correct operation of the adopted IR emulation scheme, but detected some weak points susceptible to be improved. I_{dark} autocalibration behaved with an approximate retention time of 1s (Fig. 4.9(a)), mostly limited by the discharge of M6 gate capacitance (i.e. C_{dark}) through subthreshold conduction and parasitic PN-junction leakages due to coupling along successive CTIA resets, as shown in Fig. 4.9(b).

Although gain programming was effective, DPS cells showed the transfer curve compression of Fig. 4.10. Electrical simulations pointed to parasitic coupling from the comparator to the V_{th} analog memory, which resulted in a progressive increase of this variable during acquisition, and the subsequent reduction of the density of pulses counted by the digital integrator. The regenerative comparator of Fig. 4.1(b), suffered also of unexpected metastates that reduced spike width below the minimum duration noticeable by the counter. Crosstalk was inappreciable.

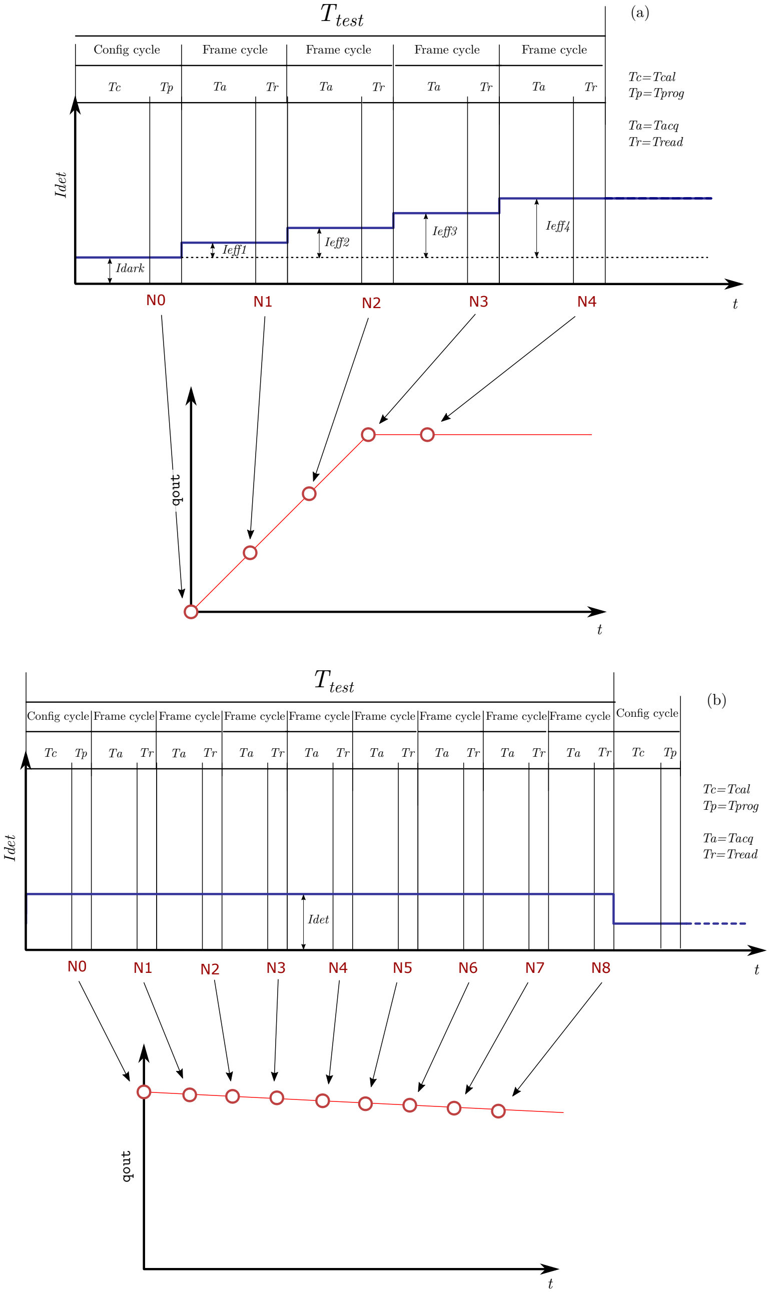

T_{test}
(a)
Config cycle
Frame cycle
Frame cycle
Frame cycle
Frame cycle
Tc Tp Ta Tr Ta Tr Ta Tr Ta Tr
Tc=Tcal
Tp=Tprog
Ta=Tacq
Tr=Tread
Idet
Ieff4
Ieff3
Ieff2
Ieff1
Idark
N0
N1
N2
N3
N4
t
qout
t
T_{test}
(b)
Config cycle
Frame cycle
Frame cycle
Frame cycle
Frame cycle
Frame cycle
Frame cycle
Frame cycle
Frame cycle
Config cycle
Tc Tp Ta Tr Ta Tr Ta Tr Ta Tr Ta Tr Ta Tr Ta Tr Ta Tr Tc Tp
Tc=Tcal
Tp=Tprog
Ta=Tacq
Tr=Tread
Idet
Idet
N0
N1
N2
N3
N4
N5
N6
N7
N8
t
qout
t

Figure 4.8 | Transfer memory (a) and I_{dark} memory retention (b) characterization protocols for DPS-S cells.

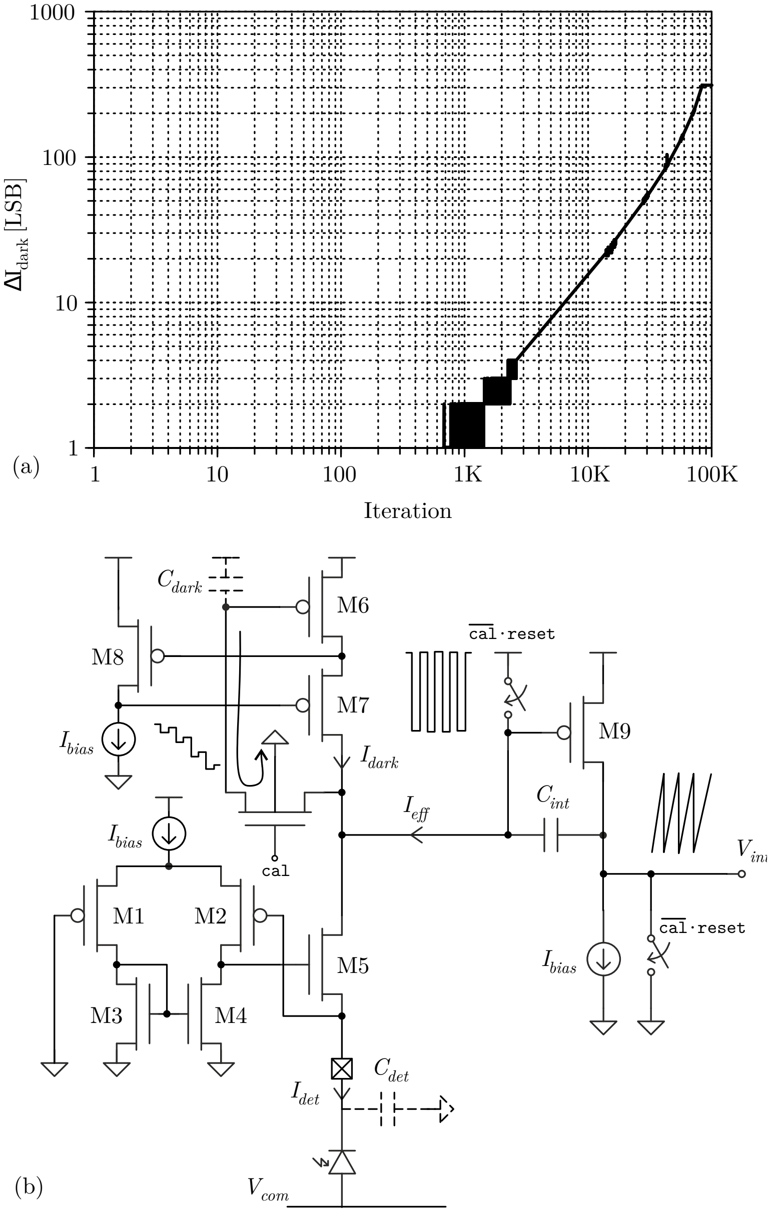


Figure 4.9 Experimental measurements of I_{dark} memory retention in DPS-S100 cells of Fig. 4.6(c) (a), and illustration of possible sources (b), for $I_{dark} = 1\mu$A and $I_{eff} = 0.5\mu$A.

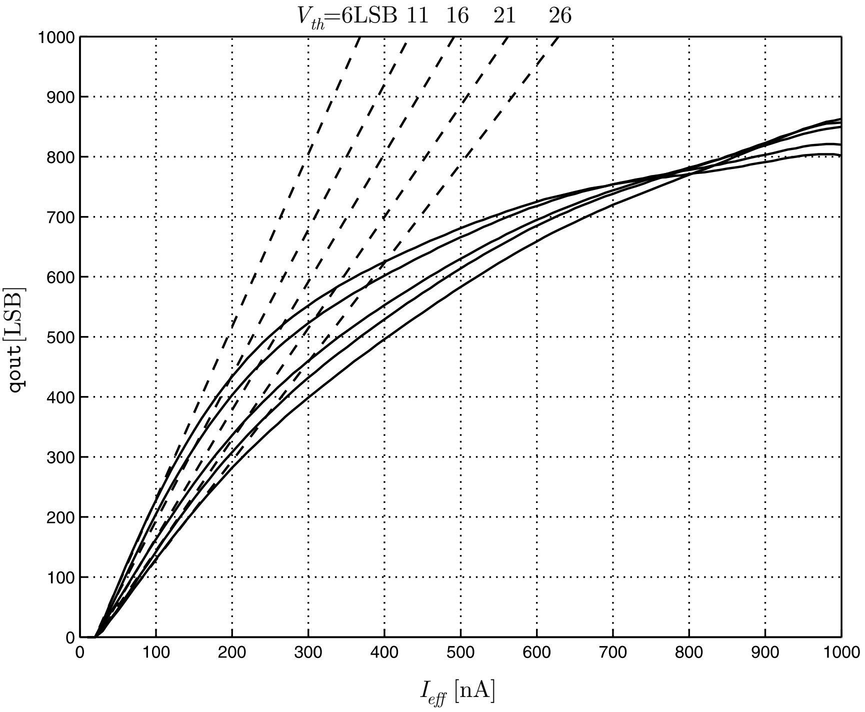


Figure 4.10 Examples of experimental transfer functions for different gain control values over a DPS-S100 cell of Fig. 4.6(c), for $I_{dark} = 1\mu$A.

DPS functionality	Comments
Self-biasing generation	✓ Correct.
Input capacitance comp.	✓ Correct.
Offset cancellation	✓ Appropriate resolution (∼nA). ✗ Low retention time (∼1s/LSB): Frequent calibration is needed.
Pulse generation	✓ Threshold comparison is correct. ✗ Coupling to the DAC: Larger DAC capacitances, minimum comparator dimensions should be employed. ✗ Slow transitions, event loosing: Spike generation circuit must be redefined.
Digital integration	✓ Correct.
Individual gain prog.	✓ Correct.
Digital comm. interface	✓ Correct.

Table 4.4 Summary of experimental results for the DPS-S100 cells of Fig. 4.6(c).

Variable	Value	Units
Dark current range	0.1-5	μA
Dark current retention time	2-10	s
Max. input capacitance	15	pF
Signal range	1-1000	nA
Integration time	1	ms
Crosstalk	< 0.5	LSB
Programming/read-out speed	10	Mbps
Supply voltage	3.3	V
Static power consumption	< 1	μW
Biasing deviations ($\pm\sigma$)	±15	%
Total Silicon area	100×100	μm^2

Table 4.5 Measured performance of the initial DPS-S100 for frame-based Smart imagers

4.2 A 200μm and 130μm-pitch Smart Pixel with Full Programmability

The new DPS generations overcame the operational issues of the DPS-S100 by introducing the following architectural changes:

- **Integration of online dark-current programming capabilities** via the CMOS topology of Fig. 2.12(a) in order to reduce the required analog memory retention time to 2 frames (typically $<$ 2ms) and provide external control over this value at no frame-rate costs.
- **Inclusion of the triple-switch reset scheme of Fig. 2.15** to correct the excessively slow initialization of C_{int} in the DPS-S100 cell while adding a compact CDS mechanism to lower low-frequency noise.
- **Redesign of the regenerative comparator to Fig. 2.16** so as to increase common-mode margin for V_{th} programming, improve slew rate and introduce enough hysteresis to ensure event counting.

These improvements were introduced in the 200μm-pitch frame-based Smart digital pixel sensor (DPS-S200) as shown in Fig. 4.11(a), the first intended for monolithic integration by PbSe deposition on top of the ROIC. This pixel was refined to the architecture of Fig. 4.11(b) for commercial 130μm-pitch frame-based Smart digital pixel sensor (DPS-S130) designs. Whereas in the former I_{dark} is configured by use of an additional SC-DAC, the latter compacts physical implementation by multiplexing the use of a single SC-DAC block along consecutive frame cycles. Table 4.6 lists all the I/O signals of the two devices.

Every pixel in both design libraries works in agreement with the chronogram of Fig. 4.12. In base of this protocol, the recommended procedure of Fig. 4.13 operates the DPS and, by extension, the imager following two main phases: an initial I_{dark} tuning, which performs a dichotomic search of the offset compensation value for a given mid-scale V_{th}; and the basic dual-frame routine, that alternatively programs the two variables for every standard acquisition cycle of Fig. 4.12. The `cal` control signal is now

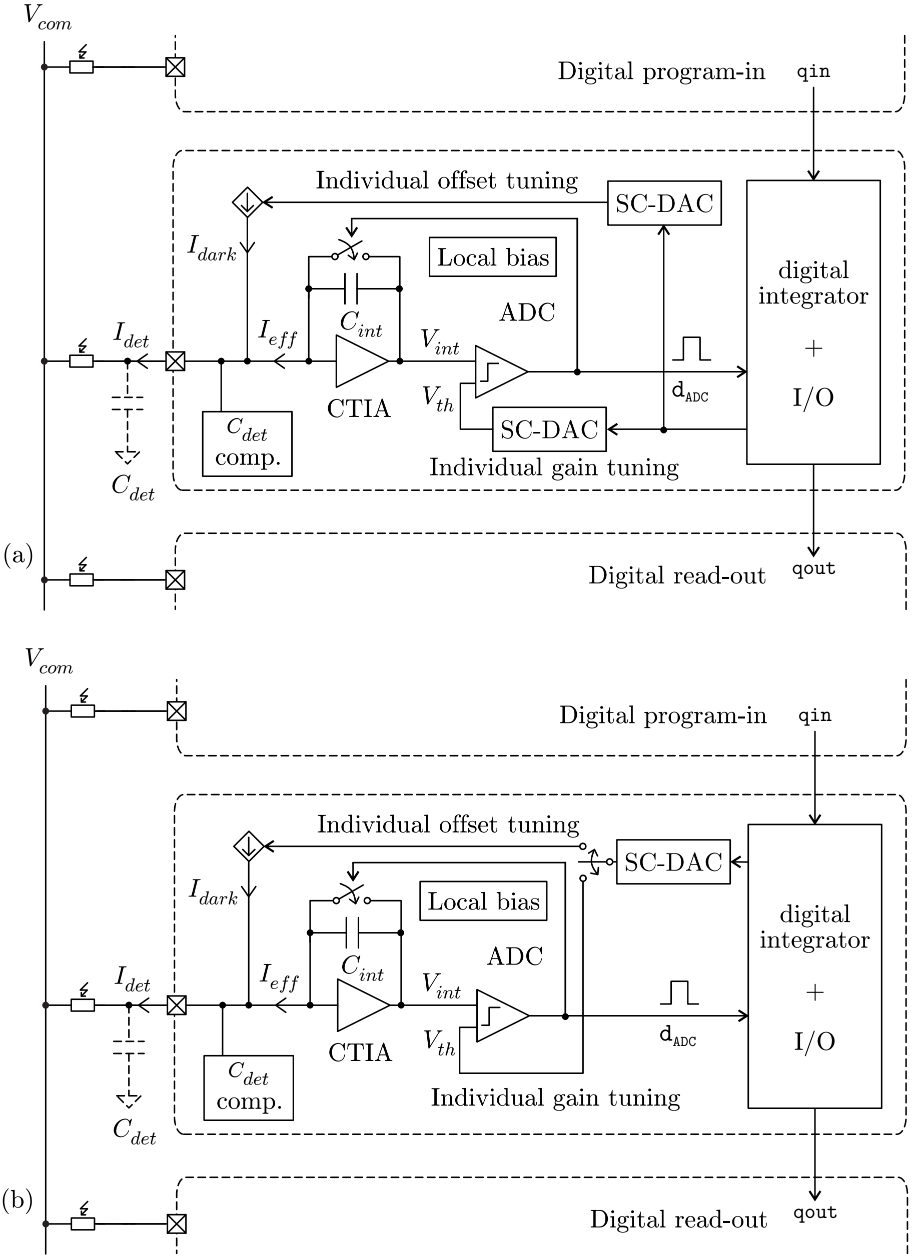

V_{com}
Digital program-in
qin
Individual offset tuning
SC-DAC
I_{dark}
Local bias
digital integrator + I/O
ADC
C_{int}
I_{det}
I_{eff}
V_{int}
CTIA
V_{th}
d_{ADC}
C_{det} comp.
C_{det}
Individual gain tuning
(a)
Digital read-out
qout
V_{com}
Digital program-in
qin
Individual offset tuning
SC-DAC
I_{dark}
Local bias
digital integrator + I/O
ADC
C_{int}
I_{det}
I_{eff}
V_{int}
CTIA
V_{th}
d_{ADC}
C_{det} comp.
C_{det}
Individual gain tuning
(b)
Digital read-out
qout

Figure 4.11 | General architecture of the DPS-S200 (a) and the DPS-S130 (b).

Name	Type	Direction	Comments
`vdda`	P	-	Analog supply
`vddd`	P	-	Digital supply
`gnda`	P	-	Analog ground
`gndd`	P	-	Digital ground
`cal`	D	I	$I_{dark}/\overline{V_{th}}$ tuning selection
`clk`	D	I	Read-out clock (at falling edge)
`count`	D	I	Acquisition/$\overline{\text{communication}}$ selection. Analog integration reset
`edac`	D	I	V_{th} programming enable
`ninit`	D	I	Digital integration initialization (active low)
`qin`	D	I	Serial communications input
`qout`	D	O	Serial communications output

Table 4.6 I/O diagram of DPS-S200 and DPS-S130 cells for frame-based Smart imagers (P)ower, (D)igital, (I)nput, (O)utput).

used to select between offset and gain programming. The preliminary tuning only requires N_{cnt} iterations, where N_{cnt} stands, as previous chapters, for the number of I_{dark} programming bits available in the digital I/O module. Posterior offset adjustments to its temporal variations are not expected to extend beyond the least significative bits, thus reducing the number of iterations needed in next uses of the algorithm.

4.2.1 Full-Custom ASIC Designs

In the DPS-S200 of Fig. 4.14, the top metal layer of the CMOS technology is entirely devoted to define the two terminals of the PbSe detector introduced in Fig. 1.5(a): the grille common bias voltage V_{com} and the terminal collecting the individual detector current I_{det}. The bonding aperture has a width of 20μm, and the resulting metal shape is slightly wider as pointed in the design rules. In this case, pixel pitch was limited to 200μm by the loss of the fourth metal level for layout design and by the lithography of the sensor post-processing itself. The larger pixel pitch was used to include a dual SC-DAC following Fig. 4.14(c) and to enhance the reliability of these blocks by triplicating C_{mem} and C_{samp} capacitance values, while improving

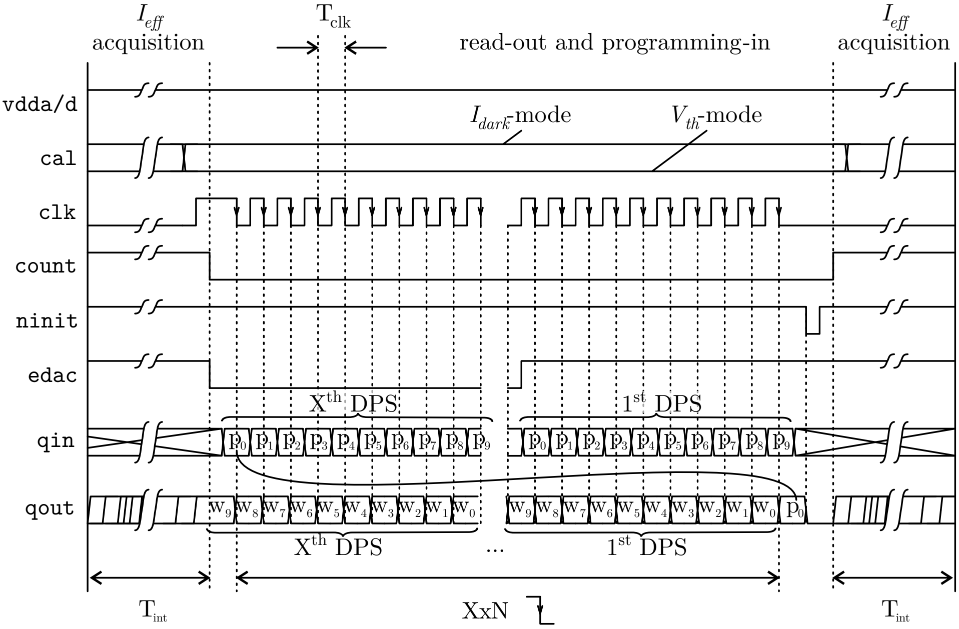

I_eff acquisition
T_clk
read-out and programming-in
I_eff acquisition
vdda/d
cal
clk
count
ninit
edac
qin
qout
I_dark-mode
V_th-mode
X^th DPS
1^st DPS
p0 p1 p2 p3 p4 p5 p6 p7 p8 p9
w9 w8 w7 w6 w5 w4 w3 w2 w1 w0
p0
X^th DPS
...
1^st DPS
T_int
XxN
T_int

Figure 4.12 Operational chronogram of DPS-S200 and DPS-S130 cells for frame-based Smart imagers.

matching between them by use of common-centroid techniques and dummy capacitances. The layout was also upgraded to provide better isolation between analog and digital circuits and reduce biasing noise coupling by the inclusion of additional current mirror stages.

The DPS-S130 of Fig. 4.15 was scaled down to about 40% of the previous DPS cell by taking advantage of the top CMOS metal which, apart from the 20μm pad structure, was entirely devoted to circuit design. In this last version of the DPS, contacting metals were defined a posteriori by post-processing CMOS circuits as explained later in Sec. 5.2.1. Offset and gain tuning were implemented through a single SC-DAC, by multiplexing I_{dark} and V_{th} programming between frames, as it can be easily seen in the reduction of the number of poly-Si capacitors in this same figure compared to Fig. 4.14. The layout of the multiplexed SC-DAC was also simplified, and I_{dark} programming range extended to the limits specified in Table 4.8. Both DPS-S200 and DPS-S130 pixels share the same design parameters of

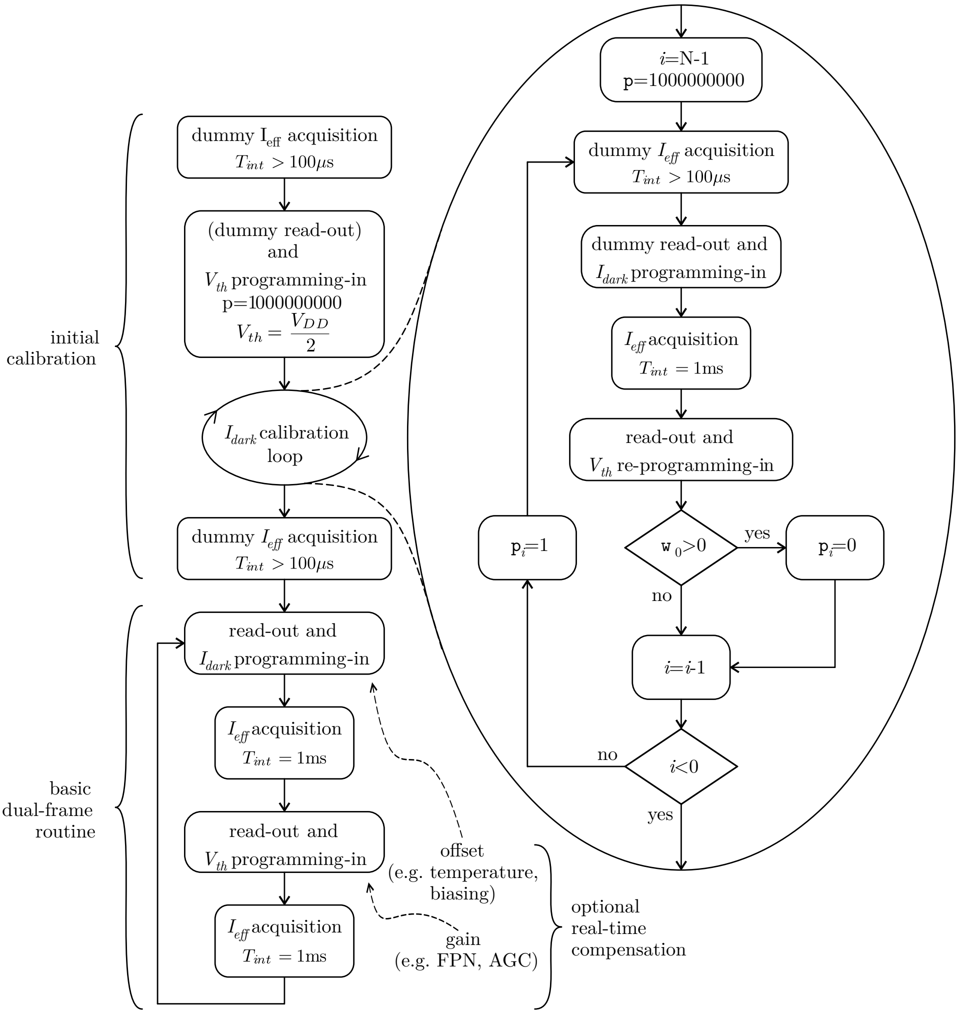

initial calibration
dummy I_{eff} acquisition $T_{int} > 100\mu$s
(dummy read-out) and V_{th} programming-in p=1000000000 $V_{th} = \frac{V_{DD}}{2}$
I_{dark} calibration loop
dummy I_{eff} acquisition $T_{int} > 100\mu$s
basic dual-frame routine
read-out and I_{dark} programming-in
I_{eff} acquisition $T_{int} = 1$ms
read-out and V_{th} programming-in
I_{eff} acquisition $T_{int} = 1$ms
offset (e.g. temperature, biasing)
gain (e.g. FPN, AGC)
optional real-time compensation
i=N-1 p=1000000000
dummy I_{eff} acquisition $T_{int} > 100\mu$s
dummy read-out and I_{dark} programming-in
I_{eff} acquisition $T_{int} = 1$ms
read-out and V_{th} re-programming-in
p$_i$=1
w$_0$>0
yes
p$_i$=0
no
i=i-1
no
i<0
yes

Figure 4.13 Standard operating routine of DPS-S200 and DPS-S130 cells for frame-based Smart imagers.

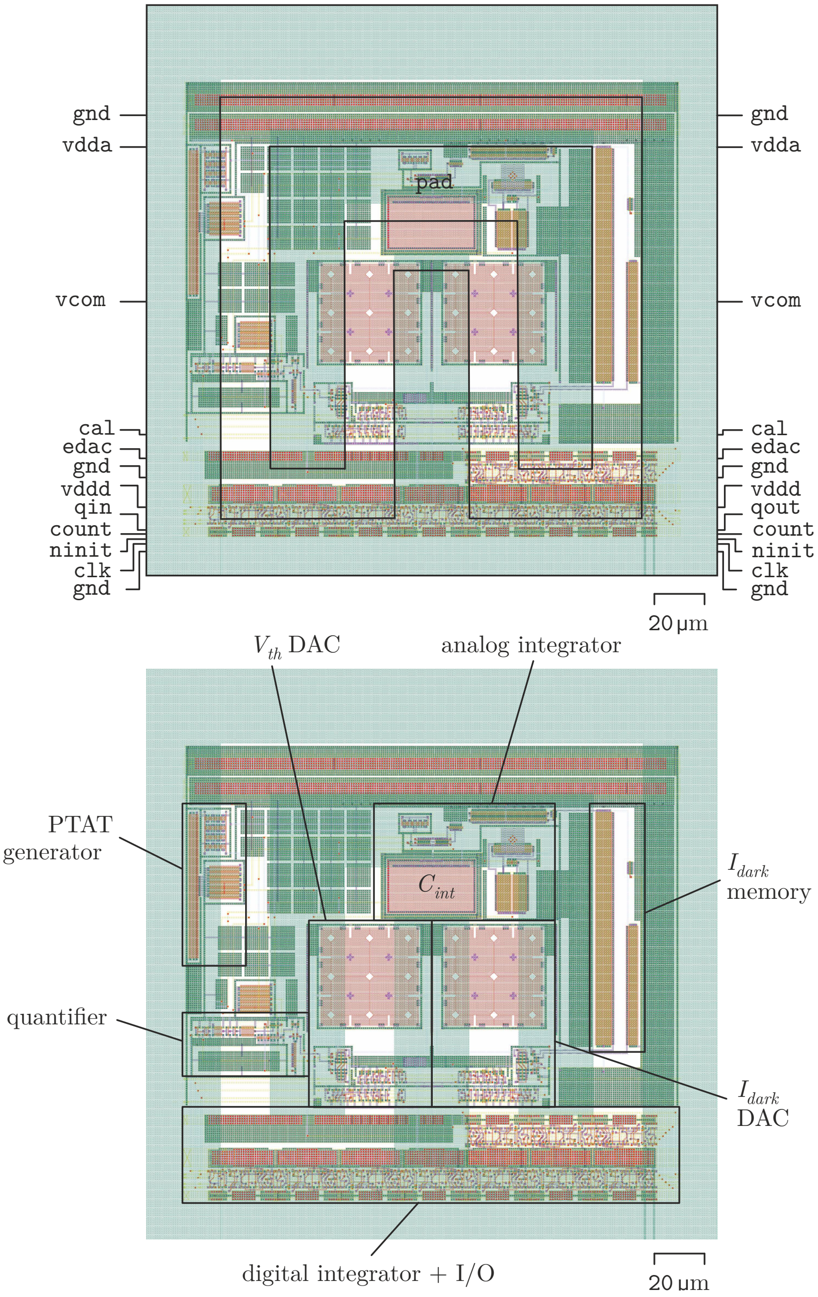

gnd
vdda
vcom
cal
edac
gnd
vddd
qin
count
ninit
clk
gnd
gnd
vdda
vcom
cal
edac
gnd
vddd
qout
count
ninit
clk
gnd
pad
20 µm
V_{th} DAC
analog integrator
PTAT generator
C_{int}
I_{dark} memory
quantifier
I_{dark} DAC
digital integrator + I/O
20 µm

Figure 4.14 Physical CMOS layout of the DPS-S200 cell for frame-based Smart imagers. External interconnections (a) and main block allocation (b).

Table 4.7.

Variable	**Value**	**Units**
I_{bias}	60	nA
C_{int}	0.5	pF
$C_{mem,samp}$	0.3	pF
N_{cnt}	10	bit
PTAT multiplicity (P)	12	-

Table 4.7 Design parameters of both the DPS-S200 and the DPS-S130 pixels for frame-based Smart imagers of Fig. 4.15 and Fig. 4.14.

Electrical tests without IR sensors were performed to the two DPS-S cells through the specific experiments of Fig. 4.16(a) and Fig. 4.16(b). These integrated circuits included an isolated active pixel for the detailed characterization of the DPS cells, as well as a tiny FPA of 3×16 pixels and 3×5 pixels (with I/O serial access by row), respectively, for crosstalk studies together with the corresponding NMOS sensor emulators.

4.2.2 Experimental Results

The test chips were characterized using the experimental setup and procedures defined in Sec. 4.1.2. Electrical results are reported in Fig. 4.17 to 4.19 and are summarized in Table 4.8. The DPS transfer curve was measured under different digital programming codes in order to study pixel tuning capabilities. The family of curves presented in Fig. 4.17(a,b) exhibits a dark current tuning range of two octaves, from 0.5μA to 2μA, and effective threshold swing. Fig. 4.17(c,d) demonstrates the improved transfer-curve programmability of the DPS-S130, enlarging the dark current range in more than one decade with respect to the previous results of Fig. 4.17(a). This feature plays an important role when covering the deviations of large FPAs of PbSe MWIR detectors. Gain tuning range is almost preserved by design.

Analog memory leakage for offset (I_{dark}) and gain (V_{th}) programming is quantified in terms of digital output error. In this case, the test protocol consists of an initial tuning of I_{dark} (or V_{th}), and the refreshment at each consecutive frame of V_{th} (or I_{dark}) only, instead of the alternate

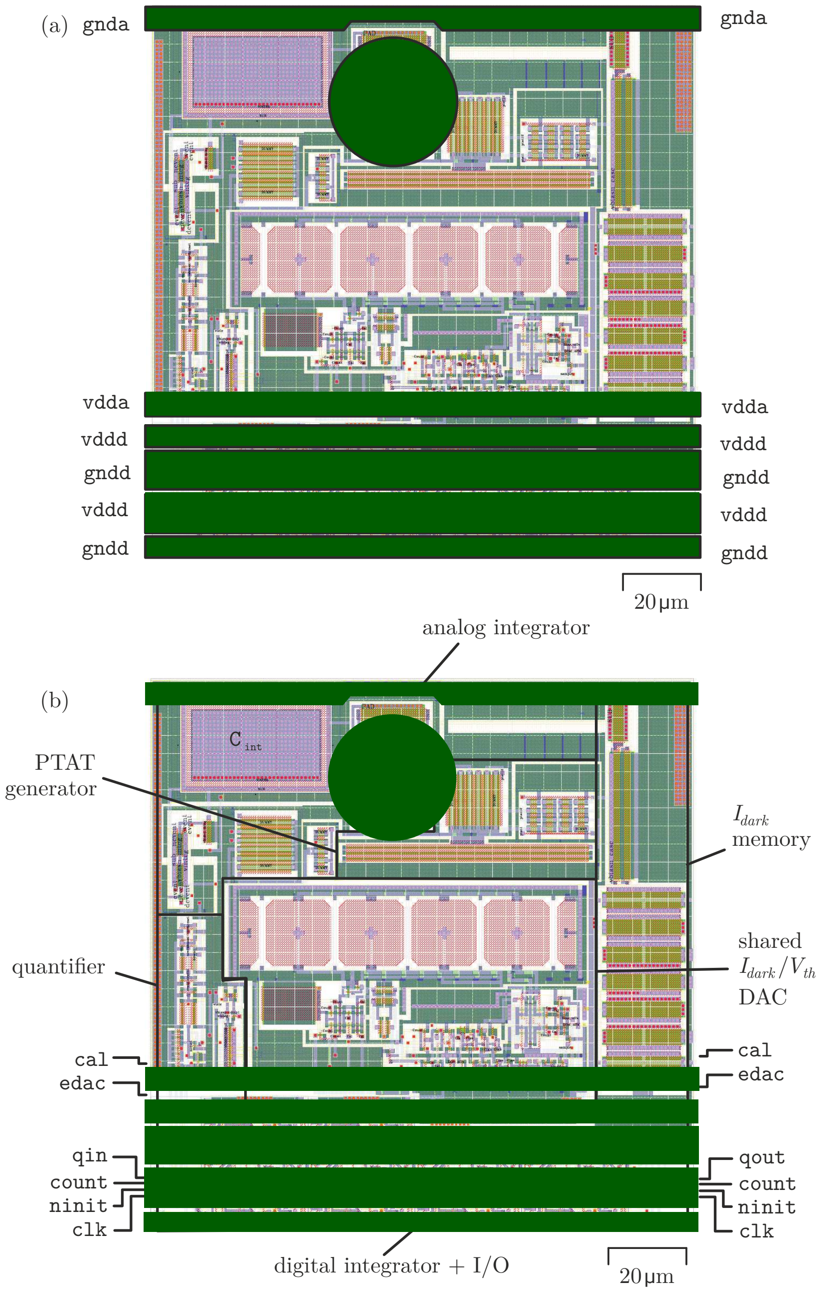

(a)
gnda
gnda
vdda
vdda
vddd
vddd
gndd
gndd
vddd
vddd
gndd
gndd
20 µm
analog integrator
(b)
C int
PTAT generator
I_{dark} memory
quantifier
shared I_{dark}/V_{th} DAC
cal
edac
cal
edac
qin
count
ninit
clk
qout
count
ninit
clk
digital integrator + I/O
20 µm

Figure 4.15 Physical CMOS layout of the DPS-S130 cell for frame-based Smart imagers. Metal-4 power-line routing (a); metal-3 routing of control signals and main block allocation (b).

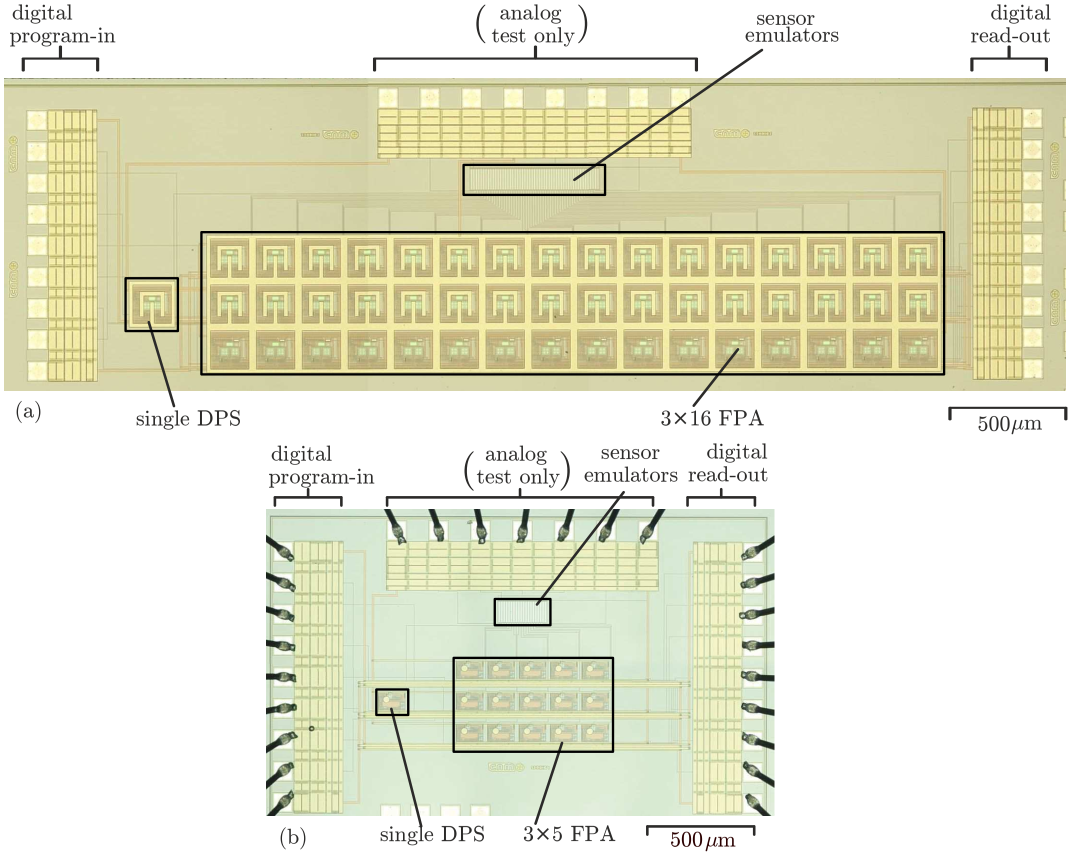

digital
program-in
analog
test only
sensor
emulators
digital
read-out
(a)
single DPS
3×16 FPA
500μm
digital
program-in
analog
test only
sensor
emulators
digital
read-out
(b)
single DPS
3×5 FPA
500μm

Figure 4.16 | Micrograph of the test chip fabricated to characterize DPS-S200 (a) and DPS-S130 (b) cells.

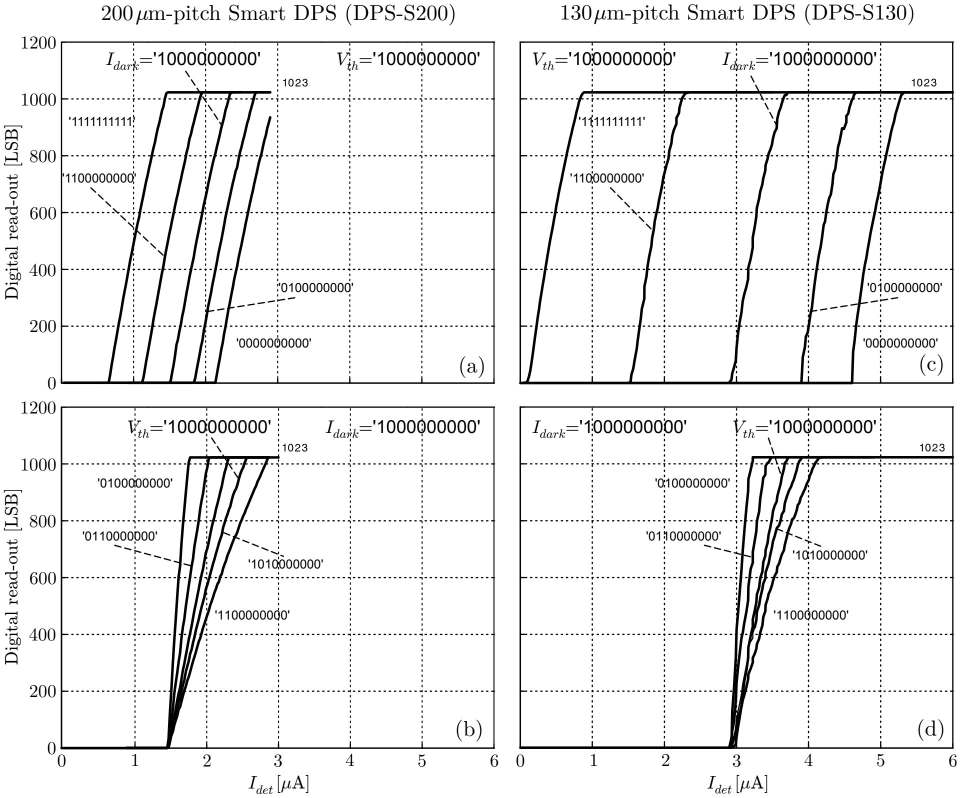


Figure 4.17 Experimental transfer curve of the DPS-S200 (a,b) and the DPS-S130 cells (c,d) for different individual offset (top) and gain (bottom) digital tuning codes, respectively.

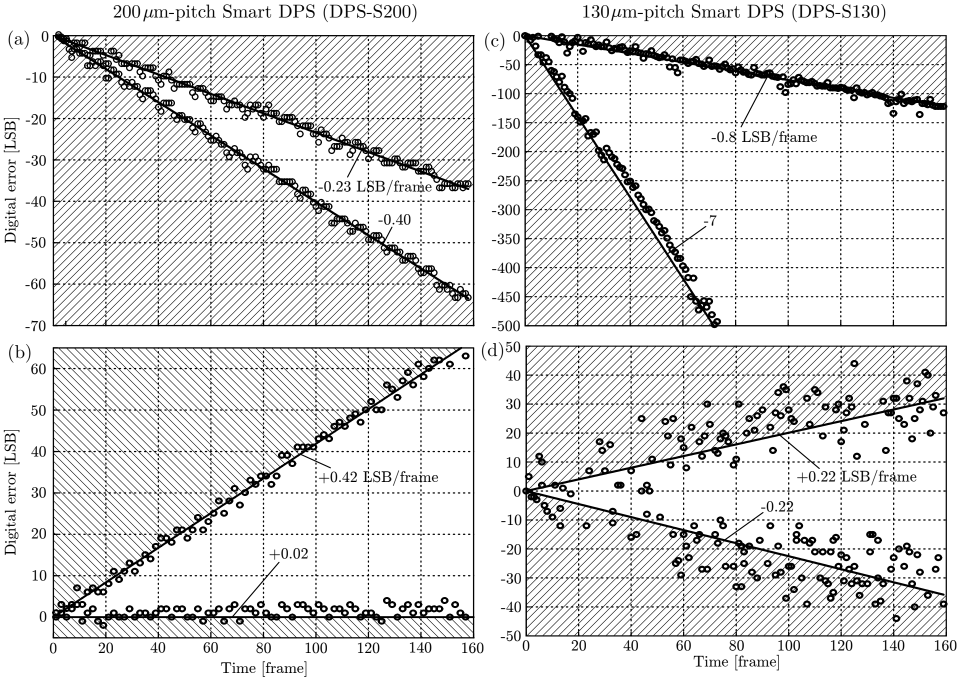


Figure 4.18 Experimental range of I_{dark} (a,c) and V_{th} memory leakage rates (b,d) inside the DPS-S200 and the DPS-S130 cells, respectively, in terms of digital output error when only the other parameter is refreshed.

method. The resulting error rates of Fig. 4.18 validate the frame programming scheme of Fig. 4.12. Contrasting the results of Fig. 4.18(a,b) with those of Fig. 4.18(c,d) evinces the slightly negative impact that the shared DAC of DPS-S130s had over analog memory storage of the offset, but also an increased retention of the gain parameter. The retention time in both cases is higher than the acquisition period targeted for high-speed MWIR imaging.

Fig. 4.19(a,b) shows statistical deviations caused by circuit technology mismatching between 480 DPS-S200 cells (10 die samples) programmed with identical digital codes. The same analysis over 105 DPS-S130 pixels (7 die samples) returned the results of Fig. 4.19(c,d). The improvement over the first distributions may be caused by both, a more optimized layout matching technique and larger dark current levels, which tend to minimize the effect of threshold voltage variances. Input offset scattering is probably caused by threshold voltage (ΔV_{TOP}) and current factor ($\Delta\beta_P$) variations in the PMOS devices employed for I_{dark} generation. Applying Pelgrom's law [118] to technological mismatching:

$$\sigma(\Delta V_{TOP}) = \frac{A_{V_{TOP}}}{\sqrt{WL}} \equiv \frac{14.5\text{mV}\mu\text{m}}{\sqrt{717\mu\text{m}^2}} \simeq 0.54\text{mV} \tag{4.2}$$

$$\sigma\left(\frac{\Delta\beta_P}{\beta_P}\right) = \frac{A_{\beta_P}/\beta_P}{\sqrt{WL}} \equiv \frac{1.0\%\mu\text{m}}{\sqrt{717\mu\text{m}^2}} \simeq 0.04\% \tag{4.3}$$

Depending on saturation region,

$$\text{Strong inversion}: \quad \sigma\left(\frac{\Delta\beta_P}{\beta_P}\right) < \sigma\left(\frac{\Delta I_{off}}{I_{off}}\right) < \frac{\sigma(\Delta V_{TOP})}{nU_t} \quad : \text{subthreshold} \tag{4.4}$$

Hence, it is expected that

$$0.04\% < \sigma\left(\frac{\Delta I_{off}}{I_{off}}\right) < 1.66\% \tag{4.5}$$

Unfortunately, this estimation is only valid for adjacent device pairs and too optimistic for a pitch higher than 100μm.

Gain differences may be produced by local mismatching in the differential pair of the NMOS (ΔV_{TON}) comparator depicted in Fig. 2.16 and, in lesser extent, by divergences between pixel integration capacitances. By the mismatch model used above,

$$\sigma(\Delta V_{TON}) = \frac{A_{V_{TON}}}{\sqrt{WL}} \equiv \frac{9.5\text{mV}\mu\text{m}}{\sqrt{0.14\mu\text{m}^2}} \simeq 25.4\text{mV} \tag{4.6}$$

$$\sigma\left(\frac{\Delta C_{int}}{C_{int}}\right) = \frac{A_C/C}{\sqrt{WL}} \equiv \frac{0.45\%\mu\text{m}}{\sqrt{576\mu\text{m}^2}} \simeq 0.02\% \tag{4.7}$$

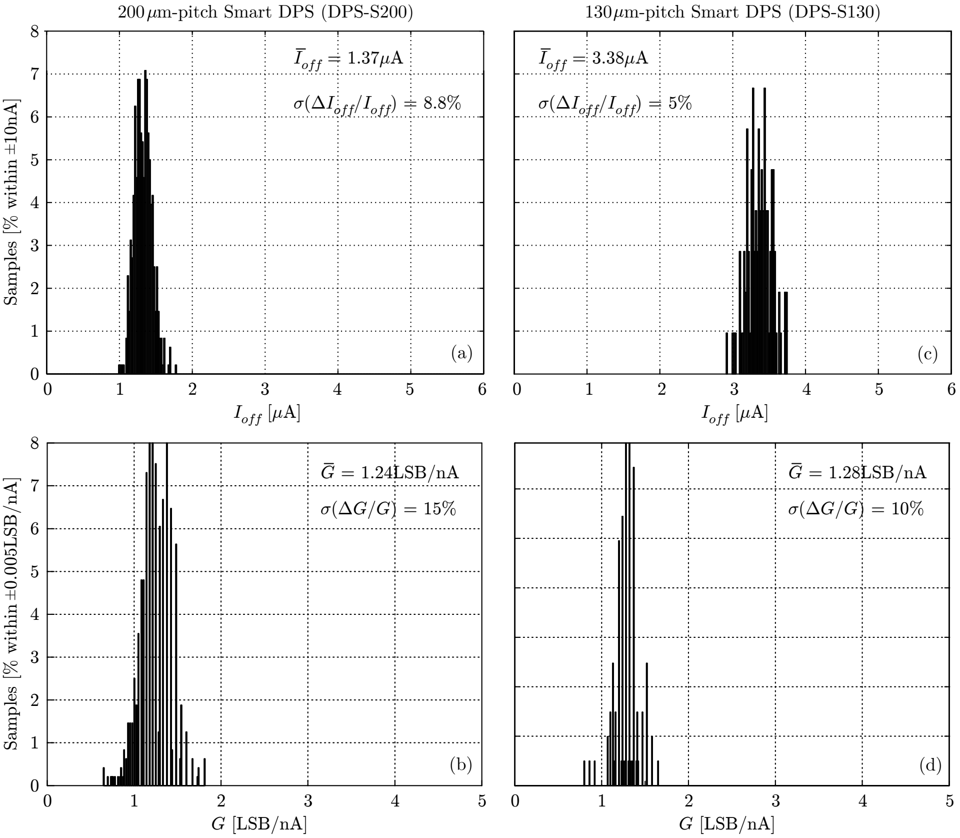


Figure 4.19 Experimental offset (a,c) and gain (b,d) deviations between 480 DPS-S200 and 105 DPS-S130 cells for the digital tuning codes I_{dark} = `‘1000000000’` and V_{th} = `‘1000000000’`.

and

$$\begin{aligned}\sigma\left(\frac{\Delta G}{G}\right) &= \sqrt{\sigma^2\left(\frac{\Delta V_{TON}}{V_{th}}\right)+\sigma^2\left(\frac{\Delta C_{int}}{C_{int}}\right)} \\ &\simeq \sigma\left(\frac{\Delta V_{TON}}{V_{th}}\right) \equiv \frac{25.4\text{mV}}{3.3\text{V}/2} = 1.54\%\end{aligned} \tag{4.8}$$

Fig. 4.19 plots larger I_{dark} and G variances, whose effects can be fully compensated by means of the external calibration included I_{dark} and V_{th} in the ROICs. These results demonstrate the necessity of the digital programmability circuits introduced in Sec. 2.3.2 and 2.5.2. Like in the previous DPS-S100 design, no crosstalk is detected between any of the pixels of the focal plane.

Parameter	**DPS-S200**	**DPS-S130**	**Units**
Pixel size	200×200	130×130	μm
Dark current range	0.5 to 2.0	0.1 to 5.5	μA
Max. input capacitance	15		pF
Typ. signal range	1 to 1000		nA
Typ. frame rate	1000		fps
Typ. output dynamic range	10		bit
Inter-pixel crosstalk	< 0.5		LSB
Typ. FPN before tuning (±σ)	15	10	%
FPN after tuning	< 0.1		%
Typ. offset leakage error	0.2	2.3	LSB/f
Typ. gain leakage error	0.3	0.1	LSB/f
Program-in/read-out speed	10		Mbps
Supply voltage	3.3		V
Static power consumption	< 1		μW
Bias deviations (±σ)	15		%

Table 4.8 | Measured performance of the DPS-S200 and DPS-S130 cells for frame-based Smart imagers.

4.3 A Self-Biased 45μm-Pitch AER Pixel with Temporal Difference Filtering

The frame-free architectural proposals of Sec. 3.2.2, 3.3.2, 3.4.2 and 3.5.2 materialized into the 45μm-pitch frame-free Compact-pitch digital pixel sensor (DPS-C45) presented here. The IC was integrated in 0.18μm 1P6M CMOS technology in agreement with the functional description of Fig. 4.20 and under the operational specs of Table 4.9. Table 4.10 specifies the I/O signals employed to operate the DPS-C45 as indicated in the chronograms of Fig. 3.4(c) and Fig. 3.9(b).

Parameter	**Value**	**Units**
Dark current range	0.1 to 2	μA
Effective current range	0.1 to 2	μA
Temporal-difference tuning range	10-10k	Hz
Max. Throughput	10	Meps
Supply voltage	1.8	V
Max. static power consumption	$3I_{dark}$	-
Max. pitch	50	μm
DR	10	bit

Table 4.9 | Operational specs of the DPS-C45 prototype for frame-free Compact-pitch imagers.

4.3.1 Full-Custom ASIC Design

In its full-custom implementation, the pixel included cascoding in the TD filter loop to secure stability as justified in Sec. 3.3; external digital initialization was also incorporated into the tuning PLL and the log-domain TD blocks. The complete CMOS pixel layout is shown in Fig. 4.21. The location of DPS I/O pins and its 6-metal usage are depicted in Fig. 4.21(a,b). Concerning the full-custom layout style and pixel floorplan, the DPS-C45 introduced some new considerations with respect to previous pixel designs:

- Triple-well isolation was applied between pixels to avoid crosstalk through the die substrate.

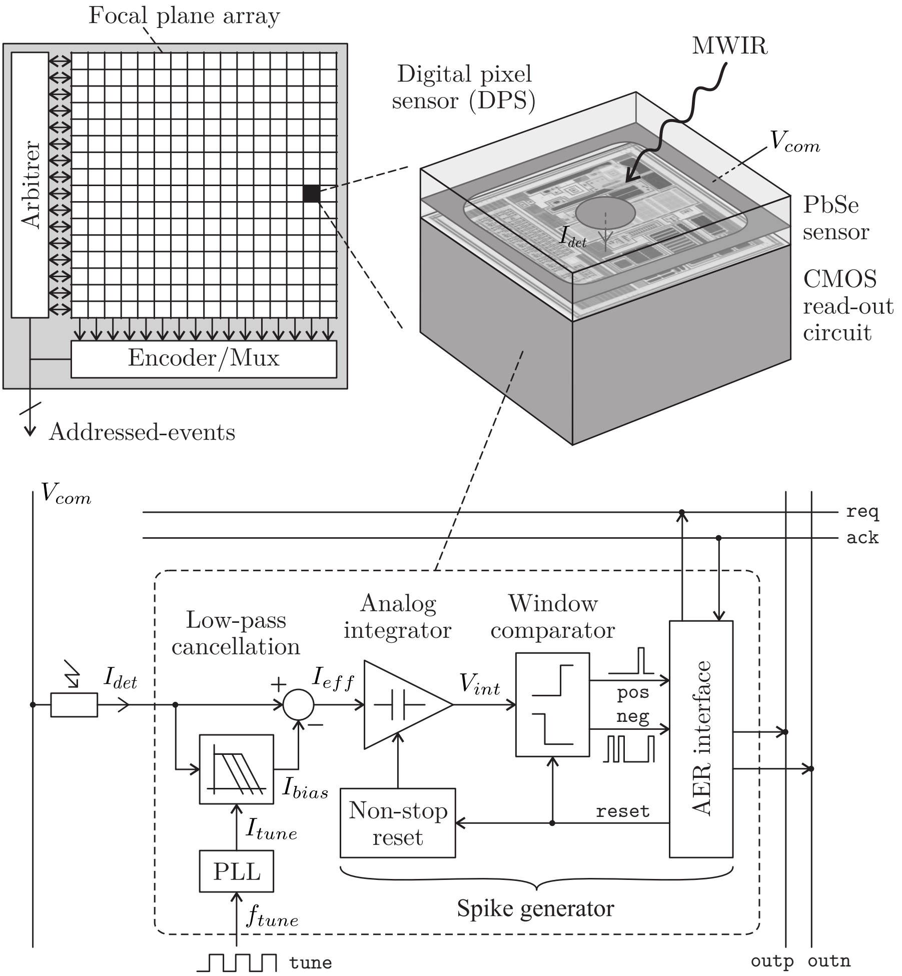

Focal plane array
Arbitrer
Encoder/Mux
Addressed-events
Digital pixel sensor (DPS)
MWIR
V_{com}
PbSe sensor
CMOS read-out circuit
I_{det}
V_{com}
req
ack
Low-pass cancellation
Analog integrator
Window comparator
I_{det}
+
I_{eff}
−
V_{int}
pos
neg
AER interface
I_{bias}
I_{tune}
PLL
f_{tune}
Non-stop reset
reset
Spike generator
tune
outp
outn

Figure 4.20 | Proposed architecture for the DPS-C45 cell.

- Power lines were arranged in a 2D grid to minimize resistance so pixel crosstalk through the voltage supply lines.
- The CTIA capacitors were implemented using the metal-insulator-metal (MIM) devices offered by the chosen technology instead of the polysilicon-insulator-polysilicon (PIP) implementations of the 2-PolySi CMOS technology employed in DPS-S cells.

Name	Type	Direction	Comments
`vdd`	P	-	Power supply
`gnd`	P	-	Power ground
`reset`	D	I	Analog integration reset
`reset_pll`	D	I	PLL reset
`tune1`	D	I	VCO reset
`tune2`	D	I	PLL-tuning signal
`ack`	D	I	AER row acknowledge input
`req`	D	O	AER row request output
`outp`	D	O	Positive event output
`outn`	D	O	Negative event output

Table 4.10 I/O diagram of the DPS-C45 cell for frame-free Compact-pitch imagers ((P)ower, (D)igital, (I)nput, (O)utput).

Like DPS-S200 and DPS-S130 designs, the passivation window of the top metal contact pad was set to 20μm. The bounding box of the pixel CMOS core was compacted to 45μm×45μm. In its matricial configuration as test imager, the pitch was artificially enlarged up to 50μm in order to comply with the target packaging of the integrated test platform (ITP) detailed in Sec. 5.1.

Although the DPS-C45 is oriented to operate jointly with other DPSs of the same type in an arbitrated FPA as depicted in Fig. 4.20, it was also integrated into a test cell in order to directly assess the performance of its main blocks. The test IC is shown in Fig. 4.22, and provided direct access to the signals `req`, `outp` and `outn` of the AER interface of Fig. 3.4, $\overline{\texttt{fast}}$, $\overline{\texttt{slow}}$ and `vco` of the PLL block of Fig. 3.9, and V_{int}, V_{high} and V_{low} of the integrate-and-fire stage of Fig. 3.13. All necessary biasing, pull-up and buffering circuitry were integrated at chip level as well.

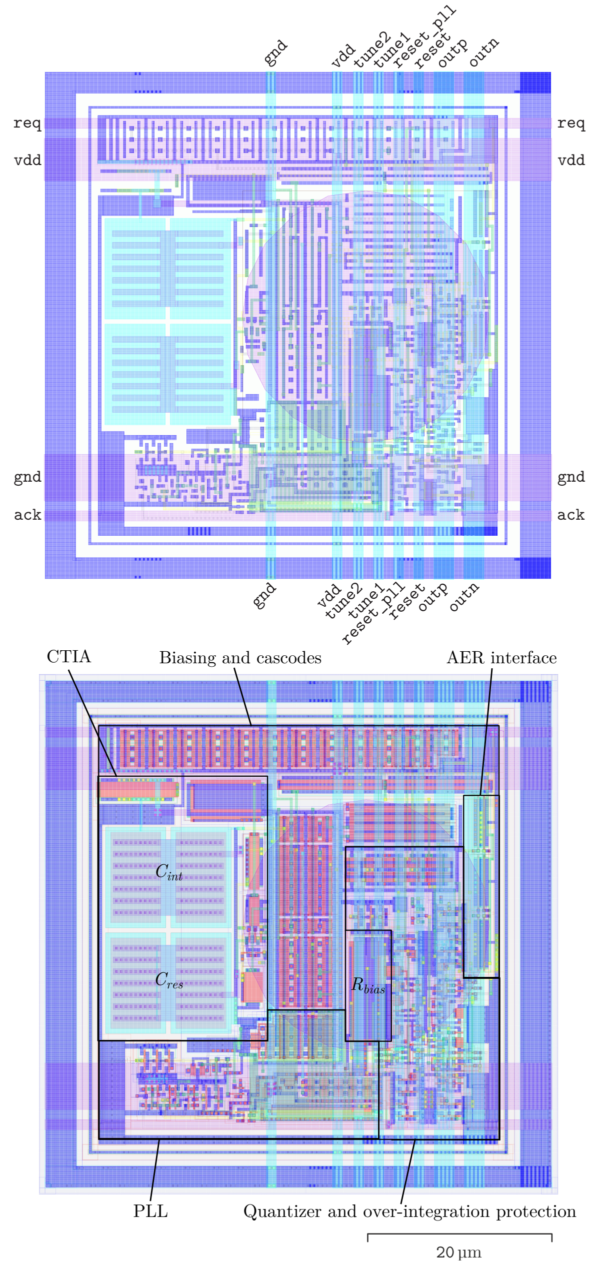

gnd
vdd
tune2
tune1
reset_pll
reset
outp
outn
req
vdd
gnd
ack
req
vdd
gnd
ack
gnd
vdd
tune2
tune1
reset_pll
reset
outp
outn
CTIA
Biasing and cascodes
AER interface
C_{int}
C_{res}
R_{bias}
PLL
Quantizer and over-integration protection
20 µm

Figure 4.21 CMOS layout of the DPS-C45 cell. Metal usage and I/O pin location in the AER pixel (a) and main block allocation (b).

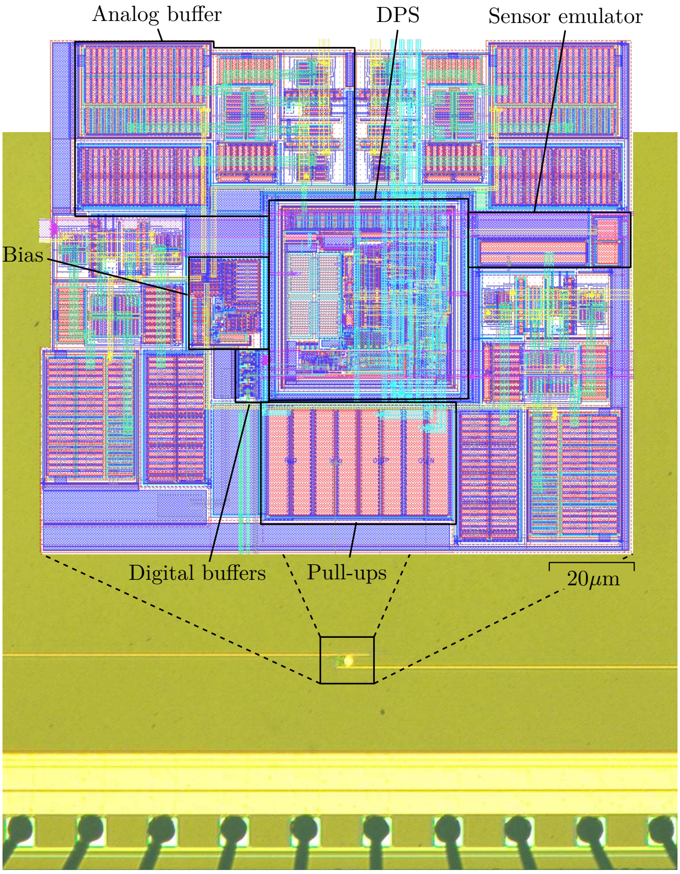

Analog buffer
DPS
Sensor emulator
Bias
Digital buffers
Pull-ups
20μm

Figure 4.22 | Physical CMOS layout of the test cell for the internal characterization of the DPS-C45.

4.3.2 Experimental Results

Unfortunately, the design of the DPS-C45 was seriously affected by innacurate leakage models supplied by the CMOS foundry. As illustrated in Fig. 4.23, the experimental leakages observed in test CMOS dies ranged 1nA, three orders of magnitude higher than nominal values. Posterior consultation with the foundry confirmed an strong underestimation of this parameter in simulation models.

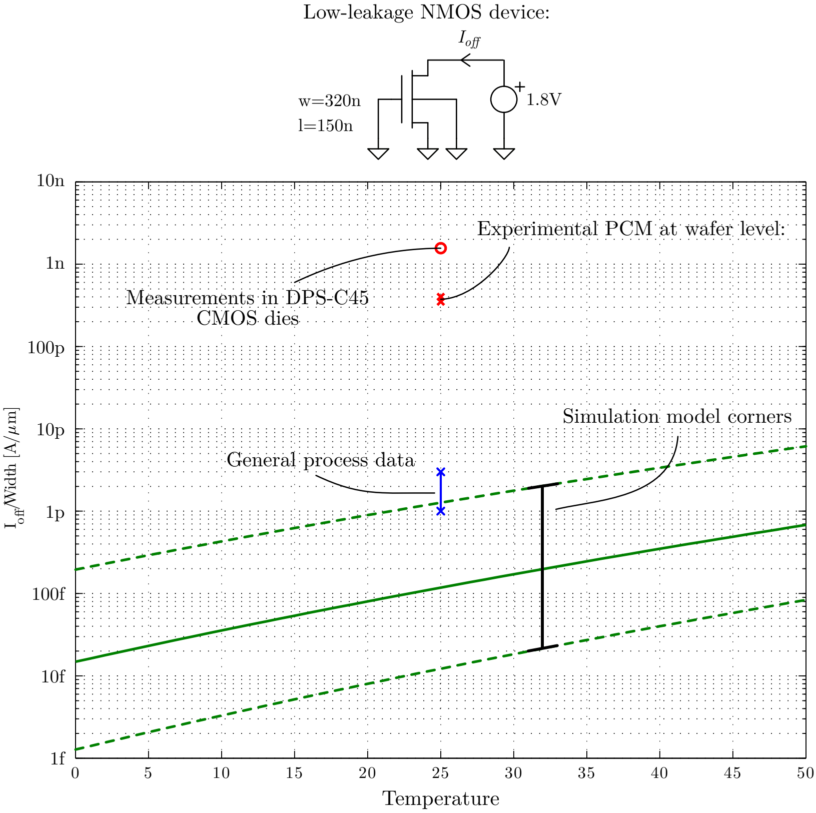


Figure 4.23 Experimental measurements vs. process reported leakage values for the CMOS technology adopted in the design of the DPS-C45.

Fig. 4.24 illustrates the critical effects of such high leakages on the overall operation of frame-free digital pixels. On the one hand, and according to simulation estimates, the high conduction of PMOS transistors in the PLL block unsettles its feedback loop by raising the gain of the charge-pump stage, and limits the programmable current-controlled oscillation range to a minimum high-pass corner of 1MHz. Such high corners not only completely invalidate temporal-difference tuning, but also have a dire influence on the stability of the filtering circuit. As rationalized in Sec. 3.3.2, the equivalent low R_{bias} of the GD transconductance brings the intendedly dominant

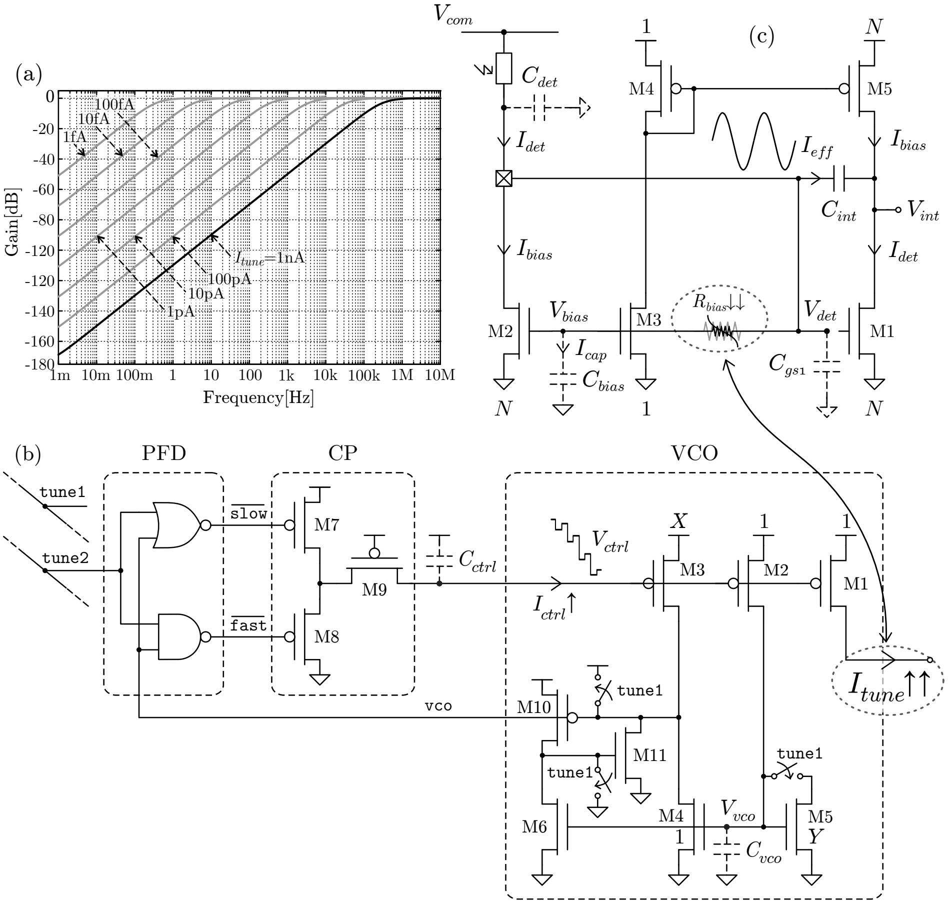

(a)
0
-20
-40
-60
-80
-120
-120
-140
-160
-180
Gain[dB]
1m 10m 100m 1 10 100 1k 10k 100k 1M 10M
Frequency[Hz]
100fA
10fA
1fA
Itune=1nA
100pA
10pA
1pA
(b)
PFD
CP
VCO
tune1
tune2
slow
fast
M7
M8
M9
Cctrl
vco
Vctrl
Ictrl↑
X
1
1
M3
M2
M1
M10
tune1
M11
tune1
tune1
M6
M4
1
Vvco
Cvco
M5
Y
Itune↑↑
(c)
Vcom
Cdet
Idet
Ibias
1
N
M4
M5
Ieff
Ibias
Cint
Vint
Idet
M2
Vbias
Icap
Cbias
M3
Rbias↓↓
Vdet
M1
Cgs1
N
1
N

Figure 4.24 Simulated log-domain high-pass filtering at room temperature (a) and critical effects of high-leakage devices on the functionality of the PLL (b) and TD (c) blocks of the DPS-C45 of Fig. 4.21.

$R_{bias}C_{bias}$ pole close over or even before the values of other high impedance nodes in the stage, leading to an inconsistent behavior of the DPS.

A new version of the DPS-C design is planned to be integrated in 0.18μm 1P6M CMOS technology in the next year for a succeeding industrial project.

Imager Test Chips in 2.5μm, 0.35μm and 0.15μm CMOS Technologies

5

5.1 A Low-Cost 32×32 Integrated Test Platform for Electrical Characterization of Imagers

The experimental validation of any integrated imager design is usually hard to achieve, since it involves not only the proper electrical test procedures of any IC, but also the development of a custom lab setup for optical characterization as well. Due to practical limitations, this optical part of the imager test has to deal with the following challenges:

- Quantitative control of the image contents at pixel level.
- Quantitative control of motion contents in video sequences.
- Repeatability and automation of the two previous points.

- In the particular case of the IR detectors of this thesis, mandatory access to the wafer for the PbSe CMOS post-processing. Due to integration costs, wafers are typically available only at the engineering run stage, long after the validation of the circuit prototypes.

In order to mitigate the above issues, a dedicated test chip platform is proposed in Fig. 5.1, which allows the accurate electrical test of full arrays of sensorless pixels already in the first CMOS prototyping stage, before sensor integration that may require pricey post-processing or hybrid packaging.

The basic idea is to replace the optical sensor in each pixel of the imager under test (IUT) by a flip-chip connection to an integrated array of current sources (I_{xy}) that can be individually programmed through a built-in digital interface. Since the ITP also allows the access to the inputs and outputs of the IUT, the full video signal processing chain can be automatically monitored. On the other hand, the new approach presented in Fig. 5.1 introduces extra costs linked to the flip-chip packaging and the necessity to access the ITP technology at wafer level. The latter is solved here by implementing the ITP in the low-cost in-house 2.5μm 2P1M CMOS technology, as detailed in Sec. 5.1.1.

The architecture of the ITP is presented in Fig. 5.2(a). The core of the chip is the bidimensional array of programmable current sources I_{xy} used to emulate the imager sensors and to stimulate each pixel of the IUT. The value of I_{xy} in a particular pixel is obtained from the combination of the row I_{ry} and column I_{cx} currents, which are programmed at every frame through the DAC circuits and the corresponding digital codes ry and cx.

The architectural approach of placing the image control blocks at row and column levels exhibits several advantages. First, the complexity of the pixel cell can be reduced in order to obtain compact pitch values. Second, programming circuits follow square-root law scalability with the number of pixels of the array, which is very attractive for large area imagers. Third, the amount of digital data to be transferred to the ITP in each frame is reduced, resulting in higher frame rates. On the other hand, arbitrary images cannot be generated with this strategy due to the partially shared programming of pixels by rows and columns. However, the final goal here is not the synthesis of any image content, like Fig. 5.3(a), but of moving test

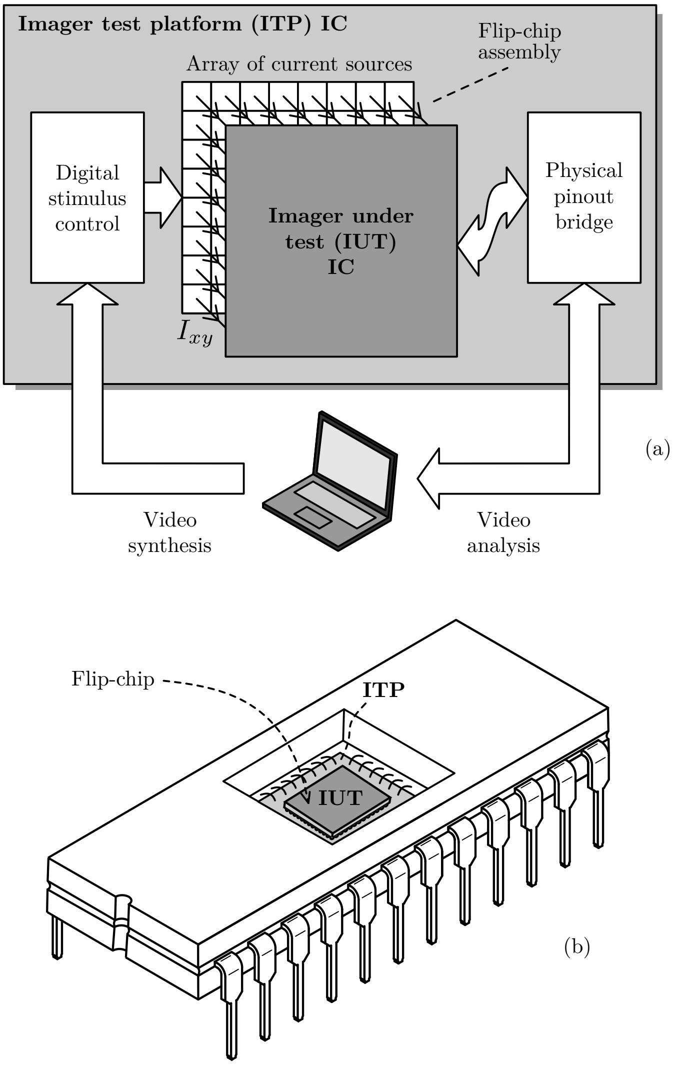

Imager test platform (ITP) IC
Flip-chip assembly
Array of current sources
Digital stimulus control
Imager under test (IUT) IC
Physical pinout bridge
I_{xy}
(a)
Video synthesis
Video analysis
Flip-chip
ITP
IUT
(b)

Figure 5.1 Functional (a) and physical (b) description of the ITP concept.

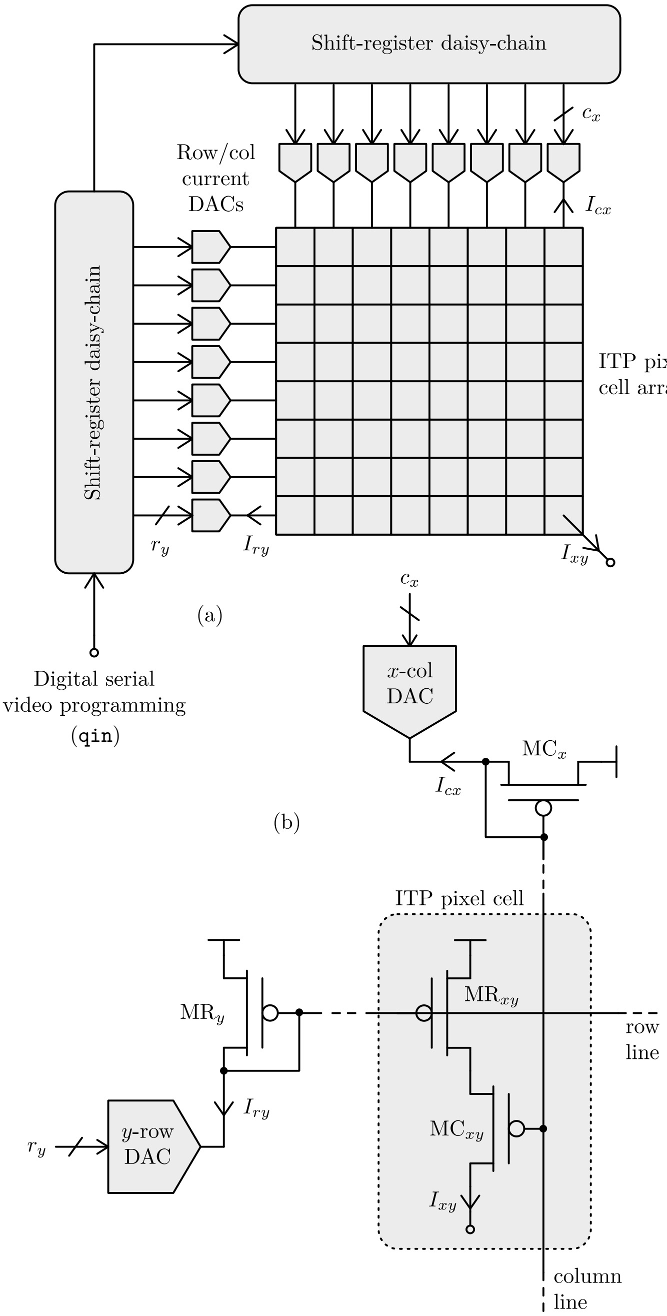

Shift-register daisy-chain
c_x
Row/col
current
DACs
I_{cx}
Shift-register daisy-chain
ITP pixel
cell array
r_y
I_{ry}
I_{xy}
(a)
Digital serial
video programming
(`qin`)
c_x
x-col
DAC
MC$_x$
I_{cx}
(b)
ITP pixel cell
MR$_y$
MR$_{xy}$
row
line
I_{ry}
r_y
y-row
DAC
MC$_{xy}$
I_{xy}
column
line

Figure 5.2 ITP architecture (a) and pixel cell with and row and column controls (b).

patterns such as rectangular areas, lines and gradients. Most of them can be generated by the the proposed ITP, as in Fig. 5.3(b,c).

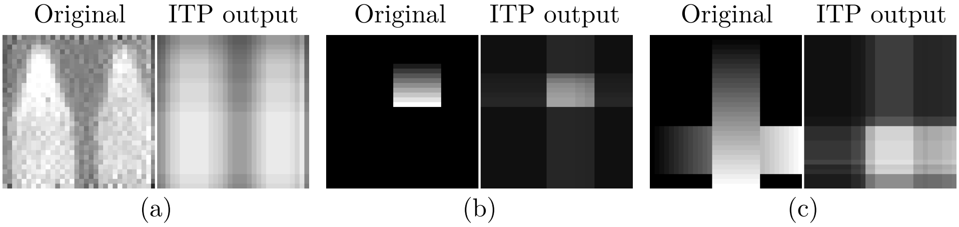


Figure 5.3 Examples of digital image synthesis using the proposed ITP for real life scenes (a) and regular patterns (b,c) using 16-level DACs. Image size is 32×32.

The CMOS topology of the ITP detector emulator is proposed in Fig. 5.2(b). The pixel cell is composed of only two transistors MR_{xy} and MC_{xy}, which are matched with their respective common row and column counterparts MR_y and MC_x. Supposing strong inversion operation for all devices and forward saturation for MC_{xy}, MR_y and MC_x, the resulting pixel current expression according to the EKV transistor model [96] is

$$I_{xy} = \frac{1}{4}\left(\sqrt{I_{cx}} - \sqrt{I_{ry}} + \sqrt{I_{ry} - I_{cx} + 2\sqrt{I_{ry}I_{cx}}}\right)^2 \tag{5.1}$$

According to the above analytical model, the current generated in each pixel is ideally independent from any technology parameter. This feature is of special interest to reduce FPN and to increase CMOS integration yield. On the contrary, the same expression shows a clear non-linear behavior respect to control parameters I_{ry} and I_{cx}. Nevertheless, the technological independence feature opens the possibility of compensating this non-linearity by digital pre-processing (e.g. look-up table). In order to validate this analytical model, general expression (5.1) is compared to the 2.5μm 2-polySi 1-metal CMOS CNM Technology (CNM25) electrical simulation of the circuit in Fig. 5.2(b) under two practical scenarios:

Row control only: the pixel current is swept through I_{ry} while keeping I_{cx} at a constant level. For our purposes, the general expression (5.1) is rewritten as a function of I_{ry} and normalized to I_{cx}:

$$\frac{I_{xy}}{I_{cx}} = \frac{1}{4}\left(1-\sqrt{\frac{I_{ry}}{I_{cx}}}+\sqrt{\frac{I_{ry}}{I_{cx}}-1+2\sqrt{\frac{I_{ry}}{I_{cx}}}}\right)^2 \qquad \text{for} \quad \frac{I_{ry}}{I_{cx}} > 3-2\sqrt{2} \sim 0.2 \tag{5.2}$$

The lower limit of $\frac{I_{ry}}{I_{cx}}$ in the above expression symbolizes the strong inversion region boundary for MR_{xy} in Fig. 5.2(b). Two characteristic points of this function can be identified:

$$\left.\frac{I_{xy}}{I_{cx}}\right|_{I_{ry}\equiv I_{cx}} = \frac{1}{2} \qquad \text{and} \qquad \lim_{\frac{I_{ry}}{I_{cx}}\to\infty} \frac{I_{xy}}{I_{cx}} = 1 \tag{5.3}$$

Fig. 5.4(a) shows a numerical comparison between the analytical expression (5.2) and the corresponding electrical simulation. It is clear from the returned results that not only the analytical model fits well with the typical electrical simulation within the strong inversion region of MR_{xy}, but pixel current also features a remarkable low technology dependence according to the corner analysis.

Column control only: In a similar way, the pixel current is generated by sweeping I_{cx} against a constant I_{ry} value. Here, the general expression (5.1) is rearranged into an I_{cx} variable normalized to I_{ry}:

$$\frac{I_{xy}}{I_{ry}} = \frac{1}{4}\left(\sqrt{\frac{I_{cx}}{I_{ry}}}-1+\sqrt{1-\frac{I_{cx}}{I_{ry}}+2\sqrt{\frac{I_{cx}}{I_{ry}}}}\right)^2 \qquad \text{for} \quad \frac{I_{cx}}{I_{ry}} < 3+2\sqrt{2} \sim 5.8 \tag{5.4}$$

Now, the upper limit of $\frac{I_{cx}}{I_{ry}}$ identifies the forward saturation boundary of MR_{xy} in Fig. 5.2(b). Like in the previous study, two characteristic points of this function are easily identified:

$$\left.\frac{I_{xy}}{I_{ry}}\right|_{I_{cx}\equiv I_{ry}} = \frac{1}{2} \qquad \text{and} \qquad \lim_{\frac{I_{cx}}{I_{ry}}\to 4} \frac{I_{xy}}{I_{ry}} = 1 \tag{5.5}$$

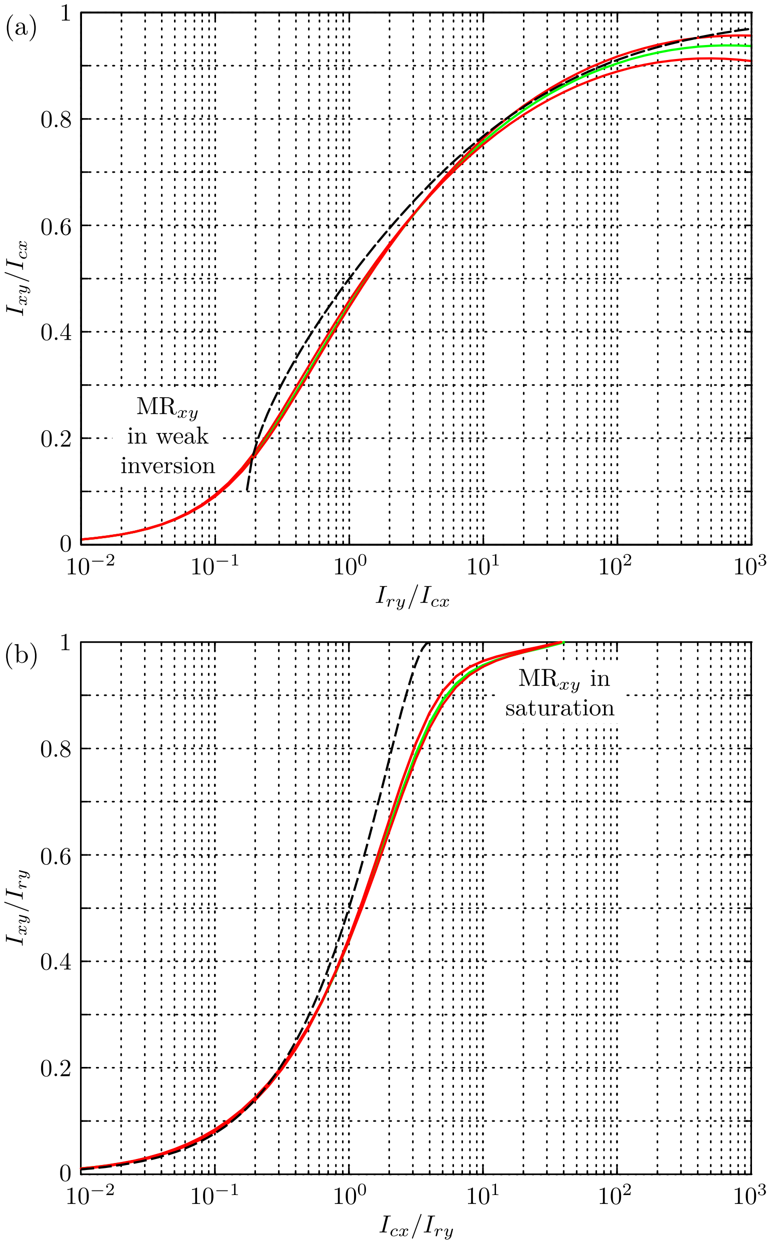


Figure 5.4 Analytical (black) versus typical (green) and corner (red) electrical simulations of the ITP pixel current for $I_{cx} = 1\mu$A (a) and $I_{ry} = 1\mu$A (b). Supply voltage is +5V

Fig. 5.4(b) plots a quantitative comparison between the analytical expression (5.4) and the corresponding electrical simulation. Again, the curves show good fitting between analytical and simulation models, and very limited technology variability.

5.1.1 Full-Custom ASIC Design

Based on the previous design, a 32×32 ITP example was integrated in the in-house 2.5μm 2P1M CMOS technology, and delivered in the form of 4" diameter wafers of the ITP chips suitable for the later flip-chip packaging of Fig. 5.1(b). The design of the IC adopted a conservative approach, adapted to the limitations of this low-cost CMOS technology such as:

- Single metal routing (combined with polySi).
- Low scaling factors (critical dimension is 2.5μm).
- High threshold voltage values (typ. > 1V).
- Lack of information about the estimated yield.

Additionally to the circuit of Fig. 5.2(b), the pixel cell of Fig. 5.5(a) incorporates an extra transistor M3 for generating the global background current I_{bkgd}. The latter is applied to all pixels in order to count for both, sensor dark current and image background illumination. In this sense, pixel current can be formulated as

$$I_{xt} = I_{bkgnd} + \frac{1}{4}\frac{I_{fs}}{16}\left(\sqrt{c_x} - \sqrt{r_y} + \sqrt{r_y - c_x + 2\sqrt{r_y c_x}}\right)^2 \qquad (5.6)$$

where I_{fs} stands for the equivalent signal full scale, while r_y and c_x are the digital programming codes for the 16-level row and column current DACs, respectively. Concerning the sizing of each MOSFET, minimum dimensions were avoided so as to improve the final yield of the full ITP. This pixel circuit can be operated at a supply voltage lower than the nominal +5V value to prevent any damage to the IUT.

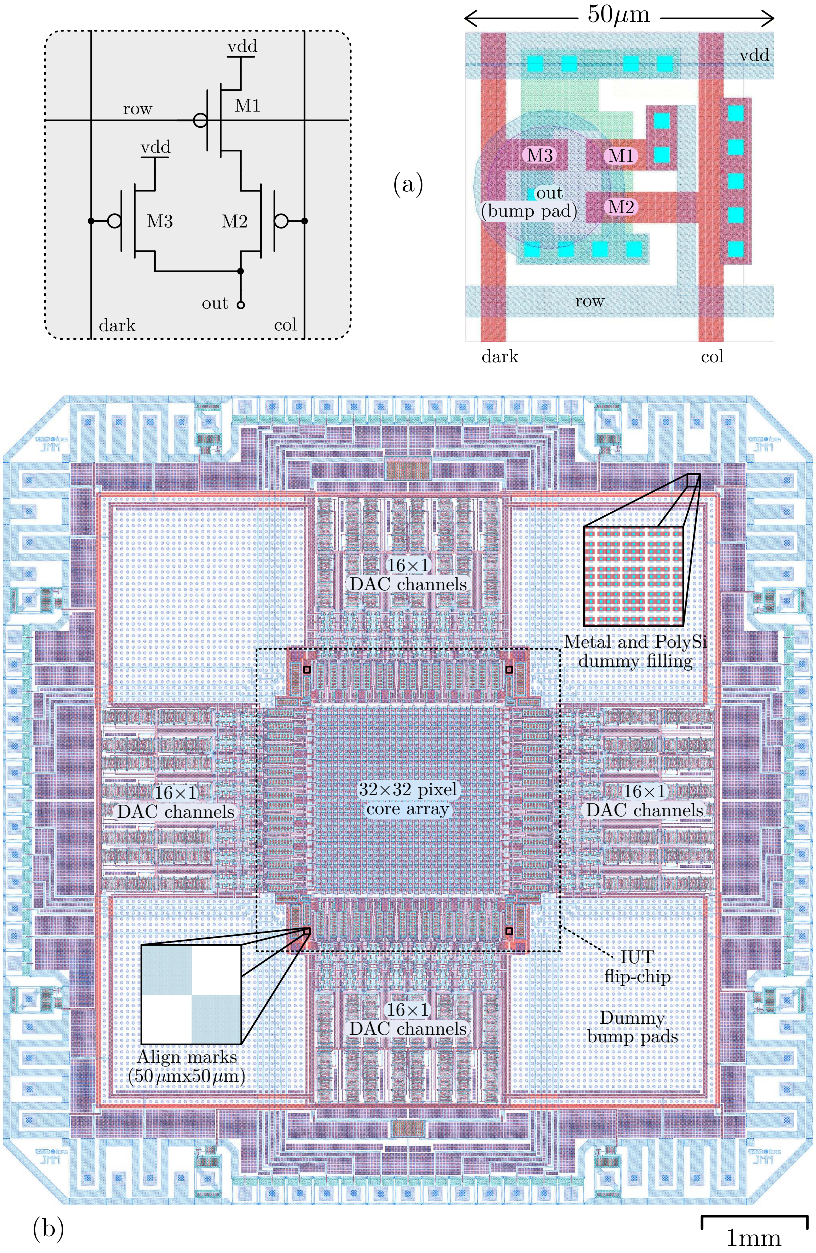

vdd
row
M1
vdd
M3
M2
out
dark
col
(a)
50μm
vdd
M3
M1
out
(bump pad)
M2
row
dark
col
16×1
DAC channels
Metal and PolySi
dummy filling
16×1
DAC channels
32×32 pixel
core array
16×1
DAC channels
IUT
flip-chip
Dummy
bump pads
16×1
DAC channels
Align marks
(50μmx50μm)
(b)
1mm

Figure 5.5 Pixel cell (a) and physical CMOS layout (b) of the ITP chip. Pixel bounding box is 50μm×50μm. Bump pad window diameter is 20μm.

From the physical CMOS design viewpoint, the ITP pixel can be adjusted for imagers down to 40μm pitch, but the final layout shown in Fig. 5.5(a) was enlarged to the maximum 50μm pixel-pitch spec of Table 4.9. The actual ITP device design is depicted in Fig. 5.5(b), where the different parts of the chip are identified. The overall size of the ITP die corresponds to one quarter of the CMOS technology reticle (15mm×15mm). Due to the downscaling limitations of the adopted in-house CMOS technology, the achievable pitch of row and column DAC control channels is considerably larger than the 50μm pitch of the ITP core array. In order to make them compatible, row (column) channels are alternated at left/right (up/down) sides of the array following a 2-level depth quincuncial arrangement. Every channel can be accessed independently following the operational chronogram of Fig. 5.6.

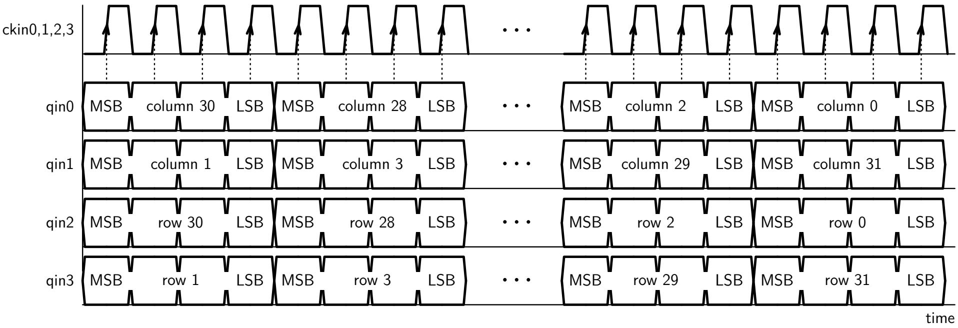

ckin0,1,2,3
qin0
MSB
column 30
LSB
MSB
column 28
LSB
MSB
column 2
LSB
MSB
column 0
LSB
qin1
MSB
column 1
LSB
MSB
column 3
LSB
MSB
column 29
LSB
MSB
column 31
LSB
qin2
MSB
row 30
LSB
MSB
row 28
LSB
MSB
row 2
LSB
MSB
row 0
LSB
qin3
MSB
row 1
LSB
MSB
row 3
LSB
MSB
row 29
LSB
MSB
row 31
LSB
time

Figure 5.6 General chronogram for the digital programming of the ITP of Fig. 5.5(b). Fully parallelized case.

Concerning power supply, a dual scheme of standard and low voltage levels was implemented. The former is the nominal value, and it is used everywhere except for the core array and the DAC stage. These two parts are connected to the IUT, so that their supply voltage can be lowered. A separated voltage source is also needed for the surrounding pad ring, which is devoted to drive all the peripheral electrostatic discharge (ESD) structures. The approximate bounding box of the imager flip-chip is also displayed in the same Fig. 5.5(b).

It is interesting to note at this point specific design for manufacturability (DFM) rules that were applied to the detailed layout, such as: dummy bump pads to improve control of the bump growing technological process, dummy metal and polySi filling to ease their CMOS processing, and the usage of metal over polySi when possible together with multiple contacts to increase the routing yield. A total number of 40 access points, distributed in 4 groups of 10 per corner, were routed from the flip-chip bridge to the ITP pads to provide direct access to the IUT power and communications. Also, 4 align marks of $50\mu m \times 50\mu m$ were included to aid the flip-chip packaging of the IUT. Fig. 5.7 illustrates the ITP core array I/O map, where `rio` signals constitute the IUT pinout bridge by bump bonding. Table 5.1 lists the pinout of the device.

In order to test the ITP chip itself, the phantom IUT of Fig. 5.8(a) was integrated together with the ITP in the same CMOS technology. This dummy die includes a simple routing map from some pixel locations to the pinout bridge of Fig. 5.7. Hence, the IUT-ITP flip-chip packaging of Fig. 5.8(b) enabled the direct measurement of a selected set of ITP pixel currents.

Name	**Type**	**Direction**	**Description**
`vdd2`	P	-	Core low supply voltage
`vdd5`	P	-	Core standard supply voltage
`vddp`	P	-	Pad supply voltage
`gnd`	P	-	Substrate ground
idark	A	I	Dark current (×50, sink)
ifs	A	I	DAC full-scale current (×100, sink)
`ckin0`	D	I	DAC clock for columns 0, 2, 4...30
`ckin1`	D	I	DAC clock for columns 1, 3, 5...31
`ckin2`	D	I	DAC clock for rows 0, 2, 4...30
`ckin3`	D	I	DAC clock for rows 1, 3, 5...31
`qin0`	D	I	DAC serial data for columns 0, 2, 4...30
`qin1`	D	I	DAC serial data for columns 1, 3, 5...31
`qin2`	D	I	DAC serial data for rows 0, 2, 4...30
`qin3`	D	I	DAC serial data for rows 1, 3, 5...31
`rio<0:39>`	P/A/D	I/O	IUT access points
`n/c`	-	-	Not connected

Table 5.1 Full list of the ITP pin-out for (P)ower, (A)nalog and (D)igital types and (I)nput and (O)utput directions. The physical location of each pin and the row/column origin are defined in Fig. 5.7.

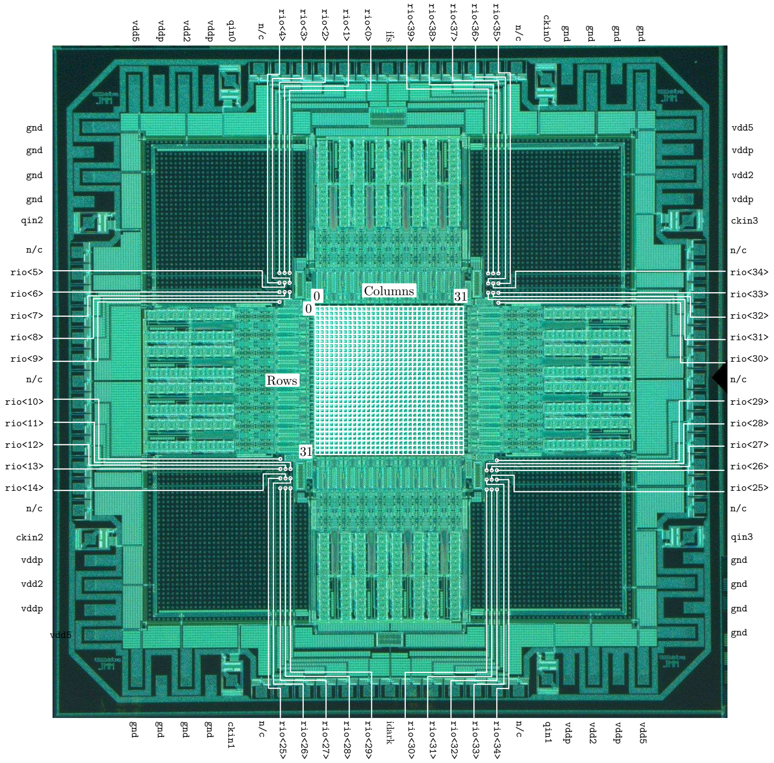

vdd5
vddp
vdd2
vddp
qin0
n/c
rio<4>
rio<3>
rio<2>
rio<1>
rio<0>
ifs
rio<39>
rio<38>
rio<37>
rio<36>
rio<35>
n/c
ckin0
gnd
gnd
gnd
gnd
gnd
gnd
gnd
gnd
qin2
n/c
rio<5>
rio<6>
rio<7>
rio<8>
rio<9>
n/c
rio<10>
rio<11>
rio<12>
rio<13>
rio<14>
n/c
ckin2
vddp
vdd2
vddp
vdd5
vdd5
vddp
vdd2
vddp
ckin3
n/c
rio<34>
rio<33>
rio<32>
rio<31>
rio<30>
n/c
rio<29>
rio<28>
rio<27>
rio<26>
rio<25>
n/c
qin3
gnd
gnd
gnd
gnd
Columns
0
31
0
Rows
31
gnd
gnd
gnd
gnd
ckin1
n/c
rio<25>
rio<26>
rio<27>
rio<28>
rio<29>
idark
rio<30>
rio<31>
rio<32>
rio<33>
rio<34>
n/c
qin1
vddp
vdd2
vddp
vdd5

Figure 5.7 Microscope photograph of the ITP, pinout and core array map.

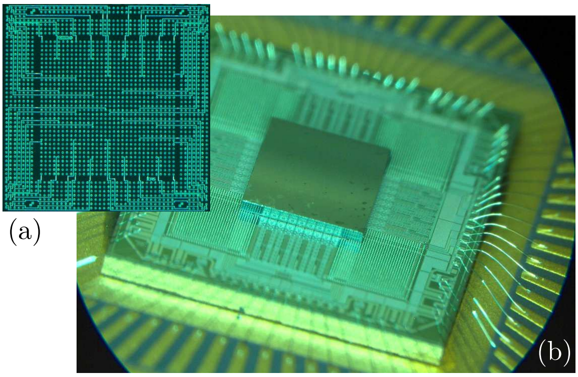


Figure 5.8 Phantom IUT chip (a) attached by flip-chip to the ITP chip (b). IUT die size is 3.5mm×3.5mm (12.3mm^2).

5.1.2 Experimental Results

Fig. 5.9 shows the experimental setup employed in the electrical characterization of the ITP prototype. The testbench included a Cyclone II field-programmable gate array (FPGA) development board connected to an extension ITP PCB in order to stimulate the device, a computer for the generation of test patterns and the programming-in of this data to the FPGA, and a Keithley 2636 Sourcemeter for the electrical measurement of the generated IR-emulated currents. Test boards were powered by a Promax FAC-662B voltage source.

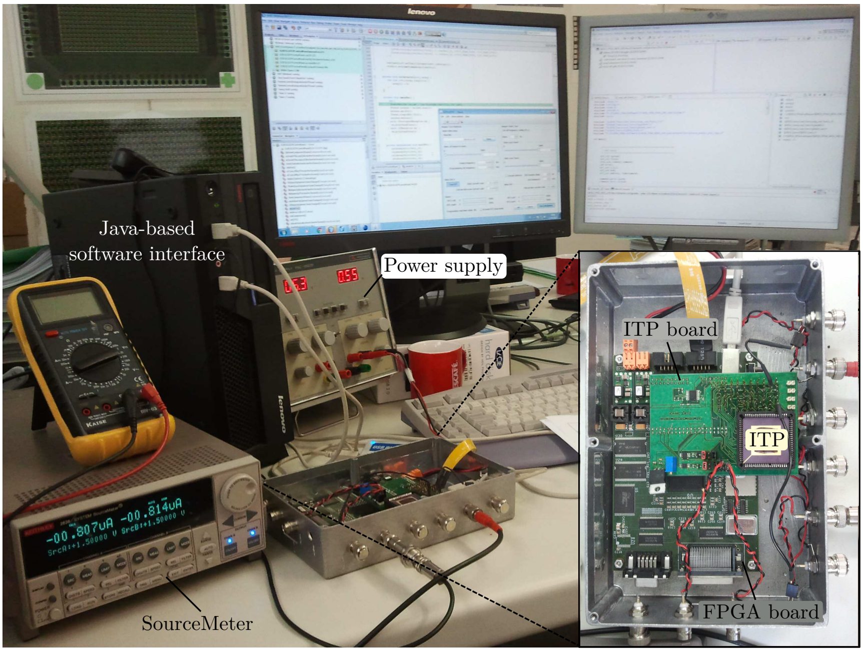


Figure 5.9 Electrical characterization testbench used for the ITP chip of Fig. 5.8(b) and the IUT chip of Fig. 5.27

In order to interact with both the ITP and the frame-free IUT chips, the FPGA was internally configured as drawn in Fig. 5.10. The embedded Nios microprocessor was programmed to act as front-end between the desktop computer and two integrated controllers: one module designed to configure the ITP of the present section, and another digital block conceived as control machine to monitor the incoming AEs [144–146] from the IUT of Sec. 5.3. Microprocessor and computer were interconnected via a Cypress SX2 chip by the universal serial bus (USB) 2.0 protocol and managed using a Java human-machine interface (HMI) based on the event-oriented jAER processing software [147] extended to run both gate-array implementations. The ITP was tested by performing a sweep of uniform luminance video sequences from the Java-based computer interface. The 4-bit column and row tuning codes were stored internally in the FPGA; the synchronous dynamic random access memory (SDRAM) included in the development board was devoted to record output events from the IUT in the experiments of Sec. 5.3.2.

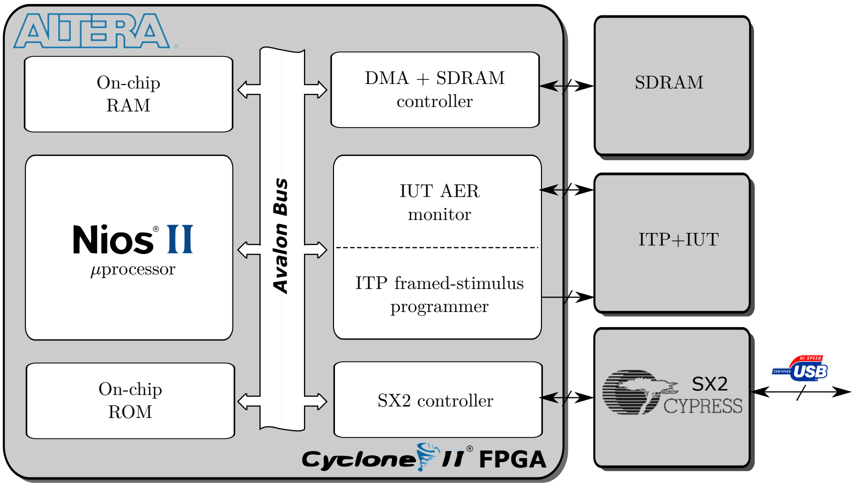

ALTERA
On-chip RAM
Nios II
µprocessor
On-chip ROM
Avalon Bus
DMA + SDRAM controller
IUT AER monitor
ITP framed-stimulus programmer
SX2 controller
Cyclone II FPGA
SDRAM
ITP+IUT
SX2
CYPRESS
USB

Figure 5.10 FPGA configuration employed to evaluate the ITP chip of Fig. 5.8(b) and the IUT chip of Fig. 5.27.

Experimental results are presented in Fig. 5.11 and Fig. 5.12 and summarized in Table 5.2. From the individual pixel programmability viewpoint, current ranges covered for both signal full scale and background levels are large enough to deal with most of the practical imager test cases. Also, digital DC transfer functions obtained in Fig. 5.11 from more than 50 pixels of 3 ITP dies show good alignment, with FPN standard deviation values below $5\%_{\mathrm{rms}}$. Concerning motion image generation capabilities, the fabricated ITP can deliver up to 10kfps with smart transitions between frames, as reported in Fig. 5.12.

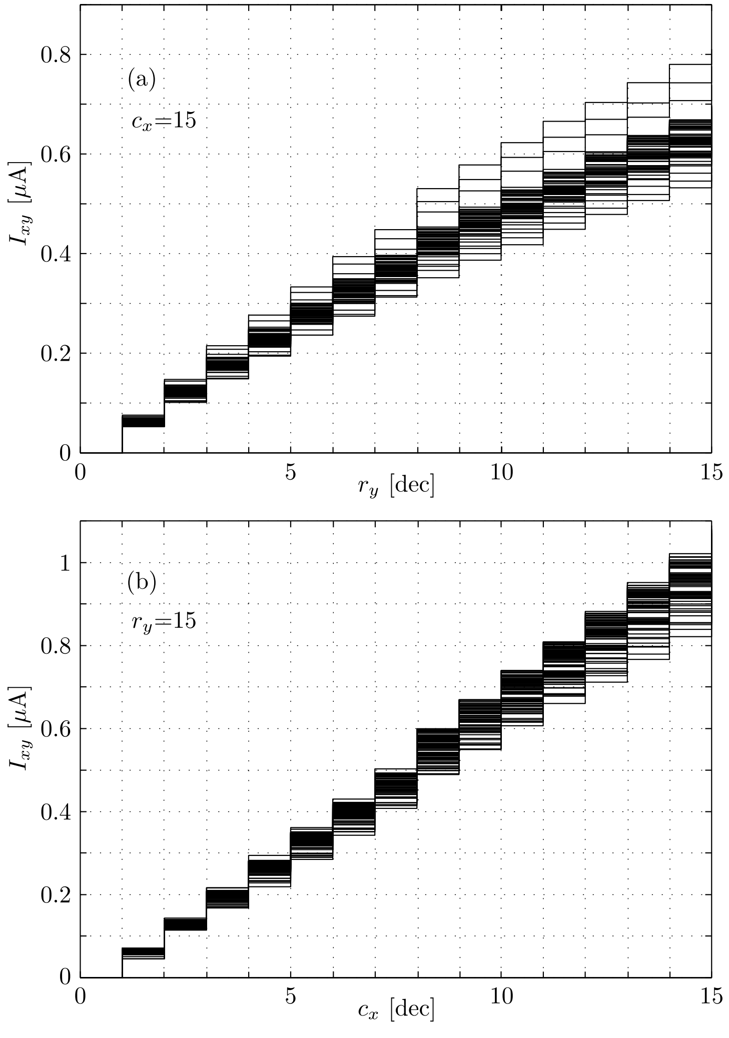


Figure 5.11 Measured ITP pixel current curves versus digital row (a) and column (b) programming for $I_{bkgd} = 0$ and $I_{fs} = 1\mu$A.

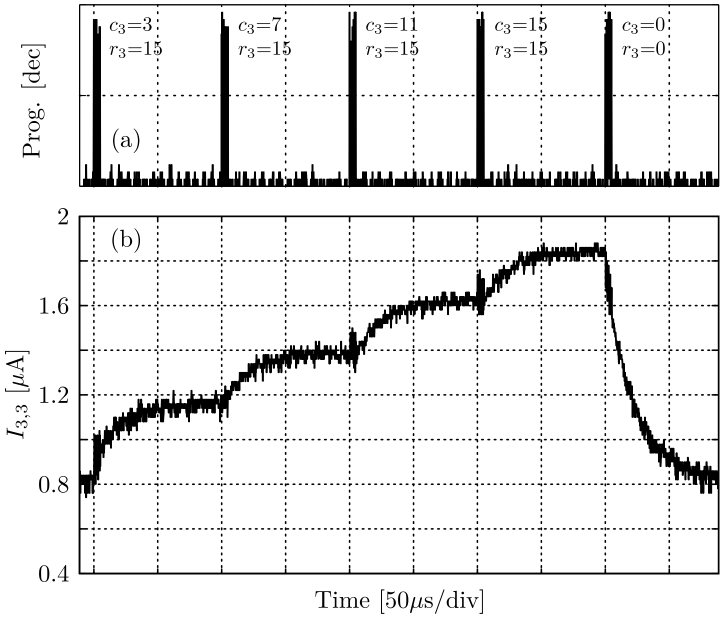


Figure 5.12 Example of dynamic programming at 12.5Mbps (a) and generated current at 10kfps (b) of an ITP pixel (3,3) for $I_{bkgd} = 0.8\mu$A and $I_{fs} = 1\mu$A.

Parameter	Value	Units
Array size	32×32	μm
Pixel pitch	50	μm
Digital row×col control	4×4	bit
Full-scale current range	0 to 4	μA
Background current range	0 to 10	μA
FPN	< 5	$\%_{\rm rms}$
Max. program-in rate	20	Mbps
Max. imaging rate	10	kfps
Supply voltage	5	V
Die area	7.2×7.2	mm^2

Table 5.2 Performance summary of the ITP device of Fig. 5.8(b).

5.2 An 80×80 Sub-1μW/pix 2kfps Smart MWIR Imager

The satisfactory electrical results obtained from the test chips of Sec. 4.2 pushed the frame-based Smart architecture into its final validation as 32×32 and 80×80 industrial imagers. The resulting commercial system of this section inherited the operational scheme and the physical design of latest DPS-S130 cells, with the only exception of rounding up inter-pixel spacing to the 135μm imposed by the Au lithography of the PbSe MWIR detector shown in Fig. 1.5. The I/O diagram is also almost identical to the one detailed in Table 4.2, but for the 32 and 80 lines of the now `qin` and `qout` buses and the inclusion of the V_{com} signal to bias the common terminal of the pixelated detectors of Fig. 1.5. Matricial implementations were corroborated in a previous multi-project wafer (MPW) through a 32×32-pixels test chip. The development of this intermediate ASIC is not detailed here for its evident similitude to the system described below.

Basically, in its highest available spatial resolution, the imager is constituted of a digital-only I/O focal plane of 80 fully independent rows of daisy chains of 80 DPS cells each, and integrates all functionality locally inside each pixel avoiding any analog signal sharing between them. The PbSe photoconductor of Sec. 1.4 is deposited by VPD on the surface of the FPA. All pixels in the FPA are accessed by rows, and operated according to two iterative global modes of Fig. 4.12 as schematized in Fig. 5.13: synchronous communication and asynchronous acquisition.

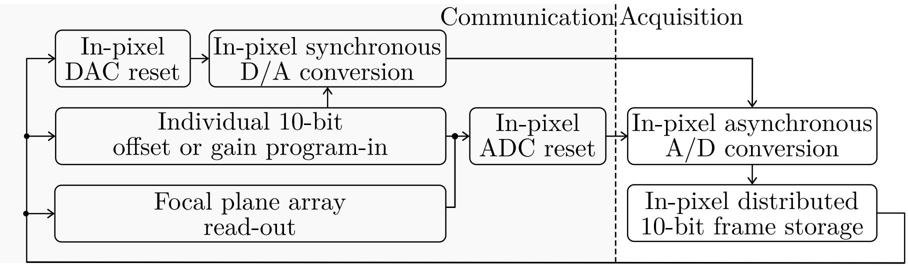

Communication
Acquisition
In-pixel DAC reset
In-pixel synchronous D/A conversion
Individual 10-bit offset or gain program-in
In-pixel ADC reset
In-pixel asynchronous A/D conversion
Focal plane array read-out
In-pixel distributed 10-bit frame storage

Figure 5.13 | Basic operation flow of the Smart IR imager.

During communication, the 10bit/pix correction maps are serially written-in through the bus of row inputs, and translated to their corresponding in-pixel analog circuit configuration; at the same time and without any speed penalty, the 10bit/pix compensated frames are also serially read-out through the bus of row outputs. Offset and gain maps are entered in different programming-in/read-out time slots (e.g. alternate frames) at a variable refreshing frequency adjustable to system requirements. Over acquisition, all pixels in the FPA are set up to collect the detector currents and to asynchronously integrate their effective values to digital 10-bit words.

5.2.1 Monolithic PbSe-CMOS Integration

As DPS-S cells contain all functionality in the pixel itself, imager implementations were constructed by simple arrangement of the basic cells in FPAs of N_{pix}^2 dimensionality but for the inclusion of I/O buffering at pad level, and the symmetrical clock-tree of Fig. 5.14. This two new additions were pursued to boost communication speed and avoid data corruption. The clock tree was buffered at four levels: input pad, routing at both sides of the FPA, DPS row and in every register of the pixel sensor.

Both 32×32 and 80×80 imagers were integrated over 8 inch wafers with standard 0.35μm 2P4M CMOS technology. In order to monolithically post-process PbSe detectors on top of CMOS circuits, two key technological bottlenecks had to be saved: compatibility between detector and circuit materials at their interface, and CMOS operational drifts that PbSe sensitization treatments at high temperature could induce. For the former, PbSe was contacted by gold (Au) as detailed in Sec. 1.4.1. For the latter, a two-fold strategy was selected as follows: PbSe post-processing was redefined in order to lower the temperature and duration of each technological step, and design rules for high-stress environments were rigorously contemplated conforming to advice from the foundry. All phases and masks were optimized to the concrete CMOS technology and wafer size of the engineering run.

As shown in the layout of Fig. 4.15 and the micrograph of Fig. 5.15(c), metal 4 was reserved for power line routing and to access the MWIR detector. Control lines were routed horizontally using metal 3, also employed to shield the in-pixel SC-DAC. Inside the FPA, pixels were arranged in alternate

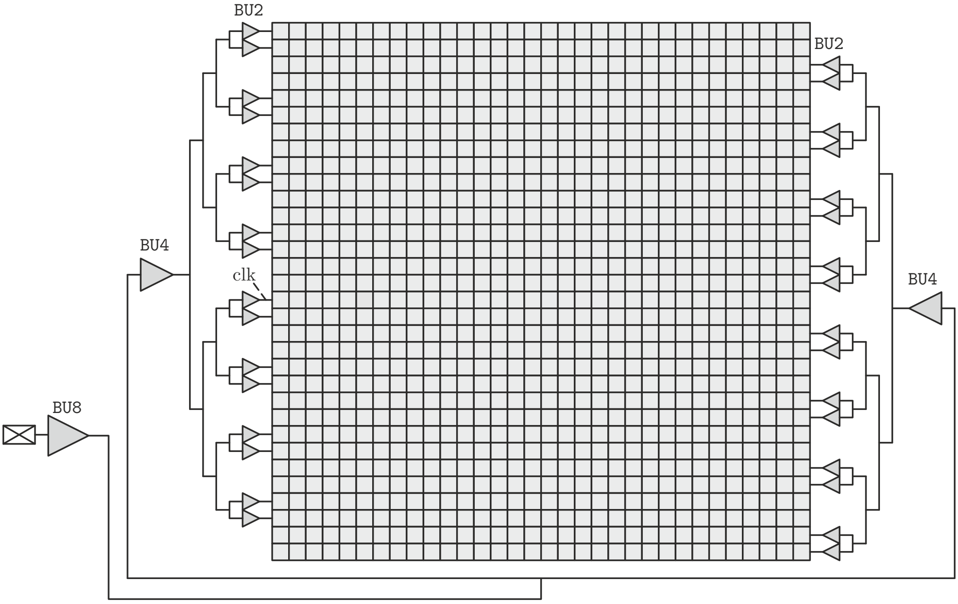


Figure 5.14 Example of clock tree distribution for a 32×32-pixel Smart MWIR imager, following the same distribution that 80×80 FPAs. `BU8`, `BU4` and `BU2` stand for 8, 4 and 2mA digital buffers, respectively.

left-right row I/O directionality to ease external daisy-chain connectivity. The fabricated imager occupied a total area of 14×14 mm^2 with 196 pads distributed along the four sides of the die. The succeeding low-cost packaging procedure included the following steps: Firstly, a rectangular sapphire glass was used in order to coat and protect the FPA from damaging external contamination or scratch. Wafers were then diced by laser and all pads of the ROIC were wire-bonded to the custom chip-carrier PCB of Fig. 5.16. The board accesses the focal plane in 5-row groups, with an equivalent 16-bit I/O bus, matching standard 64-pin leadless chip carrier (LCC) sockets. Is this external serialization which, in practice, limits the maximum frame rate of the imager to an equivalent 480×480 pixel FPA parallel-access time. Packaging was finally sheltered using standard dam-and-fill techniques.

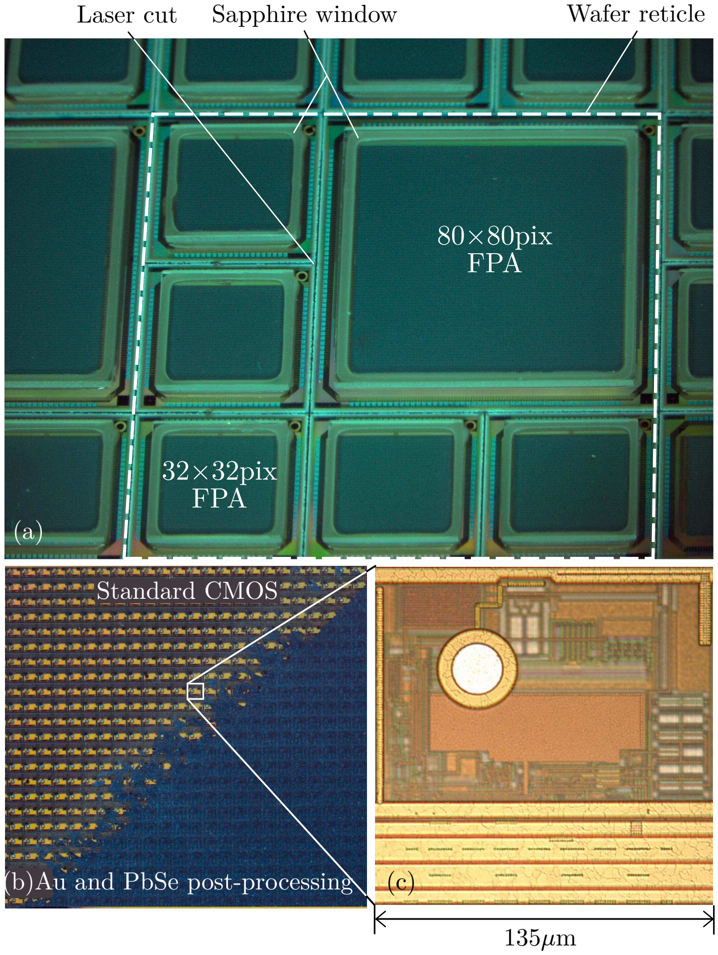

Laser cut
Sapphire window
Wafer reticle
80×80pix
FPA
32×32pix
FPA
(a)
Standard CMOS
(b)Au and PbSe post-processing
(c)
135μm

Figure 5.15 Microscope photograph of the VPD PbSe post-processed wafer with sapphire protection (a), FPA detail with (bottom-right) and without (top-left) Au and PbSe deposited on top (b), and pixel detail before post-processing (c).

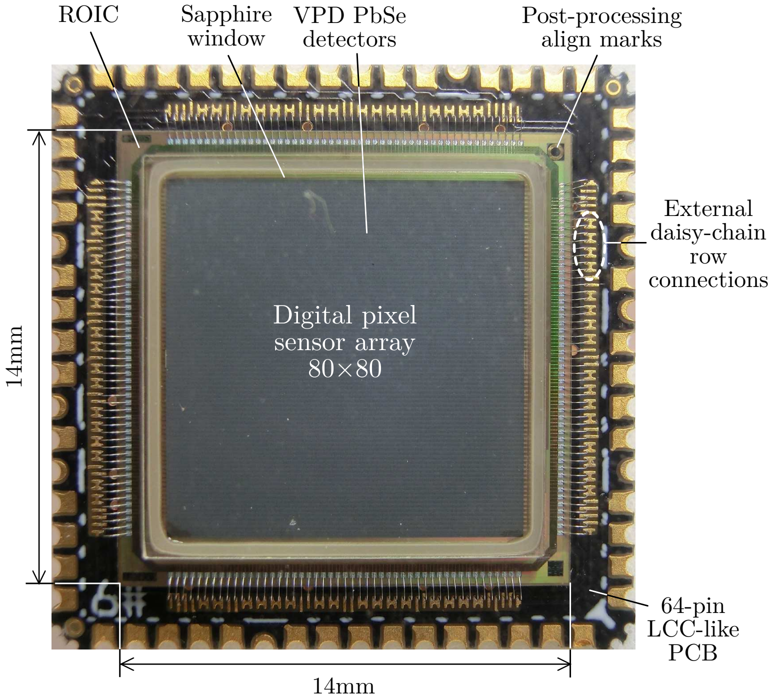

ROIC
Sapphire window
VPD PbSe detectors
Post-processing align marks
External daisy-chain row connections
Digital pixel sensor array 80×80
14mm
64-pin LCC-like PCB
14mm

Figure 5.16 Micrograph of the Smart MWIR imager fabricated in 0.35μm 2P4M CMOS technology with VPD PbSe post-processing. The ROIC is directly wire bonded to chip-carrier PCB for 64-pin LCC-like sockets.

5.2.2 Experimental Results

The integrated imager was electrooptically tested after on-wafer screening using the setup shown in Fig. 5.17. This test bench was composed of a CI Systems SR-200 high-emissivity IR blackbody with mechanical chopping, a National Instruments (NI) PXI-1042 8-slot digital measurement system and a Pegasus S200 semi-automatic 200-mm probe station from Wentworth Laboratories. Custom NI Labview-based interfaces were developed for both on-wafer and in-package testing, which included the generation of the operational chronogram of Fig. 4.12.

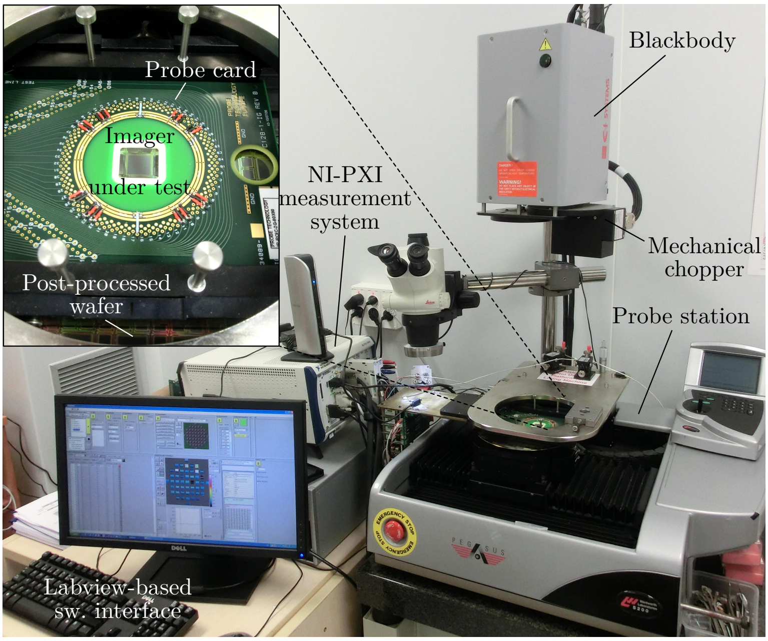

Probe card
Imager
under test
Post-processed
wafer
NI-PXI
measurement
system
Blackbody
Mechanical
chopper
Probe station
Labview-based
sw. interface

Figure 5.17 Electrooptical validation setup used for imager screening at wafer level. Experimental results were obtained utilizing the same blackbody and NI-PXI measurement system.

Fig. 5.18 shows the experimental tuning response of 24 different DPS cells to both offset and gain parameters. Measurements were taken without IR illumination. In the first case, all gain programming codes (i.e. $\mathtt{d_{gain}}$) were fixed to 226LSB. The full 10-bit range of the in-pixel SC-DAC is devoted to match the dark current (I_{dark}) dispersion exhibited by PbSe detectors according to the $\mathtt{d_{offset}}$ tuning curve of Fig. 5.18(a) and (2.16). Gain programming was performed after individual pixel offset calibration so that all outputs are aligned at half full scale for the same gain code of 226LSB. As it can be clearly seen in Fig. 5.18(b), digital output reading follows the expected $1/x$ law also predicted by (2.16). Under negligible reset times and zero V_{ref} reset CTIA voltage, substituting V_{th} by (2.47) in (2.16) results in the tuning characteristic

$$\mathtt{q_{out}} = \frac{T_{acq}}{C_{int} G_{DAC} \mathtt{d_{gain}}} (I_{det} - I_{dark}) \tag{5.7}$$

inversely proportional to the input gain programming code. Integral nonlinearities arise mainly from capacitive mismatching at both sample and hold nodes, and residual change injection and clock feedthrough effects at DAC switches. In practice, there is a lower boundary at which the reference voltage for the comparator of Fig. 2.16 is no longer operative. Higher values are not effective either, as the transfer curve saturates beyond the MSB gain code. Thus, V_{th} is programmed within a 9-bit span in order to compensate variations on both detector sensitivity and ADC conversion gain. The statistical results of Fig. 5.19 were obtained applying the same programming codes to the whole set of 6400 pixels of the focal plane, and corroborate the necessity of the included FPN correction mechanisms at pixel level.

Experimental results of the built-in FPN cancellation capabilities are presented in Fig. 5.20 to 5.22. All characteristics reported in this section were obtained setting the clock frequency to 10MHz during communication phase except for the final 10 clock periods devoted to in-pixel DAC operation, when it was scaled down to 3MHz. To generate large and uniform illumination, a 1173K IR dark body was placed 10.75cm away from the imager of Fig. 5.16, and signal strength was regulated by using 8 different apertures. Integration time was 500μs for an operating frame rate of 1.1kfps. No optics were used in these measurements.

The raw image shown in Fig. 5.20(a) corresponds to the digital read-out with null IR illumination when flat FPN code maps are programmed in all active pixels. On-chip frame equalization is achieved in Fig. 5.20(b) after

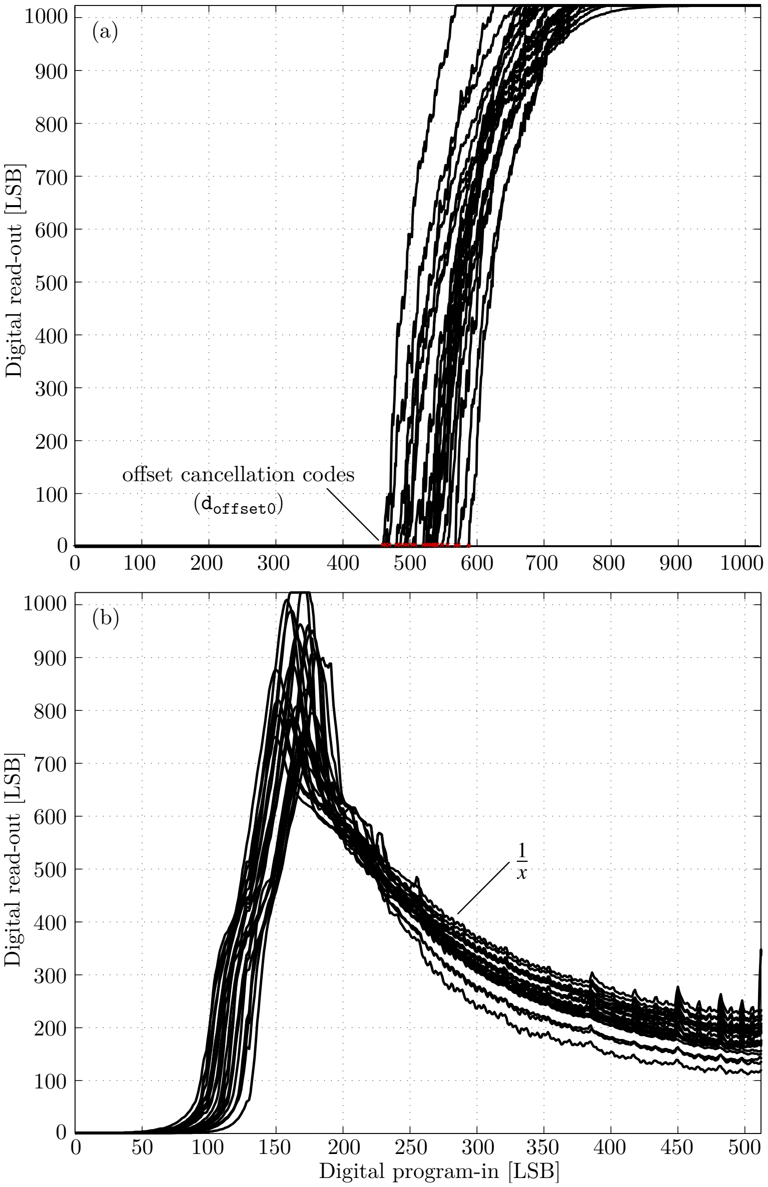


Figure 5.18 Experimental offset (a) and gain (b) tuning curves of 24 DPS cells distributed over the 80×80-pixel FPA. Operating conditions are no IR illumination and $\mathtt{d_{gain}} = 226\text{LSB}$ (a), and calibrated $\mathtt{d_{offset}}$ to achieve $\mathtt{d_{out}} = 512\text{LSB}$ at $\mathtt{d_{gain}} = 226\text{LSB}$ (b). Results averaged over 150 frames from the same FPA with $\bar{\sigma}_{\bar{\mathtt{d}}_{\mathtt{out}}} = 4\text{LSB}$.

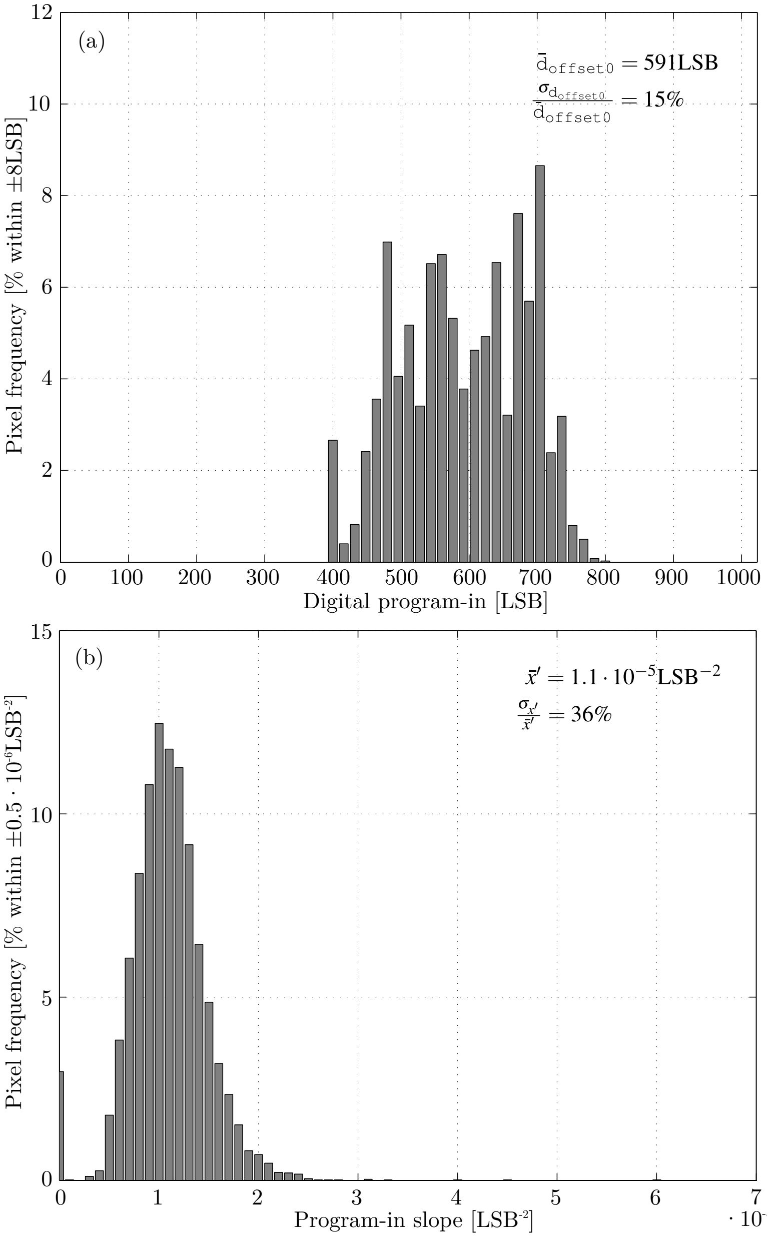


Figure 5.19 Experimental deviations of offset cancellation codes (a) and gain programming slope values (b) of the 6400 DPS cells of the entire FPA of Fig. 5.16.

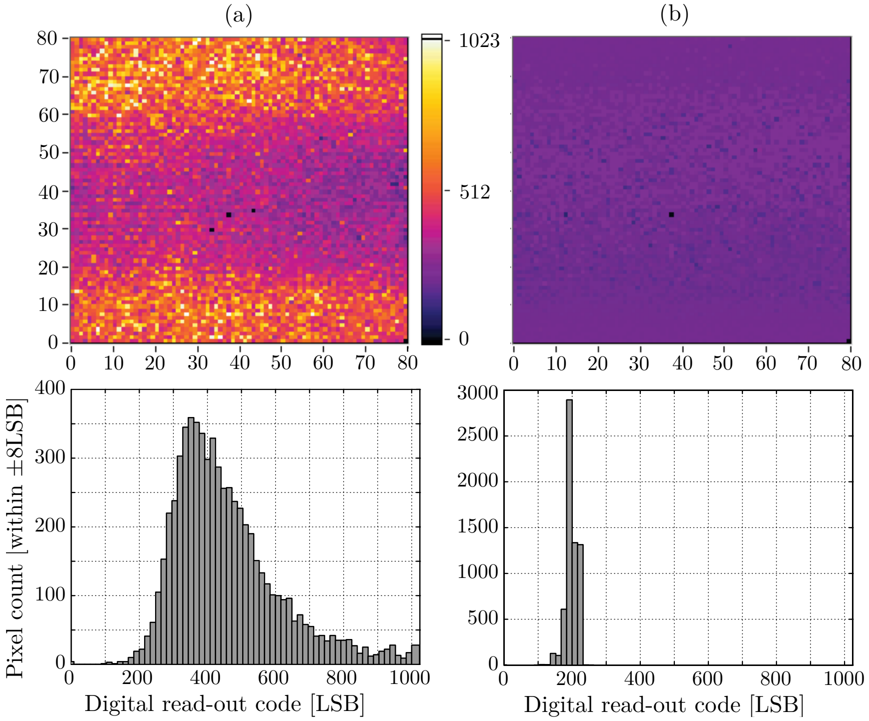


Figure 5.20 Measured image and read-out dispersion before (a) and after (b) in-pixel FPN equalization.

applying offset and gain correction. Both maps are previously computed by an automatic calibration routine running in the NI-PXI system, configured in this case for the decimal output reading code 200LSB, but reducible down to 50LSB for the target DR extension of 60dB. FPN calibration fingerprints are stored in the same system and recomputed only in case of severe temperature drifts. Fig. 5.21 shows pixel-to-pixel, row-to-row and column-to-column FPN statistics, expressed in percentages over full scale (1023LSB), for the entire focal plane. Non-uniformities in the imager arise at row level in the direction of power line routing. Calibration of the image sensor manages to reduce all FPN values under 5% full scale. FPN decays in the right side of the figure are caused by saturation of pixel digital counts. Pre and post-equalization imager read-out codes evolve as described in (2.16), with good linearity up to the frequency limit imposed by T_{reset}, as reported in Fig. 5.22. Concerning temporal noise, the NETD results of Fig. 5.23 were measured throughout the 49 dices that compose a full wafer. NETD improves with temperature according to the higher irradiance of hotter surfaces, displaying variances below 10%. Instantaneous read-out noise was measured 4LSB for an acquisition time of 200μs.

Fig. 5.24 presents dynamic captures of the MWIR imager, under uncooled operation, to a 330Hz pulsing bright spot generated by mechanical chopping. Dark body temperature is in this case 773K, placed at a distance of 40cm from the FPA, using 3cm focal length and f/1 aperture optics. The resulting digital frame sequence read at 1650fps ratifies the speed capabilities of the imager. In the same figure, the ignition sequence of a lighter is also given as a practical high-speed application example. In proof of image uniformity and sensitivity, Fig. 5.25 shows two raw photograms acquired at this same rate from different scenes and devices. The absence of inter-pixel crosstalk evinces from the spatial acuity of disk slots in Fig. 5.25(a), even with the small array size and current detector pitch constraints of the imager. Fig. 5.25(b) displays effective temperature screening for a fast-moving flame. In terms of production yield, the total amount of operative pixels exceeds the 99.9% of every FPA. Dead pixels are essentially sparse and can be easily interpolated though posterior post-processing.

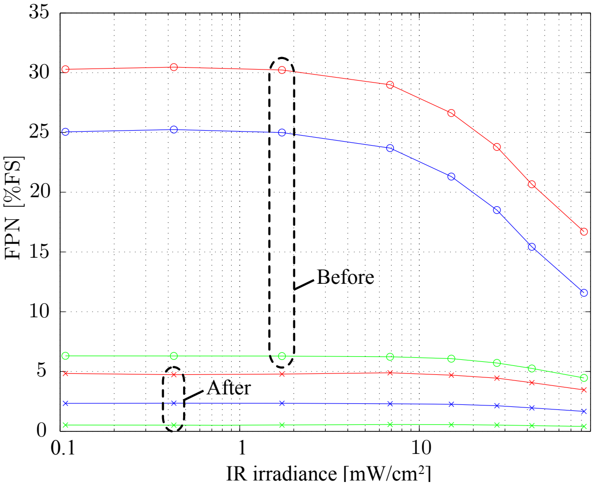


Figure 5.21 Measured image pixel-to-pixel (red), row-to-row (blue) and column-to-column (green) FPN versus incoming IR irradiance before and after in-pixel FPN equalization.

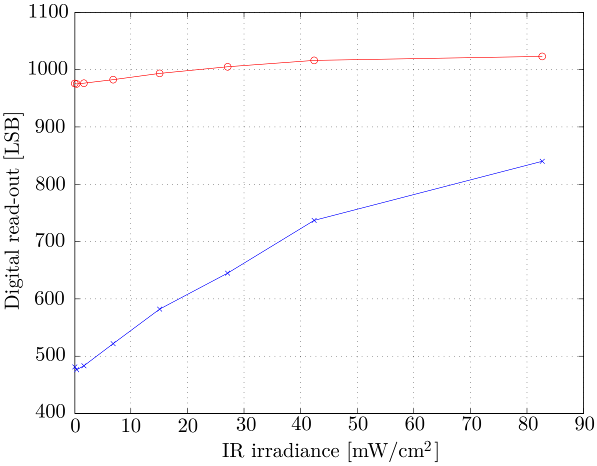


Figure 5.22 Average saturated-pixel read-out values over imager focal plane versus incoming IR irradiance before (red) and after (blue) in-pixel equalization. Offset is calibrated at 480LSB read-out in order to reach saturation.

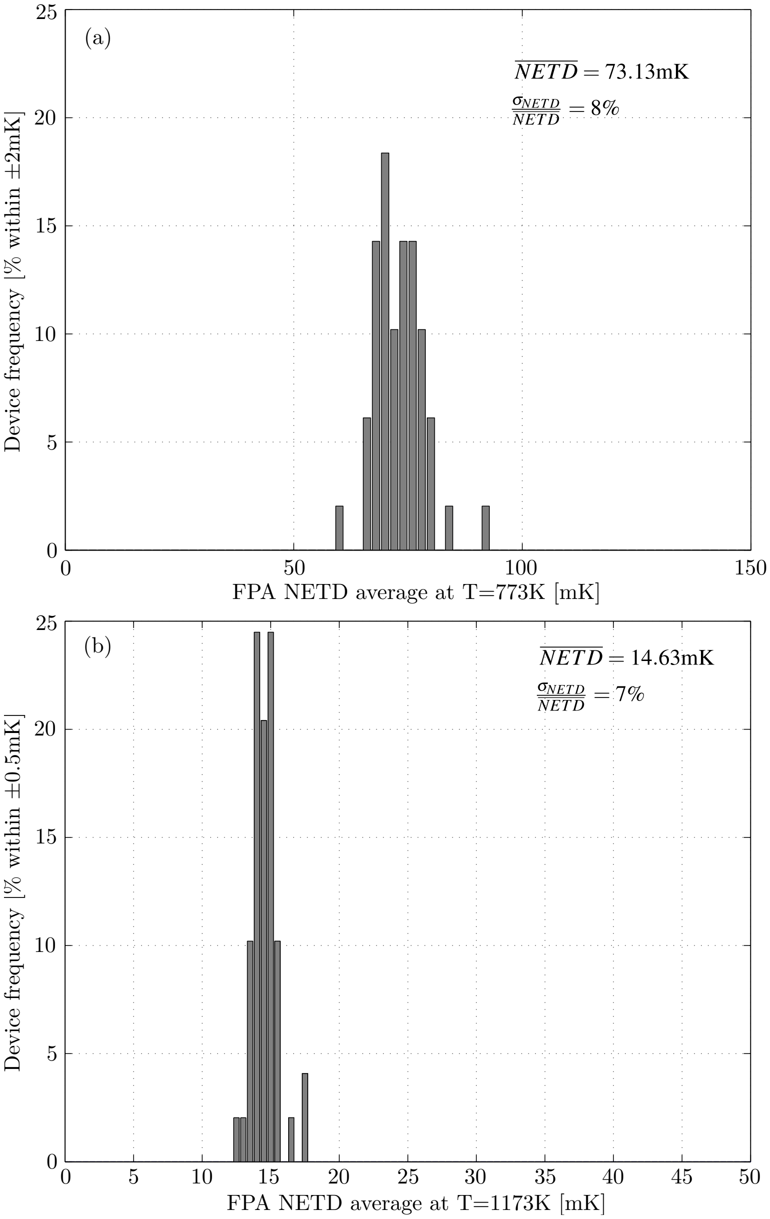


Figure 5.23 Experimental NETD statistics at 773K (a) and 1173K (b) blackbody temperatures. Noise measurements are averaged for each one of the 49 imagers of an entire wafer.

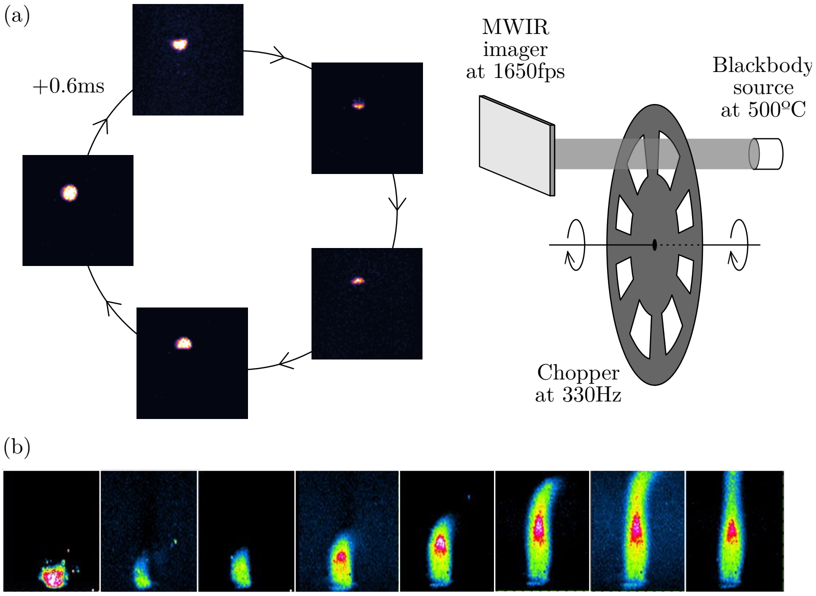
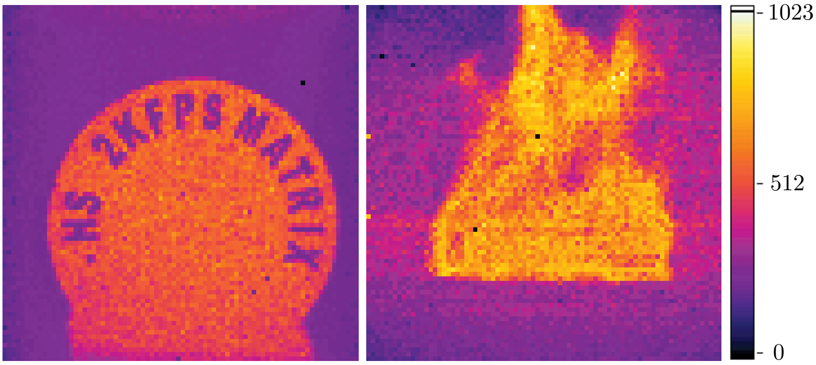

(a)
+0.6ms
MWIR
imager
at 1650fps
Blackbody
source
at 500ºC
Chopper
at 330Hz
(b)

Figure 5.24 Measured imager speed performance with mechanical chopper (a) and practical lighter switch-on sequence example (b).


HS 2KFPS MATRIX
1023
512
0

(a) (b)

Figure 5.25 Sample photograms of hot round plate (a) and flame (b) captured at 1650fps.

5.3 A 32×32 Frame-Free Compact-Pitch MWIR Imager

In order to experimentally characterize in 0.18μm 1P6M CMOS technology the DPS-C45 cell presented in Sec. 4.3, the specific IUT chip of Fig. 5.26 is proposed. Basically, the 32×32 DPS array under test is integrated together with a first version of the AER communications interface. This AER control includes the novel binary tree for row arbitration and the minimalist output encoder introduced in Sec. 3.6 to fit the column data events in a 16-bit bus format. The particularities of the proposed peripheral AER communication module are as follows:

- The priority allocation rule in case of collision is not fixed, random or simply toggled but toggled between last attended requests. In this way, a more fair row arbitration should be obtained in practice.
- The acknowledge feedback loop can be directly controlled by the external logic equipment. This test setup allows to investigate the effects of excessive arbitration delays on the event generation, and it can be also used as a back-pressure mechanism to limit the output bandwidth.

Output events are multiplexed in time to 4 readout cycles per row. The external AE receiver acquires this data from the IUT by generating four consecutive `acksel` pulses, and by synchronizing communication at the rising edge of this signal. Such signaling is input to a 2-bit ripple counter that controls the output multiplexing of column-wise events. The fair arbiter receives a single wired-OR `ackext` pulse to select which row to access in the FPA of DPS-C45 cells. Row requests are latched in the peripheric AER interface to keep stable logic levels at `outp` and `outn` buses throughout the four `acksel` periods of the readout cycle.

It is important to note that the test chip is not designed for the PbSe MWIR sensor post-processing like in the imager of Sec. 5.2, but to be attached by flip-chip to the 40 I/O bump-bonding pads of the ITP of Fig. 5.7. The latter is used to generate synthetic video sequences specifically programmed to validate the whole frame-free chip.

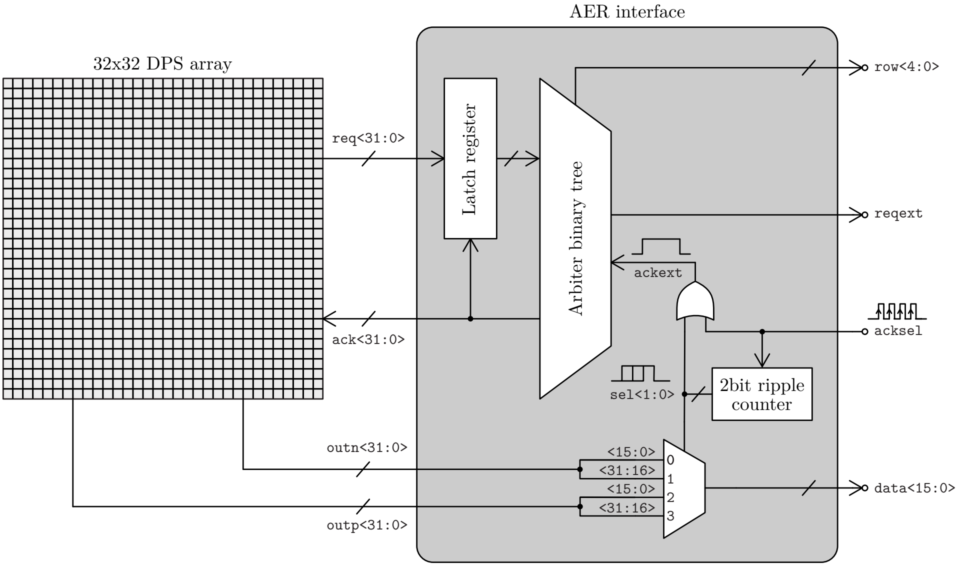

AER interface
32x32 DPS array
row<4:0>
req<31:0>
Latch register
Arbiter binary tree
reqext
ackext
acksel
ack<31:0>
sel<1:0>
2bit ripple counter
outn<31:0>
<15:0>
<31:16>
<15:0>
<31:16>
0
1
2
3
data<15:0>
outp<31:0>

Figure 5.26 Proposed architecture for the frame-free Compact-pitch MWIR imager.

5.3.1 Full-Custom ASIC Design

The complete test chip is shown in Fig. 5.27. As detailed in the same figure, all I/O pins of Table 5.3 were specifically positioned for the flip-chip packaging with the ITP of Sec. 5.1. Except the reference current input for the tuning of bus terminations, the resting I/O pads are in the digital domain only. The bounding box of the pixel CMOS core is about $45\mu m \times 45\mu m$ but, due to the target bump-bonding to the test platform, pitch was artificially expanded up to $50\mu m \times 50\mu m$.

Fig. 5.27(b) also zooms in to a micrograph of the DPS-C45 before packaging post-processing in its oxide apertures in order to interface the bumps. Fig. 5.27(c) depicts a close photograph of pixel bumping pads in the array, after Cu under bump metallization (UBM). The seeding profile detailed in the same subpicture was adjusted to a thick oxide height of $3\mu m$.

ITP and IUT chips were finally joined by the same bump-bonding procedure employed in Sec. 5.1.1. The resulting system-in-package (SIP) is depicted in Fig. 5.28, together with a near sight of the SnAg bumps [148] grown in the ITP at wafer level. After bump growing, the ITP dies were sawed from their containing 4-inch CNM25 wafers, and used as target device for the pick-and-place of frame-free IUT imagers.

Name	Type	Direction	Description
`vdda`	P	-	Pad supply voltage
`vddd`	P	-	Core supply voltage
`gnd`	P	-	Substrate ground
ipup	A	I	Pull-up bias current
`tune1`	D	I	PLL-tuning signal
`tune2`	D	I	VCO reset
`reset`	D	I	Analog integration reset
`reset_pll`	D	I	PLL reset
`reqext`	D	O	AER row request output
`ackext`	D	I	AER row acknowledge input
`row<0:4>`	D	O	Output bus of encoded row addresses
`out<0:15>`	D	O	Multiplexed output bus for pos. and neg. events

Table 5.3 Full list of the frame-free IUT pin-out for (P)ower, (A)nalog and (D)igital types and (I)nput and (O)utput directions. The physical location of each pin and the row/column origin is defined in Fig. 5.27.

5.3.2 Experimental Results

As explained in Sec. 4.3.2, the frame-free IUT could not be evaluated due the unrealistic MOSFET simulation models provided by the foundry. This issue was not reported until long after the reception of the die samples. The intermediate period allowed for the development of the experimental setup of Fig. 5.29; this illustration provides an overview of the extent that R&D activities had when devoted to the evaluation of the CMOS design proposals of Chapter 3.

The experimental setup of the frame-free IUT made use of the FPGA-based characterization system of Fig. 5.10, using in this case as well the AER monitoring module in order to record, encode, time-stamp and transmit AEs to the jAER software running in the computer. Synchronous FPGA implementations of AER systems offer good performances at relatively low

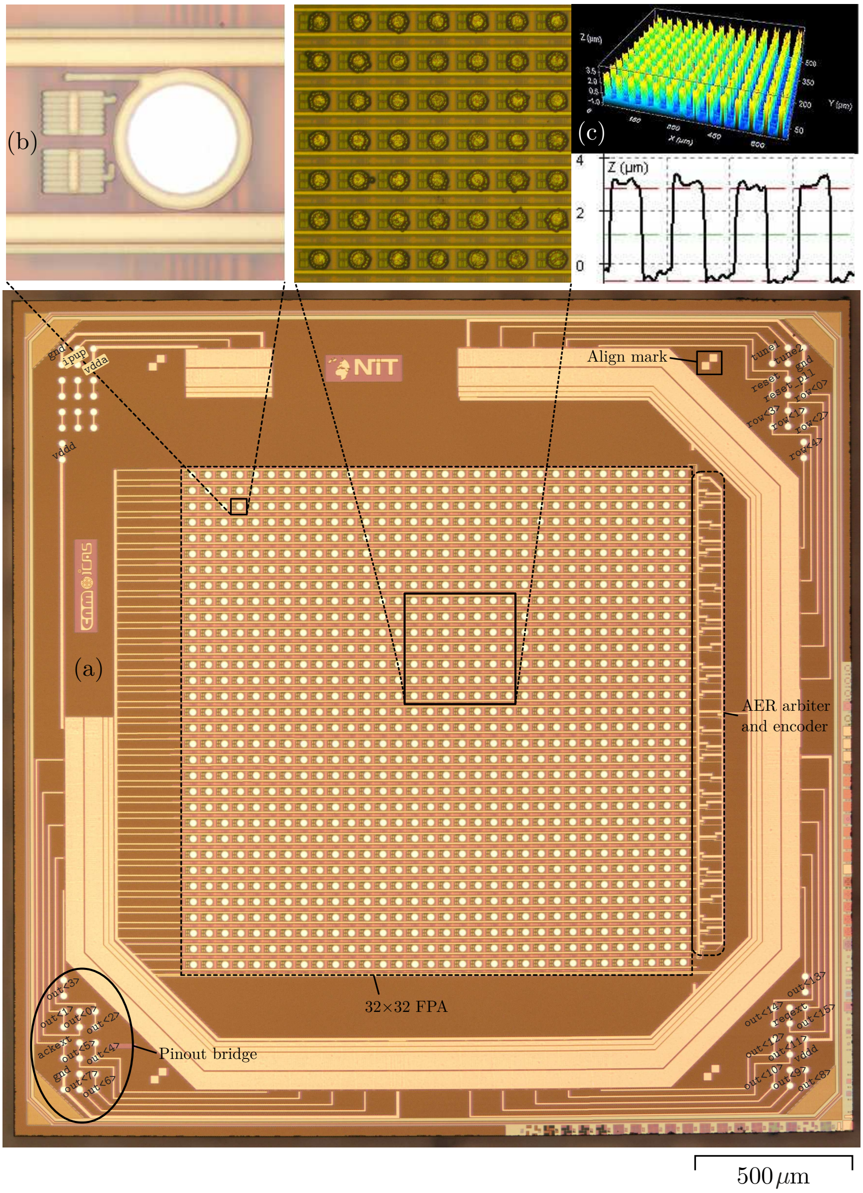

(b)
(c)
Z (µm)
Y (µm)
X (µm)
4
2
0
Z (µm)
gnd
ipup
vdda
vddd
NiT
(a)
Align mark
tune1
tune2
gnd
reset
reset_pll
row<0>
row<3>
row<1>
row<2>
row<4>
AER arbiter and encoder
32×32 FPA
out<3>
out<1>
out<0>
out<2>
ackext
out<5>
out<4>
gnd
out<7>
out<6>
Pinout bridge
out<13>
out<14>
reqext
out<15>
out<12>
out<11>
vddd
out<10>
out<9>
out<8>
500 µm

Figure 5.27 Micrograph of the 32×32 frame-free DPS-C45 IUT test chip tracing the location of main blocks and the I/O bumping pads that conform the pinout bridge (a). Pixel detail (b) and Cu-UBM zoom-in with height profile (c). Bounding box including scribe-line is about 2.6mm×2.6mm (6.8mm^2).

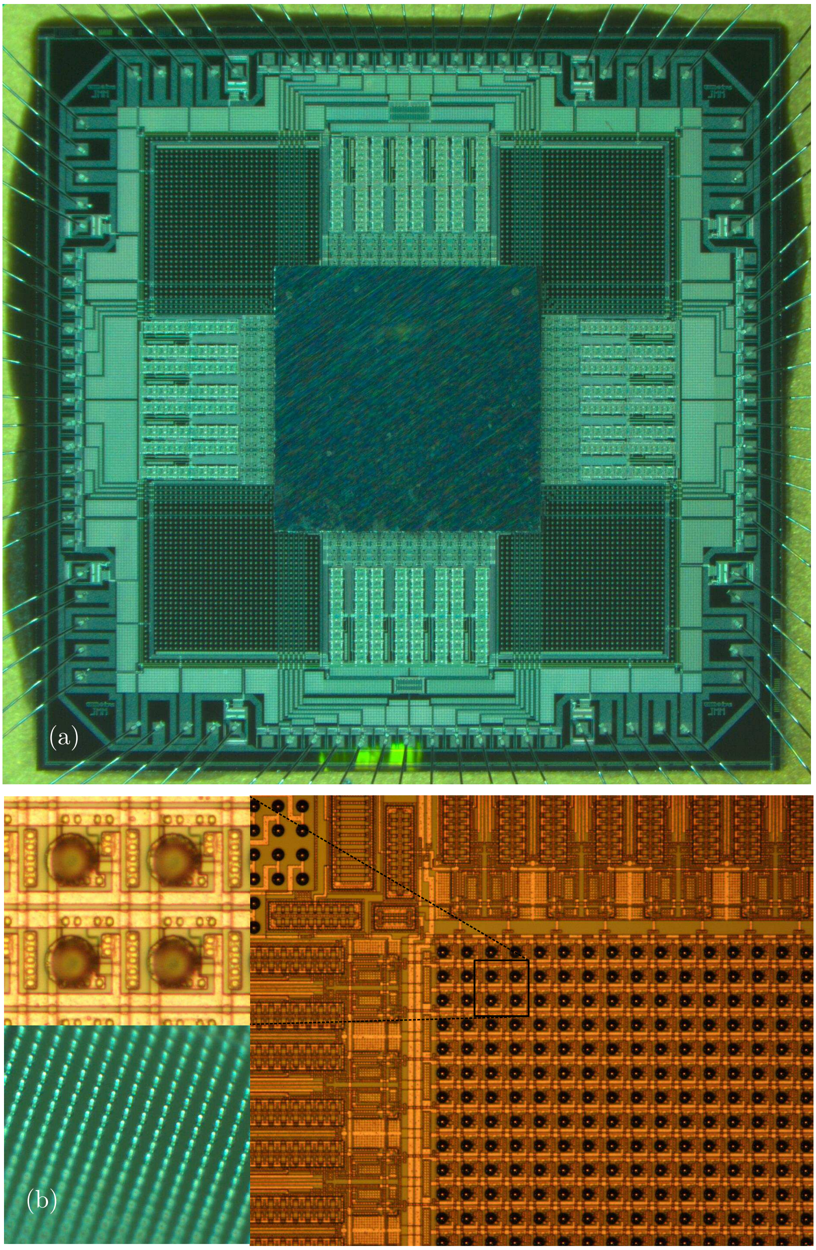


Figure 5.28 Micrograph of the complete test SIP integrated for the electrical validation of the frame-free Compact-pitch imager of Fig. 5.27 (a), and detail of the SnAg bumps grown in the ITP side at wafer level (b).

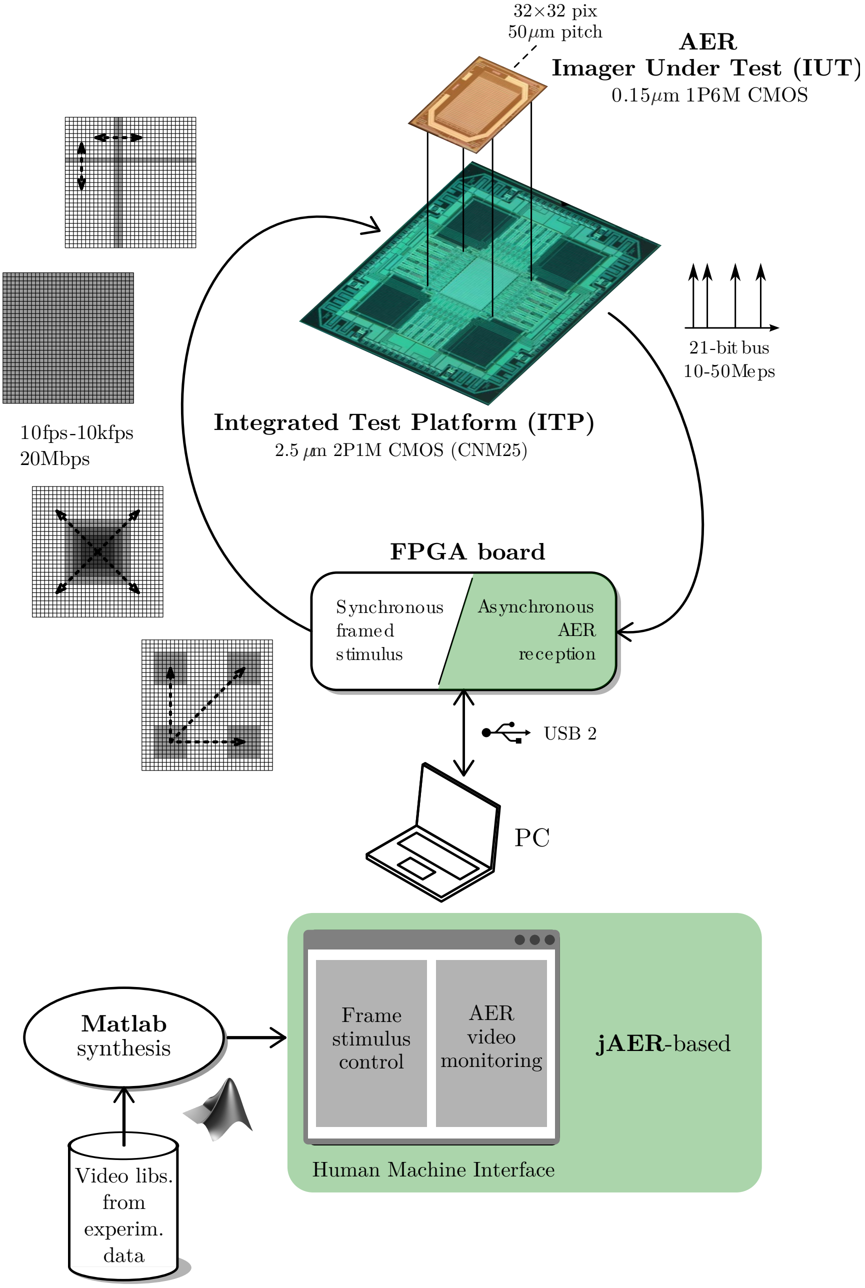

32×32 pix
50μm pitch
AER
Imager Under Test (IUT)
0.15μm 1P6M CMOS
21-bit bus
10-50Meps
10fps-10kfps
20Mbps
Integrated Test Platform (ITP)
2.5 μm 2P1M CMOS (CNM25)
FPGA board
Synchronous framed stimulus
Asynchronous AER reception
USB 2
PC
Matlab synthesis
Video libs. from experim. data
Frame stimulus control
AER video monitoring
jAER-based
Human Machine Interface

Figure 5.29 General scheme of the experimental setup defined for the electrical validation of the frame-free Compact-pitch imager architecture of Chapter 3.

development times when compared to their asynchronous analogues [149]. The embedded ITP stimulus programmer was now envisioned to transmit simple and real-alike video sequences to the integrated sensor emulator. Such sequences were generated in Matlab from a predefined library of video samples by fitting (5.1) into a 5th-degree polynomial in x and y, and running gradient descent into the equivalent system of equations of the full image to convert.

Even though the electrical characterization of these designs was not finally possible, the copious work invested on this research line provides significant contributions towards the integration, operation and test of forthcoming frame-free implementations of the industrial MWIR camera in another target CMOS technology. Such contributions are discussed in extent in Chapter 6.

5.4 Comparison with State-of-the-Art IR Imagers

Table 5.4 summarizes the performance of the first generation of commercial MWIR imagers for high-speed uncooled applications originated from this thesis. The parameters shown in this chart are based on the experimental results of Sec. 5.2.2 and are compared to the latest IR vision sensor solutions of Table 1.4.

When evaluated at their corresponding spectral range of operation, the VPD PbSe frame-based Smart imager stands out from other contemporary solutions for exhibiting the highest frame rate and lowest NETD$\times\tau_{\mathrm{img}}$ (i.e. 15 times higher and more than 5 times lower than state-of-the-art high-end quantum devices, respectively). Even implementing the full A/D conversion and dual FPN compensation inside each active pixel, the implementation of Sec. 5.2 keeps static power consumption below 1 μW/pix. The compact pitch reported in [88] and [83, 84] is achieved at the cost of having analog pixel output, which may be prone to inter-pixel crosstalk and to extra FPN added at column or row levels, compared to all-digital I/O active pixels. Since the area of the DPS-S130 circuits proposed here is dominated by the digital block, pixel pitch can be downscaled by upgrading the target CMOS technology. Thanks to the level of technological maturity achieved throughout this work, ongoing implementations of this architecture pack DPS pitch below 100μm and pursue FPA resolutions of 256×256 pixels. The 45μm pitch resolved in the latest DPS-C45 prototype of Fig. 4.21 crosses a promising milestone in this direction, while opening the door to extend bandwidth up to the limits imposed by the PbSe PC detection technology itself.

To the best of my knowledge, the industrial MWIR imaging device developed along the research activities of this thesis is the only uncooled IR imager (i) acquiring at kfps and (ii) supplying independent digital offset and gain tuning capabilities for FPN cancellation and DR adjustment at every pixel of the FPA. Thanks its fully digital readout and programmability at pixel level, the device can be incorporated in minimalist cameras with very few components and reduced dimensions. It overcomes the limited sensitivity and poor spectral discrimination of microbolometer-based solutions, avoids complex hybrid packaging procedures and bulky cryocooling mechanisms, and offers an affordable consumer product for MWIR vision, an expanding market sector with few competitors and promising applications.

	This work	Posch et al. [90]	Lv et al. [88]	Gunapala et al. [85, 86]	Peirezat et al. [81, 82]	Ilan et al. [83, 84]	Units
Pixel array	80×80	64×64	640×512	1024×1024	320×256	1920×1536	pixels
Pixel pitch	135	50	25	30	30	10	μm
Cryocooling-free	Yes	Yes	Yes	No	No	No	-
Packaging tech.	Monolithic	Monolithic	Monolithic	Hybrid	Hybrid	Hybrid	-
CMOS tech.	0.35μm 2P4M	0.35μm 2P4M	0.5μm 2P3M	0.5μm 2P3M	0.18μm 1P6M	0.18μm	-
IR tech.	VPD PbSe	a-Si μbolom.	VOx μbolom.	QWIP	HgCdTe PV	InSb PV	-
IR wavelth.	MWIR	LWIR	LWIR	M/LWIR	LWIR	MWIR	-
Fill factor	68	69	75	50	∼100	∼100	%
Spectral range	1.7 to 4.3	8 to 15	8 to 14	4.4 to 5.1; 7.8 to 8.8	7.7 to 9.5	1 to 5.4	μm
Peak det. wavelth.	3.6	-	-	4.6; 8.4	N.A.	4.7	μm
Peak detectivity	1.9×10^9	$\sim\times10^8$	$\sim\times10^9$	4×10^{11}; 1×10^{11}	$\sim\times10^{10}$	$\sim\times10^{11}$	cm$\sqrt{\text{Hz}}$/W
Readout technique	CTIA	CTIA	CTIA	DI	CTIA	DI	-
Pixel output	Digital 10b	Digital AER	Analog	Analog	Digital 11b	Analog	-
ROIC output	Digital 10b	Digital AER	Analog/Digital	Analog	Digital 16b	Digital 13b	-
ADC	In-pixel PDM	In-pixel PDM	Col-wise PWM	None	In-pixel PDM Col-wise flash	Col-wise PWM	
In-pixel FPN cancel.	Offset & gain	None	Offset only	None	None	None	-
Max. frame rate	2000	30	60 (analog)	30	320	120	fps
NETD	73 @773K	>1000 @300K	45 @300K	27; 40 @300K	25 @300K	25 @300K	mK
NETD$\times\tau_{\text{img}}$	18	N.A.	375	450; 665	40	105	mK×ms
Supply voltage	3.3	3.3	5	5	1.8	1.8	V
Static power cons.	<1	<1	<1	<1	<1	<1	μW/pix

Table 5.4 Performance comparison between this work and state-of-the-art IR vision sensors.

Conclusions | 6

6.1 Contributions

As a result of the research activities presented in this PhD thesis, the initial working hypothesis, firstly stated in Sec. 1.6.3, have been successively tested and confirmed:

> *"By the use of novel low-power mixed-signal VLSI design techniques at system and circuit levels, high-speed uncooled MWIR imagers can be monolithically integrated and validated in standard low-cost CMOS technologies, fulfilling all operational requirements of the VPD PbSe detector in terms of connectivity, reliability, functionality and scalability for their use in industrial applications."*

In order to achieve the above milestone in the field of analog and mixed-signal IC design, "Low-Power CMOS Digital-Pixel Imagers for High-Speed Uncooled PbSe IR Applications" builds on the top-down methodology described in Sec. 1.6.5 to drive forward contemporary IR imaging knowledge in three concrete research areas:

1. The investigation of a new frame-based “Smart” MWIR imager architecture based on self-biased DPS circuit topologies with in-pixel frame memory and fully-programmable gain and offset FPN correction.

2. The exploration of a novel frame-free “Compact”-pitch MWIR vision sensor architecture building from a memoryless DPS design with self-biasing and configurable temporal-difference dark-current cancellation, combined with AER communication protocols inside the focal plane.

3. The study of innovative integrated test platforms and characterization protocols to free electrical characterization in initial CMOS ROIC prototypes from the time and money-costing deposition of PbSe MWIR detectors at wafer level.

Contributions to every one of the three lines include:

Frame-based “Smart” MWIR imaging:

- A highly-modular, in-pixel, reconfigurable ripple-counter-based I/O interface for the fully-digital operation of vision sensors.

- An in-pixel pF-range input capacitance compensation circuit to avoid signal leakages through the low output impedance of the PbSe detector.

- Three high-resolution in-pixel offset cancellation topologies: self-calibrated, SC-DAC programmed and SI-copier-DAC tuned.

- A high-resolution individual DPS gain tuning scheme that makes reuse of the SC-DAC and digital interface implemented in each pixel.

- A novel 3-switch-reset class-AB CTIA with CDS to ensure fast reset times under low-power operation.

- A temperature-compensated in-pixel nA-range bias generation circuit with low dependence to both technology mismatching and process variations.

- A 100μm self-calibrated DPS version of the frame-based architecture (DPS-S100) integrated in a standard 0.35μm 2P4M CMOS technology, and experimental results at both single and mini-FPA levels.

- Two 200μm and 135μm versions of the frame-based DPS (DPS-S200 and DPS-S130) with external SC-DAC offset tuning integrated in a standard 0.35μm 2P4M CMOS technology, and experimental results at both single and mini-FPA levels.

- A kfps-range sub-μW/pix uncooled-PbSe commercial MWIR imager with 10-bit DR Adjustment and FPN correction in both 32×32 and 80×80 FPA formats, monolithically integrated in a standard 0.35μm 2P4M CMOS technology and electrooptically validated.

- The best NETD$\times\tau_{\text{img}}$ FOM published for MWIR imaging without any need of external cooling nor hybrid packaging procedures.

Frame-free “Compact”-pitch MWIR imaging:

- A built-in log-domain temporal difference (TD) circuit to cancel the high mean-and-variance dark current signal generated by the PbSe detector, and to provide adaptive self-biasing to this component with effective signal compression so as to minimize communication-channel loads.

- A digital PLL-based and PVT-compensated scheme for the digital tuning of the high-pass corner frequency set at the TD stage.

- A new family of in-pixel lossless-reset integrate-and-fire ADCs, which uses a novel switched-capacitor technique to improve its linearity, reduce power consumption and allow low-voltage operation for the switching devices at high frame rates.

- A CMOS circuit example of the previous pulse density modulation (PDM) strategy with built-in CDS, no low output-impedance requirements and over-integration protection.

- An in-pixel address event representation (AER) interface with internal request holding and dynamic bus driving to ensure proper event transmission under low-power operation.

- A novel arbiter tree with glitch-insensitive distributed encoding and fair arbitration to grant visual representation of all busy regions of the FPA.
- A 45μm DPS implementation (DPS-C45) of previous circuits in a standard 0.15μm 1P6M CMOS technology.
- A 32×32 frame-free compact-pitch MWIR imager prototype with PLL-tuned temporal difference (TD) and fair arbitration integrated in a standard 0.15μm 1P6M CMOS technology.

Integrated test platforms and characterization protocols:

- Custom-built integrated experiments with isolated pixels, tiny FPAs and internal emulation of the PbSe detector for the electrical characterization of DPS-S100, DPS-S130 and DPS-S200 cells.
- A complete test protocol and Labview-based experimental setup for the electrical characterization of ADC performance, offset memory retention, individual programmability and crosstalk effects in the aforementioned devices.
- A 10kfps 32×32 integrated test platform (ITP) for the digital programming of video contents and motion patterns at pixel level, in order to emulate the PbSe detector by flip-chip packaging in preliminary imager prototypes.
- A complete test protocol and FPGA-based experimental setup with automatic video synthesis, individual pixel stimulation and AER monitoring, for the electrical characterization of TD tuning, crosstalk, ADC response, bandwidth, arbitration performance and delay-insensitiveness of the frame-free Compact-pitch imager developed in this work.

The specific achievements of this thesis have derived in the following publications and patents:

Journals:

- J.M. Margarit, G. Vergara, V. Villamayor, R. Gutiérrez-Álvarez, C. Fernández-Montojo, L. Terés and F. Serra-Graells, “A 2 kfps Sub-μW/pix Uncooled-Pbse Digital Imager with 10 bit DR Adjustment and FPN Correction for High-Speed and Low-Cost MWIR Applications,” in *IEEE Journal of Solid-State Circuits*, vol. 50, no. 10, pp. 2081–2084, October 2015.

- J.M. Margarit, L. Terés and F. Serra-Graells, “A Sub-μW Fully Tunable CMOS DPS for Uncooled Infrared Fast Imaging,” in *IEEE Transactions on Circuits and Systems-I*, vol. 56, no. 5, pp. 987–996, May 2009. **Invited paper**.

Conferences:

- J.M. Margarit, L. Terés, E. Cabruja and F. Serra-Graells, “A 10kfps 32×32 Integrated Test Platform for Electrical Characterization of Imagers,” in *Proceedings of the IEEE International Symposium on Circuits and Systems*, pp. 53–56, Melbourne, Australia, June 2014.

- J.M. Margarit, M. Dei, L. Terés and F. Serra-Graells, “A Self-Biased PLL-Tuned AER Pixel for High-Speed Infrared Imagers,” in *Proceedings of the IEEE International Symposium on Circuits and Systems*, pp. 1812-1815, Rio de Janeiro, Brazil, May 2011.

- G. Vergara, R. Gutiérrez, L. J. Gómez, V. Villamayor, M. Álvarez, M. C. Torquemada, M. T. Rodrigo, M. Verdú, F. J. Sánchez, R. M. Almazán, J. Plaza del Olmo, P. Rodríguez, I. Catalán, D. Fernández, A. Heras, F. Serra-Graells, J. M. Margarit, L. Terés, G. de Arcas, M. Ruiz, J. M. López, “Fast uncooled low density FPA of VPD PbSe,” in *Proceedings of SPIE*, vol. 7298, Bellingham, USA, 2009.

- J. M. Margarit, L. Terés and F. Serra-Graells, “A Sub-1μW Fully Programmable CMOS DPS for Uncooled Infrared Fast Imaging,” in *Proceedings of the XXIII Conference on Design of Circuits and Integrated Systems*, Grenoble, France, November 2008.

- J. M. Margarit, L. Terés and F. Serra-Graells, "A Sub-μW Fully Programmable CMOS DPS for Uncooled Infrared Fast Imaging," in *Proceedings of the IEEE International Symposium on Circuits and Systems*, pp. 1424–1427, Seattle, USA, May 2008. **2008 Best Paper Award by the Sensory Systems Technical Committee of the IEEE Circuits and Systems Society**.

- J. M. Margarit, J. Sabadell, L. Terés and F. Serra-Graells, "A Novel DPS Integrator for Fast CMOS Imagers," in *Proceedings of the IEEE International Symposium on Circuits and Systems*, pp. 1632–1635, Seattle, USA, May 2008.

- F. Serra-Graells, J. M. Margarit and L. Terés, "A Self-Biased and FPN-Compensated Digital APS for Hybrid CMOS Imagers," in *Proceedings of the IEEE International Symposium on Circuits and Systems*, pp. 2850-2853, New Orleans, USA, May 2007.

- G. Vergara, L. J. Gómez, V. Villamayor, M. Álvarez, M. C. Torquemada, M. T. Rodrigo, M. Verdú, F. J. Sánchez, R. M. Almazán, J. Plaza, P. Rodriguez, I. Catalán, R. Gutiérrez, M. T. Montojo, F. Serra-Graells, J. M. Margarit and L. Terés, "Monolithic Uncooled IR Detectors of Polycrystalline PbSe: a Real Alternative," in *Proceedings of SPIE*, vol. 6542, Orlando, USA, April 2007.

Patents:

- F. Serra-Graells, J.M. Margarit, M. Dei, L. Terés, M.T. Montojo, G. Vergara, R. Linares, R. Gutiérrez, inventors; Consejo Superior de Investigaciones Científicas (CSIC), New Infrared Technologies, S.L., asignee. "Integrated Circuit for the Digital Tuning of Temporal Contrast in Image Sensors," World Patent WO 2 012 152 978, issued date November 15, 2012.

- F. Serra-Graells, J.M. Margarit and L. Terés, inventors; Consejo Superior de Investigaciones Científicas (CSIC), asignee. "Digital Read-Out Integrated Circuit for the Digital Reading of High-Speed Image Sensors," World Patent WO 2 009 138 545, issued date August 18, 2010.

In conclusion, these results have led to the first high-speed uncooled frame-based IR quantum imager monolithically fabricated in a standard VLSI CMOS technology, and have given rise to the Tachyon series [1], a new line of commercial IR cameras for industrial imaging applications. The frame-free architectures investigated in this work represent a firm step forward to push further pixel pitch and system bandwidth up to the limits imposed by the evolving PbSe detector in future generations of the device.

6.2 Discussion and Future Work

Reached this point, it is good practice to take some perspective and look both back and forward in time. It has been a long journey since I first visited the IMB-CNM(CSIC) facilities in Bellaterra: "We have a new industrial proposal in our hands and we are seeking an aspiring researcher to make it come true", the enthusiasm that Lluís and Paco had in their eyes and words was contagious. I had just finished my Image Processing course at the UPC Telecom School in Barcelona, had been working for two years with the LCD-TV Eng. Dpt. at the Sony Bcn Tech center and was hungry for a new challenge. I found it: I'll develop a new imager from scratch! Could not say no to this. And so it goes... The lessons learned along the venture have been numerous and variate; professional and personal. Let me keep the personal stuff for a more private occasion and center here on the second, summarized in three main take-homes:

Take the big picture: A PhD thesis needs time to materialize. You do not want to waste it in an undefined strategy. Think about the what, the why, and the how, document yourself from the very beginning, and leave plenty of time and freedom for ideas to come. Research feeds on proper planning, and this is specially true when applied to inter-sectoral collaborations like this work. I learned it quickly from my supervisors. No pixel would have been operative if it had not been for the previous definition of specific research milestones along the design and validation of the ROIC. Developing imager architectures required of successive meeting rounds to define the specs of each aimed IR device. This was not always easy in the parallel research context of this dissertation.

Keep it simple, keep it clear: Simplicity is key in any ambitious design. An efficient project flow avoids unnecessary burdens, and facilitates progress by using hierarchical procedures, a clear design framework, and periodical status updates. Modularizing imager design at the DPS level was a good idea: squeezing every block in the active pixels saved area and power; distributing imager circuitry inside each cell increased functionality and kept system complexity bounded from the first stages of the research. And having close contact with NIT S.L. accelerated debugging and kept development driven to real-world requirements.

Lead your simulations: This may sound obvious, but I have seen it many times go the other way around. Blind automatic design goes nowhere. The limitations that current simulators still have to estimate and calculate the effects of parasitics and variances in large microelectronic systems make researcher's abilities to foresee critical points a must. In the case of the development of limited-pitch pixel sensors, this extends to the prediction of area requirements and modularity of each building block; noise, mismatch, stability and corner effects; and the forthcoming complexity of the final matricial system. The accuracy and ease-of-use of EKV subthreshold models helped a good deal in this task, but the previous experience of my colleagues and the many hours spent sharpening "my intuition" under Cadence were crucial. Once identified the major dependencies of your design, let machines do the hard calculations and the repetitive work for you.

The research activities presented in this work lay foundation of what I believe is going to be a bright future in the area of PbSe-based MWIR vision. Short term activities include:

- The exploration of pitch-reduction strategies for frame-based Smart imagers, by the use of more compact CMOS technologies, the PRMLS-LFSR of Sec. 2.2.1 and the SI-copier DAC strategy of Sec. 2.3.2. As PbSe PC technology progresses in pitch and yield, gain corrections can be gradually overlooked in favor of a minimization of the final dimensions of the DPS-S. In this scenario, the SC-DAC of Fig. 2.12(a) can be substituted by the CMOS topology of Fig. 2.12(b) so as to save extra area in the design.

- The investigation of parallel bus-access alternatives to speedup readout and reduce heating during communication in these same frame-based systems.

These ideas have materialized already in a 128×128 pixel imager design in a 0.18μm 1P6M CMOS technology, and are currently pending to complete electrical validation.

In the longer term, innovation tasks will be focused on the frame-free architecture of Chapter 3, by gaining insight in the following topics:

- The integration of the frame-free imager of Fig. 5.27 in another 0.18μm 1P6M CMOS technology so as to detect and refine possible weak points in view of the fabrication of the first commercial AER-based MWIR imaging prototype.
- The adaptation of the FPGA-based setup of fig. 5.29 to the new frame-free system and its validation in direct interaction with the previous ROIC.
- The exploration of novel schemes at system-level like the configuration of different ROIs in the FPA and the implementation of mixed framed and event-based architectures by employment of distributed digital filtering (i.e. in-chip AER communication) in the ROIC.
- The study of new dark current cancellation methods based on its modulation and filtering in the frequency domain in order to minimize noise injection and power consumption in the first stage of the DPS.

The list is extensive and could give birth to new doctoral pursuits and industrial projects.

References

[1] New Infrared Technologies S.L., “The New Tachyon Series FPA ROIC from New Infrared Technologies.” http://www.niteurope.com/en/tachyon-series-fpa-roic-2g.html, April 2013.

[2] G. Vergara, R. Almazán, L. Gómez, M. Verdu, P. Rodríguez, and M. T. Montojo, “Method of Treating Polycristalline Lead Selenide Infrared Detectors,” 2007.

[3] Aristotle, “Aristotle: Problems, Volume I: Books 1-19,” in *Book 15*, Loeb Classical Library, pp. 451–476, Harvard University Press, 2011.

[4] G. Batchen, “Images Formed by Means of a Camera Obscura,” in *Burning with Desire: The Conception of Photography*, ch. Images formed by means of a camera obscura, pp. 78–85, The MIT Press, 1999.

[5] J. N. Niépce, “Classic Essays on Photography,” in *Memoire on the Heliograph* (A. Trachtenberg, ed.), ch. Memoire on the Heliograph, pp. 5–10, Leete’S Island Books, 1980.

[6] L. J. M. Daguerre, “Daguerreotype,” in *Classic Essays on Photography* (A. Trachtenberg, ed.), ch. Daguerreotype, pp. 11–14, Leete’S Island Books, 1980.

[7] E. R. Fossum, “Active Pixel Sensors: Are CCD’s Dinosaurs?,” in *Proceedings of SPIE*, vol. 1900, pp. 2–14, SPIE, 1993.

[8] G. Moore, “Cramming More Components onto Integrated Circuits,” *Electronics*, vol. 38, no. 8, pp. 114–117, 1965.

[9] C. Ibarra-Castanedo, “The Infrared Bands in the Infrared Spectrumé.” Wikimedia Commons media file repository, 2007.

[10] L. Cheng and G. Y. Tian, “Surface Crack Detection for Carbon Fiber Reinforced Plastic (CFRP) Materials Using Pulsed Eddy Current Thermography,” *IEEE Sensors Journal*, vol. 11, no. 12, pp. 3261–3268, 2011.

[11] J. H. Lim, O. Tsimhoni, and Y. Liu, “Investigation of Driver Performance With Night Vision and Pedestrian Detection Systems - Part I: Empirical Study on Visual Clutter and Glance Behavior,” *IEEE Transactions on Intelligent Transportation Systems*, vol. 11, no. 3, pp. 670–677, 2010.

[12] F. Lamberti, A. Sanna, and G. Paravati, “Improving Robustness of Infrared Target Tracking Algorithms Based on Template Matching,” *IEEE Transactions on Aerospace and Electronic Systems*, vol. 47, no. 2, pp. 1467–1480, 2011.

[13] N. Jaiswal and C. Kishtawal, “Objective Detection of Center of Tropical Cyclone in Remotely Sensed Infrared Images,” *IEEE Journal of Selected Topics in Applied Earth Observations and Remote Sensing*, vol. 6, no. 2, pp. 1031–1035, 2013.

[14] K. Yamamoto, K. Murakami, Y. Aoike, K. Fukui, K. Mizuno, and M. Tani, “Study on Weak Hydrogen Bond by Terahertz and Mid-IR Spectroscopy,” in *IEEE International Conference on Infrared, Millimeter, and Terahertz Waves (IRMMW-THz)*, pp. 1–2, 2013.

[15] "Infrared and Thermal Imaging Systems Market by Technology, Subsector, Application, & by Geography - Forecasts & Analysis 2014–2019," tech. rep., Research and Markets Ltd., 2014.

[16] "The MATRIX 1024 SERIES: Applications of High-Speed Uncooled MWIR Imaging Sensors," tech. rep., New Infrared Technologies S.L., 2011.

[17] L. Kozlowski and W. Kosonocky, *Handbook of Optics.* McGraw-Hill, Inc., 1995.

[18] A. Rogalski, *Infrared Detectors.* CRC Press, 2011.

[19] C. Hsieh, C. Wu, F. Jih, and T. Sun, "Focal-Plane-Arrays and CMOS Readout Techniques of Infrared Imaging Systems," *IEEE Transactions on Circuits and Systems for Video Technology*, vol. 7, no. 4, pp. 594–605, 1997.

[20] A. Rogalski, "Progress in Focal Plane Array Technologies," *Progress in Quantum Electronics*, vol. 36, pp. 342–473, 2012.

[21] M. A. Kinch, *Fundamentals of Infrared Detector Materials.* SPIE Press, 2007.

[22] "Selection Guide for PbS & PbSe Infrared Detectors," tech. rep., Laser Components GmbH, 2015.

[23] J. Diezhandino, G. Vergara, G. Pérez, I. Génova, M. T. Rodrigo, F. J. Sánchez, M. C. Torquemada, V. Villamayor, J. Plaza, I. Catalán, R. Almazán, M. Verdú, P. Rodríguez, L. J. Gómez, and M. T. Montojo, "Monolithic Integration of Spectrally Selective Uncooled Lead Selenide Detectors for Low Cost Applications," *Applied Physics Letters*, vol. 83, no. 14, pp. 2751–2753, 2003.

[24] Y.-C. Shih and C.-Y. Wu, "A New CMOS Pixel Structure for Low-Dark-Current and Large-Array-Size Still Imager Applications," *IEEE Transactions on Circuits and Systems-I*, vol. 51, no. 11, pp. 2204–2214, 2004.

[25] A. Fish, S. Hamami, and O. Yadid-Pecht, “CMOS Image Sensors with Self-Powered Generation Capability,” *IEEE Transactions on Circuits and Systems-II*, vol. 53, no. 11, pp. 1210–1214, 2006.

[26] A. Olyaei and R. Genov, “Focal-Plane Spatially Oversampling CMOS Image Compression Sensor,” *IEEE Transactions on Circuits and Systems-I*, vol. 54, no. 1, pp. 26–34, 2007.

[27] M. Tänzer and A. Graupner and R. Schüffny, “Design and Evaluation of Current-Mode Image Sensors in CMOS-Technology,” *IEEE Transactions on Circuits and Systems-II*, vol. 51, no. 10, pp. 566–570, 2004.

[28] D. J. Banks, P. Degenaar, and C. Tomazou, “Distributed Current-Mode Image Processing Filters,” *IET Electronics Letters*, vol. 41, no. 22, pp. 1201–1202, 2005.

[29] Y. L. Wong and P. A. Abshire, “A 144×144 Current-Mode Image Sensor With Self-Adapting Mismatch Reduction,” *IEEE Transactions on Circuits and Systems-I*, vol. 54, no. 8, pp. 1687–1697, 2007.

[30] R. M. Philipp, D. Orr, V. Gruev, J. V. der Spiegel, and R. Etienne-Cummings, “Linear Current-Mode Active Pixel Sensor,” *IEEE Journal of Solid State Circuits*, vol. 42, no. 11, pp. 2482–2491, 2007.

[31] A. M. Fowler, R. G. Probst, J. P. Britt, R. R. Joyce, and F. C. Gillett, “Evaluation of an Indium Antimonide Hybrid Focal Plane Array for Ground-Based Infrared Astronomy,” vol. 26, pp. 232–240, 1987.

[32] N. Lum, J. Asbrock, R. White, R. Kelchner, L. Lum, L. Pham, C. McCreight, M. McKelvey, R. J. McMurray, W. Forrest, and J. Garnett, “Low-noise, low-temperature, 256×256 Si:As IBC staring FPA,” in *Proceedings of SPIE*, vol. 1946, 1993.

[33] K. M. Merrill, A. M. Fowler, W. Ball, A. Hendon, F. Vbra, and C. McCreight, “Orion II: The Second-Generation Readout Multiplexer for Largest Infrared Hybrid Focal Plane,” in *Proceeedings of SPIE*, vol. 5167, pp. 186–193, 2004.

[34] P. J. Love, A. W. Hoffman, D. L. Gulbransen, K. J. Ando, M. P. Murray, and N. J. Therrien, "Large-Format 0.85 and 2.5 μm HgCdTe Detector Arrays for Low-Background Applications," in *Proceedings of SPIE*, vol. 5167, pp. 134–143, 2004.

[35] P. J. Love, E. J. Beuville, E. Corrales, J. J. Drab, A. W. Hoffman, R. S. Holcombe, and N. A. Lum, "1024 x 1024 Si: As IBC Detector Arrays for MID-IR Astronomy," in *Proceedings of SPIE*, vol. 6276, 2006.

[36] N. Bluzer and R. Stehlik, "Buffered Direct Injection of Photocurrents into Charge Coupled Devices," *IEEE Transactions on Electron Devices*, vol. 25, no. 2, pp. 160–166, 1978.

[37] J. T. Longo, D. T. Cheung, A. M. Andrewheung, A. M. Andrews, C. C. Wang, and J. M. Tracy, "Infrared Focal Planes in Intrinsic Semiconductors," *IEEE Transactions on Electron Devices*, vol. 25, no. 2, pp. 213–232, 1978.

[38] K. Chow, J. P. Rode, D. H. Seib, and J. D. Blackwell, "Hybrid Infrared Focal-Plane Arrays," *IEEE Transactions on Electron Devices*, vol. 29, no. 1, pp. 3–13, 1982.

[39] "Large-Format Readout Integrated Circuits," tech. rep., FLIR Systems, Inc., 2008.

[40] L. J. Kozlowski, W. V. McLevige, S. A. Cabelli, A. H. B. Vanberwyck, D. E. Cooper, E. R. Blazejewski, K. Vural, and W. E. Tennant, "Attainment of High Sensitivity at Elevated Operating Temperatures with Staring Hybrid HgCdTe-on-Sapphire Focal Plane Arrays," *SPIE Optical Engineering*, vol. 33, no. 3, pp. 704–715, 1994.

[41] P. Norton, "Infrared Image Sensors," *SPIE Optical Engineering*, vol. 30, no. 11, pp. 1649–1660, 1991.

[42] C. Staller, L. Ramiirez, C. Niblack, M. Blessinger, and W. Kleiinhans, "A Radiation Hard, Low Background Multiplexer Design for Spacecraft Imager Applications," in *Proceedings of SPIE*, 1992.

[43] L. Kozlowski, S. Cabelli, R. Kezer, and W. Kleinhans, "10×132 CMOS/CCD Readout with 25μm Pitch and On-Chip Signal Processing Including CDS and TDI," in *Proceedings of the SPIE Conference on Infrared Readout Electronics*, vol. 1684, pp. 175–181, 1992.

[44] M. D. Enriquez, M. A. Blessinger, J. V. Groppe, T. M. Sudol, J. Battaglia, J. Passe, M. Stern, and B. M. Onat, "Performance of High Resolution Visible-InGaAs Imager for Day/Night Vision," in *Proceedings of SPIE*, vol. 6940, 2008.

[45] C. Y. Wu, C. C. Hsieh, F. W. Jih, T. P. Sun, and S. J. Yang, "A New Share-Buffered Direct-Injection Readout Structure for Infrared Detector," in *Proceedings of SPIE*, vol. 2269, pp. 718–726, 1994.

[46] C. C. Hsieh, C. Y. Wu, F. W. Jih, T. P. Sun, and S. J. Yang, "A New Switch-Current Integration Readout Structure for Infrared Focal Plane Array," in *Proceedings of SPIE*, vol. 2269, pp. 718–726, 1996.

[47] C. C. Hsieh, C. Y. Wu, F. W. Jih, T. P. Sun, and H. Chang, "A New CMOS Readout Circuit Design for the IR FPA with Adaptive Gain Control and Current-Mode Background Suppression," in *Proceedings of the International Symposium on Circuits and Systems*, vol. 1, pp. 137–140, 1996.

[48] D. Das and S. Collins, "Fixed-Pattern-Noise Correction for an Integrating Wide-Dynamic-Range CMOS Image Sensor," *IEEE Transactions on Electron Devices*, vol. 60, no. 1, pp. 314–319, 2013.

[49] M. Perenzoni, N. Massari, D. Stoppa, L. Pancheri, M. Malfatti, and L. Gonzo, "A 160×120-Pixels Range Camera With In-Pixel Correlated Double Sampling and Fixed-Pattern Noise Correction," *IEEE Journal of Solid State Circuits*, vol. 46, no. 7, pp. 1672–1681, 2011.

[50] N. Cottini, M. Gottardi, N. Massari, R. Passerone, and Z. Smilansky, "A 33-μW 64×64 Pixel Vision Sensor Embedding Robust Dynamic Background Subtraction for Event Detection and Scene Interpretation," *IEEE Journal of Solid State Circuits*, vol. 48, no. 3, pp. 850–863, 2013.

[51] M. Loinaz, K. Singh, A. Blanksby, D. Inglis, K. Azadet, and B. Ackland, “A 200-mW, 3.3-V, CMOS Color Camera IC Producing 352×288 24-b Video at 30 Frames/s,” *IEEE Journal of Solid State Circuits*, vol. 33, no. 12, pp. 2092—-2103, 1998.

[52] S. Smith, J. Hurwitz, M. Torrie, D. Baxtr, A. Murray, P. Likoudis, A. Holmes, M. Panaghiston, R. Henderson, S. Anderson, P. Denyer, and D. Renshaw, “A Single-Chip CMOS 306×244-Pixel NTSC Video Camera and a Descendant Coprocessor Device,” *IEEE Journal of Solid State Circuits*, vol. 33, no. 12, pp. 2104–2111, 1998.

[53] M. Snoeij, A. Theuwissen, K. A. A. Makinwa, and J. Huijsing, “A CMOS Imager With Column-Level ADC Using Dynamic Column Fixed-Pattern Noise Reduction,” *IEEE Journal of Solid State Circuits*, vol. 41, no. 12, pp. 3007–3015, 2006.

[54] R. Xu, B. Liu, and J. Yuan, “A 1500-fps Highly Sensitive 256×256 CMOS Imaging Sensor With In-Pixel Calibration,” *IEEE Journal of Solid State Circuits*, vol. 6, no. 6, pp. 1408–1418, 2012.

[55] J. Lee, I. Baek, D. Yang, and K. Yang, “On-Chip FPN Calibration for a Linear-Logarithmic APS Using Two-Step Charge Transfer,” *IEEE Transactions on Electron Devices*, vol. 60, no. 6, pp. 1989–1994, 2013.

[56] S. Kleinfelder, S. Lim, X. Liu, and A. El-Gamal, “A 10000 Frames/s CMOS Digital Pixel Sensor,” *IEEE Journal of Solid State Circuits*, vol. 12, no. 12, pp. 2049–2059, 2001.

[57] W. Bidermann, A. E. Gamal, S. Ewedemi, J. Reyneri, H. Tian, D. Wile, and D. Yang, “A 0.18 μm High Dynamic Range NTSC/PAL Imaging System-on-Chip with Embedded DRAM Frame Buffer,” in *Proceedings of the International Solid-State Circuits Conference*, pp. 212–213, 2003.

[58] A. Kitchen, A. Bermak, and A. Bouzerdoum, “A Digital Pixel Sensor Array with Programmable Dynamic Range,” *IEEE Transactions on Electron Devices*, vol. 52, no. 12, pp. 2591–2601, 2005.

[59] D. H. Woo, C. H. Hwang, Y. S. Lee, and H. C. Lee, “Time-Based Pixel-Level ADC with Wide Dynamic Range for 2-D LWIR Applications,” *IET Electronics Letters*, vol. 41, no. 14, pp. 782–783, 2005.

[60] M. Sawan and A. Trépanier and J.-L. Trépanier and Y. Audet and R. Ghannoum, “A New CMOS Multimode Digital Pixel Sensor Dedicated to an Implantable Visual Cortical Stimulator,” *Journal of Analog Integrated Circuits and Signal Processing, Springer Engineering*, vol. 49, pp. 187–197, 2006.

[61] A. Bermak and Y.-F. Yung, “A DPS Array With Programmable Resolution and Reconfigurable Conversion Time,” *IEEE Transactions on Very Large Scale Integration Systems*, vol. 14, no. 1, pp. 15–22, 2006.

[62] C. Shoushun, F. Boussaid, and A. Bermak, “Robust Intermediate Read-out for Deep Submicron Technology CMOS Image Sensors,” *IEEE Sensors Journal*, vol. 8, no. 3, pp. 286–294, 2008.

[63] J. Crooks, S. Bohndiek, C. Arvanitis, R. Speller, H. XingLiang, E. Villani, M. Towrie, and R. Turchetta, “A CMOS Image Sensor with in-Pixel ADC, Timestamp, and Sparse Readout,” *IEEE Sensors Journal*, vol. 9, no. 1, pp. 20–28, 2009.

[64] C. Posch, D. Matolin, and R. Wohlgenannt, “A QVGA 143 dB Dynamic Range Frame-Free PWM Image Sensor with Lossless Pixel-Level Video Compression and Time-Domain CDS,” *IEEE Transactions on Circuits and Systems-II*, vol. 46, no. 1, pp. 259–275, 2011.

[65] L. G. McIlrath, “A Low-Power Low-Noise Ultrawide-Dynamic-Range CMOS Imager with Pixel-Parallel A/D Conversion,” *IEEE Journal of Solid State Circuits*, vol. 36, no. 5, pp. 846–853, 2001.

[66] E. Culurciello, R. Etienne-Cummings, and K. Boahen, “A Biomorphic Digital Image Sensor,” *IEEE Journal of Solid State Circuits*, vol. 38, no. 2, pp. 281–294, 2003.

[67] Y. M. Chi, U. Mallik, M. A. Clapp, E. Choi, G. Cauwenberghs, and R. Etienne-Cummings, “CMOS Camera With In-Pixel Temporal Change Detection and ADC,” *IEEE Journal of Solid State Circuits*, vol. 42, no. 10, pp. 2187–2196, 2007.

[68] J. Costas-Santos, T. Serrano-Gotarredonda, R. Serrano-Gotarredonda, and B. Linares-Barranco, “A Spatial Contrast Retina With On-Chip Calibration for Neuromorphic Spike-Based AER Vision Systems,” *IEEE Transactions on Circuits and Systems-I*, vol. 54, no. 7, pp. 1444–1458, 2007.

[69] R. Berner and T. Delbruck, “Event-Based Pixel Sensitive to Changes of Color and Brightness,” *IEEE Transactions on Circuits and Systems-I*, vol. 58, no. 7, pp. 1581–1590, 2011.

[70] T. Serrano-Gotarredona and B. Linares-Barranco, “A 128×128 1.5% Contrast Sensitivity 0.9% FPN 3-μs Latency 4-mW Asynchronous Frame-Free Dynamic Vision Sensor Using Transimpedance Preamplifiers,” *IEEE Journal of Solid State Circuits*, vol. 48, no. 3, pp. 827–838, 2013.

[71] J. Rhee and Y. Joo, “Wide Dynamic Range CMOS Image Sensor with Pixel Level ADC,” *IET Electronics Letters*, vol. 39, no. 4, pp. 360–361, 2003.

[72] J. Leñero-Bardallo and P. Hafliger, “A Dual-Operation-Mode Bio-Inspired Pixel,” *IEEE Transactions on Circuits and Systems-II*, vol. 61, no. 11, pp. 855–859, 2014.

[73] E. Culurciello, R. Etienne-Cummings, and K. Boahen, “Arbitrated Address-Event Representation Digital Image Sensor,” *IET Electronics Letters*, vol. 37, no. 24, pp. 1443–1445, 2001.

[74] C. Shoushun and A. Bermak, “Arbitrated Time-to-First Spike CMOS Image Sensor With On-Chip Histogram Equalization,” *IEEE Transactions on Very Large Scale Integration Systems*, vol. 15, pp. 346–357, 2007.

[75] P. Topart, C. Alain, L. LeNoc, S. Leclair, Y. Desroches, B. Tremblay, and H. Jerominek, “Hybrid Micropackaging Technology for Uncooled FPAs,” in *Proceedings of SPIE*, vol. 5783, pp. 544–550, 2005.

[76] M. Bigas, E. Cabruja, M. Lozano, F. Serra-Graells, and L. Terés, “Modular Hybrid Device for Reading Image Sensor Arrays,” 2007.

[77] J. W. Beletic, R. Blank, D. Gulbransen, D. Lee, M. Loose, E. C. Piquette, T. Sprafke, W. E. Tennant, M. Zandian, and J. Zino, “Teledyne Imaging Sensors: Infrared Imaging Technologies for Astronomy & Civil Space,” in *Proceedings of SPIE*, vol. 7021, 2008.

[78] J. Rothman, E. de Borniol, P. Ballet, L. Mollard, S. Gout, M. Fournier, J. P. Chamonal, G. Destéfanis, F. Pistone, S. Courtas, X. Lefoule, and P. Tribolet, “HgCdTe APD-Focal Plane Array Performance at DEFIR,” in *Proceedings of SPIE*, vol. 7298, 2009.

[79] J. A. Robo, E. Costard, J. P. Truffer, A. Nedelcu, X. Marcadet, and P. Bois, “QWIP Focal Plane Arrays Performances from MWIR to VLWIR,” in *Proceedings of SPIE*, vol. 7298, 2009.

[80] M. Razeghi, D. Hoffman, B. M. Nguyen, P.-Y. Delaunay, E. K. Huang, M. Z. Tidrow, and V. Nathan, “Recent Advances in LWIR Type-II InAs/GaSb Superlattice Photodetectors and Focal Plane Arrays at the Center for Quantum Devices,” *Proceedings of the IEEE*, vol. 97, pp. 1056–66, 2009.

[81] A. Peizerat, J.-P. Rostaing, N. Zitouni, N. Baier, F. Guellec, R. Jalby, and M. Tchagaspanian, “An 88dB SNR, 30μm pixel pitch Infra-Red image sensor with a 2-step 16 bit A/D conversion,” pp. 128–129, 2012.

[82] “MARS LW. The Reference LWIR Staring Array,” tech. rep., Sofradir EC, Inc, 2015.

[83] E. Ilan, N. Shiloah, S. Elkind, R. Dobromislin, W. Freiman, A. Zviagintsev, I. Nevo, O. Cohen, F. Khinich, A. Adin, R. Talmor, and Y. Milstain, “A 3Mpixel ROIC with 10μm Pixel Pitch and 120Hz Frame Rate Digital Output,” in *Proceedings of SPIE*, vol. 8659, 2013.

[84] “Blackbird. MWIR InSb detector, 1920 x 1536 format, 10μm pitch, Digital ROIC,” tech. rep., SCD Semiconductor Devices, 2015.

[85] B. Simolon, N. Aziz, S. Cogan, E. Kurth, S. Lam, S. Petronio, J. Woolaway, S. Bandara, S. Gunapala, and J. Mumolo, “High Performance Two-Color One Megapixel CMOS ROIC for QWIP Detectors,” *Elsevier Infrared Physics & Technology*, vol. 52, no. 6, pp. 391—-394, 2009.

[86] S. Gunapala, S. Bandara, J. K. Liu, J. Mumolo, D. Ting, C. J. Hill, J. Nguyen, B. Simolon, J. Woolaway, S. Wang, W. Li, P. LeVan, and M. Tidrow, "Demonstration of Megapixel Dual-Band QWIP Focal Plane Array," vol. 46, no. 2, pp. 285–293, 2010.

[87] R. Blackwell, D. Lacroix, T. Bach, J. Ishii, S. Hyland, J. Geneczko, S. Chan, B. Sujlana, and M. Joswick, "Uncooled VOx Systems at BAE Systems," in *Proceedings of SPIE*, vol. 6940, 2008.

[88] J. Lv, L. Que, L. Wei, Y. Zhou, B. Liao, and Y. Jiang, "Uncooled Microbolometer Infrared Focal Plane Array Without Substrate Temperature Stabilization," *IEEE Sensors Journal*, vol. 14, no. 5, pp. 1533–1544, 2014.

[89] P. Robert, J. Tissot, D. Pochic, V. Gravot, F. Bonnaire, H. Clerambault, A. Durand, and S. Tinnes, "Uncooled 17μm 1/4 VGA IRFPA Development for Compact and Low Power Systems," in *Proceedings of the SPIE*, vol. 8541 of *Electro-Optical and Infrared Systems: Technology and Applications IX*, 2012.

[90] C. Posch, D. Matolin, R. Wohlgenannt, T. Maier, and M. Litzenberger, "A Microbolometer Asynchronous Dynamic Vision Sensor for LWIR," *IEEE Sensors Journal*, vol. 9, no. 6, pp. 654–664, 2009.

[91] B. Dupont, A. Dupret, S. Becker, A. Hamelin, F. Guellec, P. Imperinetti, and W. Rabaud, "A [10°C; 70°C] 640x480 17μm Pixel Pitch TEC-Less IR Bolometer Imager with Below 50mK and Below 4V Power Supply," in *Proceedings of the International Solid-State Circuits Conference*, pp. 394–396, IEEE, 2013.

[92] "Strategic Research Agenda," tech. rep., The European Technology Platform on Smart Systems Integration (EPoSS), 2009.

[93] "Strategic Research Agenda Pre-Print," tech. rep., The European Technology Platform on Smart Systems Integration (EPoSS), 2013.

[94] "Towards 2020– Photonics Driving Economic Growth in Europe," tech. rep., European Technology Platform Photonics21, 2013.

[95] F. Serra-Graells, A. Rueda, and J. L. Huertas, *Low-Voltage CMOS Log Companding Analog Design.* Engineering and Computer Science: Analog Circuits and Signal Processing, Kluwer Academic Publishers, 2003.

[96] C. C. Enz, F. Krummenacher, and E. A. Vittoz, "An Analytical MOS Transistor Model Valid in All Regions of Operation and Dedicated to Low-Voltage and Low-Current Applications," *Journal of Analog Integrated Circuits and Signal Processing, Kluwer Academic Publishers*, vol. 8, no. 1, pp. 83–114, 1995.

[97] E. A. Vittoz, "Weak Inversion for Ultra Low-Power and Very Low-Voltage Circuits," in *Solid-State Circuits Conference, 2009. A-SSCC 2009. IEEE Asian*, pp. 129 – 132, IEEE, IEEE, 2009.

[98] D. Woo, I. Nam, and H. Lee, "Smart Reset Control for Wide-Dynamic-Range LWIR FPAs," *IEEE Sensors Journal*, vol. 11, no. 1, pp. 131–136, 2011.

[99] K. Murari, R. Etienne-Cummings, N. Thakor, and G. Cauwenberghs, "A CMOS In-Pixel CTIA High-Sensitivity Fluorescence Imager," *IEEE Transactions on Biomedical Circuits and Systems*, vol. 5, no. 5, pp. 449–458, 2011.

[100] H.-S. Kim, S.-W. Han, J.-H. Yang, S. Kim, Y. Kim, S. Kim, D.-K. Yoon, J.-S. Lee, J.-C. Park, Y. Sung, S.-D. Lee, S.-T. Ryu, and G.-H. Cho, "An Asynchronous Sampling-Based 128×128 Direct Photon-Counting X-Ray Image Detector with Multi-Energy Discrimination and High Spatial Resolution," *IEEE Journal of Solid State Circuits*, vol. 48, no. 2, pp. 541–558, 2013.

[101] S. Otim, B. Choubey, D. Joseph, and S. Collins, "Characterization and Simple Fixed Pattern Noise Correction in Wide Dynamic Range "Logarithmic" Imagers," *IEEE Transactions on Instrumentation and Measurement*, vol. 56, no. 5, pp. 1910–1916, 2007.

[102] A. Hastings, *The Art of Analog Layout.* Prentice Hall, 2005.

[103] X. Wang, W. Wong, and R. Hornsey, "A High Dynamic Range CMOS Image Sensor With Inpixel Light-to-Frequency Conversion," vol. 53, no. 12, pp. 2988–2992, 2006.

[104] D. Ho, M. Noor, U. Krull, G. Gulak, and R. Genov, "CMOS Tunable-Color Image Sensor With Dual-ADC Shot-Noise-Aware Dynamic Range Extension," *IEEE Transactions on Circuits and Systems-I*, vol. 60, no. 8, pp. 2116–2129, 2013.

[105] K. Gofrey, *Perturbation Signals for System Identification.* Prentice Hall, 1993.

[106] R. E. Suarez, P. R. Gray, and D. A. Hodges, "All-MOS Charge Redistribution Analog-to-Digital Conversion Techniques - Part II," *IEEE Journal of Solid State Circuits*, vol. 10, no. 6, pp. 379–385, 1975.

[107] S. Ouzounov, E. Roza, J. Hegt, G. van der Weide, and A. van Roermund, "Analysis and Design of High-Performance Asynchronous Sigma-Delta Modulators with a Binary Quantizer," *IEEE Journal of Solid State Circuits*, vol. 41, no. 3, pp. 588–596, 2006.

[108] A. Alvarado, M. Rastogi, J. Harris, and J. Principe, "The Integrate-and-Fire Sampler: A Special Type of Asynchronous $\Sigma - \Delta$ Modulator," in *Proceedings of the International Symposium on Circuits and Systems*, 2011.

[109] M. Peng and H.-S. Lee, "Study of Substrate Noise and Techniques for Minimization," *IEEE Journal of Solid State Circuits*, vol. 39, no. 11, pp. 2080–2086, 2004.

[110] A. Bendali and Y. Audet, "A 1-V CMOS Current Reference with Temperature and Process Compensation," *IEEE Transactions on Circuits and Systems-I*, vol. 54, no. 7, pp. 1424–1429, 2007.

[111] C. Yoo and J. Park, "CMOS Current Reference with Supply and Temperature Compensation," *IET Electronics Letters*, vol. 43, no. 25, 2007.

[112] G. D. Vita and G. Iannacone, "A Sub-1V, 10ppm/°C, Nanopower Voltage Reference Generator," *IEEE Journal of Solid State Circuits*, vol. 42, no. 7, pp. 1536–1542, 2007.

[113] A. Becker-Gomez, T. Lakshmi, and T. R. Viswanathan, “A Low-Supply-Volatge CMOS Sub-Bandgap Reference,” *IEEE Transactions on Circuits and Systems-II*, vol. 55, no. 7, pp. 609–613, 2008.

[114] W. Yand, W. Li, and R. Liu, “Nanopower CMOS Sub-Bandgap Reference with 11ppm/°C Temperature Coefficient,” *IET Electronics Letters*, vol. 45, no. 12, 2009.

[115] K. Ueno, T. Hirose, T. Asai, and Y. Amemiya, “A 300 nW, 15 ppm/$\circ$ C, 20 ppm/V CMOS Voltage Reference Circuit Consisting of Subthreshold MOSFETs,” *IEEE Journal of Solid State Circuits*, vol. 44, no. 7, pp. 2047—-2054, 2009.

[116] L. Magnelli, F. Crupi, P. Corsonello, C. Pace, and G. Iannaccone, “A 2.6 nW, 0.45 V Temperature-Compensated Subthreshold CMOS Voltage Reference,” *IEEE Journal of Solid State Circuits*, vol. 46, no. 2, pp. 465—-474, 2011.

[117] F. Serra-Graells and J. L. Huertas, “Sub-1V CMOS Proportional-to-Absolute-Temperature References,” *IEEE Journal of Solid State Circuits*, vol. 38, no. 1, pp. 84–88, 2003.

[118] M. J. M. Pelgrom, A. C. J. Duinmaijer, and A. P. G. Welbers, “Matching Properties of MOS transistors,” *IEEE Journal of Solid State Circuits*, vol. 24, no. 5, pp. 1433–1440, 1989.

[119] T. Delbruck, B. Linares-Barranco, E. Culurciello, and C. Posch, “Activity-Driven, Event-Based Vision Sensors,” in *Proceedings of the International Symposium on Circuits and Systems*, pp. 2426–2429, IEEE, 2010.

[120] M. Azadmehr, J. Abrahamsen, and P. Häfliger, “A Foveated AER Imager Chip,” in *Proceedings of the International Symposium on Circuits and Systems*, vol. 3, pp. 2751–2754, 2005.

[121] R.-J. Vogelstein, U. Mallik, E. Culurciello, R. Etienne-Cummings, and G. Cauwenberghs, “Spatial Acuity Modulation of an Address-Event Imager,” in *Proceedings of the International Conference on Electronics Circuits and Systems*, pp. 207–210, 2004.

[122] P. Ruedi, P. Heim, F. Kaess, E. Grenet, F. Heitger, P.-Y. Burgi, S. Gyger, and P. Nussbaum, "A 128 x 128 Pixel 120-dB Dynamic-Range Vision-Sensor Chip for Image Contrast and Orientation Extraction," *IEEE Journal of Solid State Circuits*, vol. 38, pp. 2325–2333, 2003.

[123] J. Kramer, "An Integrated Optical Transient Sensor," *IEEE Transactions on Circuits and Systems-II*, vol. 49, pp. 612–628, 2002.

[124] P. Lichtsteiner, C. Posch, and T. Delbruck, "A 128×128 120dB 15μs Latency Asynchronous Temporal Contrast Vision Sensor," *IEEE Journal of Solid State Circuits*, vol. 43, no. 2, pp. 566–576, 2008.

[125] P.-F. Ruedi, P. Heim, S. Gyger, F. Kaess, C. Arm, R. Caseiro, J.-L. Nagel, and S. Todeschini, "An SoC Combining a 132dB QVGA Pixel Array and a 32b DSP/MCU Processor for Vision Applications," in *Proceedings of the International Solid-State Circuits Conference*, pp. 46–47,47a, IEEE, 2009.

[126] E. Özalevli and C. Higgins, "Reconfigurable Biologically Inspired Visual Motion System using Modular Neuromorphic VLSI Chips," *IEEE Transactions on Circuits and Systems-I*, vol. 52, pp. 79–92, 2005.

[127] K. Boahen, "Retinomorphic Chips that See Quadruple Images," in *International Conference on Microelectronics for Neural, Fuzzy and Bio-inspired Systems, MicroNeuro*, pp. 12–20, 1999.

[128] K. Zaghloul and K. Boahen, "Optic Nerve Signals in a Neuromorphic Chip I: Outer and Inner RetinaModels," *IEEE Transactions on Biomedical Engineering*, vol. 51, pp. 657–666, 2004.

[129] K. Zaghloul and K. Boahen, "Optic Nerve Signals in a Neuromorphic Chip II: Testing and Results," *IEEE Transactions on Biomedical Engineering*, vol. 51, pp. 667–675, 2004.

[130] M. Sivilotti, *Wiring Considerations in Analog VLSI Systems, with Application to Field-Programmable Networks.* PhD thesis, California Institute of Technology, Pasadena, CA, USA, 1991.

[131] M. Mahowald, *An Analog VLSI System for Stereoscopic Vision*, vol. 265 of *The Springer International Series in Engineering and Computer Science*. Springer, 1994.

[132] K. Boahen, “Point-to-point Connectivity Between Neuromorphic Chips Using Address Events,” *IEEE Transactions on Circuits and Systems-II*, vol. 47, pp. 416–434, 2000.

[133] K. Boahen, “A Burst-Mode Word-Serial Address-Event Link—I: Transmitter Design,” *IEEE Transactions on Circuits and Systems-I*, vol. 51, no. 7, pp. 1269–1280, 2004.

[134] C. Brandli, R. Berner, M. Yang, S.-C. Liu, and T. Delbruck, “A 240 × 180 130 dB 3 μs Latency Global Shutter Spatiotemporal Vision Sensor,” *IEEE Journal of Solid State Circuits*, vol. 49, no. 19, pp. 2333–2341, 2014.

[135] R. Berner, *Building-Blocks for Event-Based Vision Sensors*. PhD thesis, Eidgenossische Technische Hochschule ETH Zurich, 2011.

[136] M.-H. Yang, S.-C. Liu, and T. Delbruck, “A Dynamic Vision Sensor with 1% Temporal Contrast Sensitivity and In-Pixel Asynchronous Delta Modulator for Event Encoding,” *IEEE Journal of Solid State Circuits*, vol. 50, no. 9, pp. 2149–2160, 2015.

[137] F. Serra-Graells and J. L. Huertas, “Low-Voltage CMOS Subthreshold Log-Domain Filtering,” *IEEE Transactions on Circuits and Systems-I*, vol. 52, no. 10, pp. 2090–2100, 2005.

[138] B. Linares-Barranco, T. Serrano-Gotarredona, and R. Se, “Compact Low-Power Calibration Mini-DACs for Neural Arrays With Programmable Weights,” *IEEE Transactions on Neural Networks*, vol. 14, no. 5, pp. 1207–1216, 2003.

[139] J. A. Leñero-Bardallo, T. Serrano-Gotarredona, and B. Linares-Barranco, “A Calibration Technique for Very Low Current and Compact Tunable Neuromorphic Cells: Application to 5-bit 20-nA DACs,” *IEEE Transactions on Circuits and Systems-II*, vol. 55, no. 6, pp. 522–526, 2008.

[140] A. Martin and M. Nystrom, “Asynchronous Techniques for System-on-Chip Design,” *Proceedings of the IEEE*, vol. 94, no. 6, pp. 1089–1120, 2006.

[141] S. Chen and A. Bermak, “Arbitrated time-to-first spike CMOS image sensor with on-chip histogram equalization,” *IEEE Transactions on Very Large Scale Integration Systems*, vol. 15, no. 3, pp. 346–357, 2007.

[142] A. M. T. Lyn, D. A. Tuan, C. Shoushun, and Y. K. Seng, “Adaptive Priority Toggle Asynchronous Tree Arbiter for AER-based Image Sensor,” in *IEEE International Conference on VLSI and System-on-Chip* (IEEE, ed.), pp. 66–71, 2011.

[143] J. Georgiou and A. Andreou, “High-speed, Address-Encoding Arbiter Architecture,” *IET Electronics Letters*, vol. 42, no. 3, pp. 170–171, 2006.

[144] R. Berner, T. Delbruck, A. Civit-Balcells, and A. Linares-Barranco, “A 5 Meps $100 USB2.0 Address-Event Monitor-Sequencer Interface,” in *Proceedings of the International Symposium on Circuits and Systems*, 2007.

[145] A. Linares-Barranco, R. Paz, A. Jimenez-Fernandez, C. Lujan, M. Rivas, J. Sevillano, G. Jimenez, and A. Civit, “Neuro-Inspired Real-Time USB & PCI to AER Interfaces for Vision Processing,” in *Proceedings of the International Symposium on Performance Evaluation of Computer and Telecommunication Systems*, pp. 330–337, 2008.

[146] G. Fasnacht, D.B.and Indiveri, “A PCI Based High-Fanout AER Mapper with 2 GiB RAM Look-Up Table, 0.8 μs Latency and 66MHz Output Event-Rate,” in *Proceedings of the Annual Conference on Information Sciences and Systems*, 2011.

[147] T. Delbruck, “Frame-free Dynamic Digital Vision,” in *Proceedings of the International Symposium on Secure-Life Electronics, Advanced Electronics and Quality Life and Society*, pp. 21–26, 2008.

[148] M. Lozano, E. Cabruja, A. Collado, J. Santander, and M. Ullán, "Bump Bonding of Pixel Systems," *Nuclear Instruments and Methods in Physics Research*, vol. 473, no. 1–2, pp. 95–101, 2001.

[149] R. Paz-Vicente, E. Cerezuela-Escudero, M. Dominguez-Morales, A. Jimenez-Fernandez, A. Linares-Barranco, and G. Jimenez-Moreno, "A Perfomance Comparison Study Between Synchronous and Asynchronous FPGA for Spike Based Systems. Under the AER Synthetic Generation," in *Proceedings of the International Symposium on Performance Evaluation of Computer and Telecommunication Systems*, pp. 38–45, 2011.