

# A CMOS Imager for Time-of-Flight and Photon Counting Based on Single Photon Avalanche Diodes and In-Pixel Time-to-Digital Converters

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**Abstract.** The design of a CMOS image sensor based on single-photon avalanche-diode (SPAD) array with in-pixel time-to-digital converter (TDC) is presented. The architecture of the imager is thoroughly described with emphasis on the characterization of the TDCs array. It is targeted for 3D image reconstruction. Several techniques as fast quenching/recharge circuit with tunable dead-time and time gated-operation are applied to reduce the noise and the power consumption. The chip was fabricated in a 0.18  $\mu\text{m}$  standard CMOS process and implements a double functionality: time-of-flight (ToF) estimation and photon counting. The imager features a programmable time resolution of the array of TDCs down to 145 ps. The measured accuracy of the minimum time bin is lower than  $\pm 1\text{LSB DNL}$  and  $\pm 1.7\text{ LSB INL}$ . The TDC jitter over the full dynamic range is less than 1 LSB.

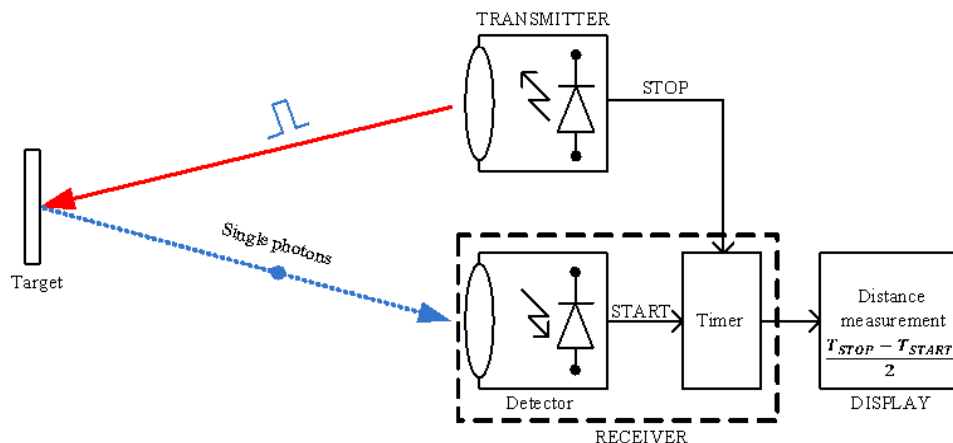
**Key words:** direct time-of-flight; photon counting; in-pixel time-to-digital converter; time gating; single photon avalanche diode.

## 1. Introduction

Amongst the different approaches to estimate the depth map of scenes, the use of Single Photon Avalanche Diodes (SPAD) proved to be very appealing for applications

involving low light conditions [1]. This kind of imagers based on SPADs is able to acquire 2-D images at high frame rate by merely counting photons. Moreover they incorporate additional functionality of time-of-flight estimation for 3-D image reconstruction [2].

3-D ranging systems are classified into: *i*) interferometers based on the superposition of two waves of the same frequency whose phase difference determines the resulting pattern; *ii*) double acquisition or stereoscopic systems [3], which requires a large amount of computation to solve the correspondence problem – which pairs of points in the two images are projections of the same point in the scene –; *iii*) single-sensor active-illumination systems, which rely on the Time-of-Flight (ToF) technique [4]. The computation of ToF can be made either indirectly or directly. Indirect ToF (iToF) relies on the phase shift between a pulsed [5] or continuous-modulated [6] light source and the detected signal. Both illumination sources are employed to improve the expected depth resolution for different background levels and target distances [7]. Indirect ToF requires the measurement of the amplitude of the back-scattered light in different charge-integration or photon counting windows [8]. This is the most suitable technique for automotive applications. Direct ToF (dToF) approach is based on the measurement of the time required by a photon to travel from the transmitter towards a target and back to the detector. The illuminator is an accurate picosecond-width pulsed light source. Figure 1 shows a typical arrangement for depth map estimation by applying dToF technique. The chip presented in this work is able to implement both dToF and iToF techniques.



**Fig. 1.** Principle of direct ToF measurement based on picosecond-width pulsed light.

Besides night vision applications, requiring a very high sensitivity, these SPAD-based systems find applications for complex imaging tasks such as looking around corners [9].

Human face reconstruction is also possible even with 115 ps time resolution [1]. ToF estimation is also used in medical imaging like Positron Emission Tomography (PET) [10] and in other biomedical techniques dealing with a faint light source, like

Fluorescence Lifetime Imaging Microscopy (FLIM) which requires a time bin below 100 ps [4].

The architecture of the SPAD-based image sensor with in-pixel Time-to-Digital Converter (TDC) and the characterization of the TDCs array were briefly presented [11]. This work is focused on the extended description of the imager, thoroughly explaining its functionalities. Additional details of the design at architectural and transistor level are shown. In order to have a better insight of the sensor design, new block diagrams of the chip, post-layout simulations and measurements of the array of TDCs are presented as well. The imager incorporates both 2-D and 3-D imaging capabilities by in-pixel photon counting and ToF measurement. An external time interval can be routed simultaneously to the TDCs of each imager's row. In this case the chip acts as a 64 channels-TDC. The goal is to achieve the best possible performance using a standard CMOS process without any low-noise and/or high-voltage features. Several techniques at architectural and transistor level have been applied as: *i*) in-pixel TDC to achieve a high frame rate, up to 1 kfps; *ii*) fast active quenching/recharge circuit for afterpulsing and power consumption reduction; *iii*) reverse start/stop scheme (Fig. 5) and time-gated SPAD front-end to mitigate the power consumption and Dark Count Rate (DCR). Using a compact pseudo-differential Voltage-Controlled Ring-Oscillator (VCRO), the in-pixel TDC area is of  $1740 \mu\text{m}^2$  which is smaller than the state-of-the-art [4], [12]. The normalized power consumption per TDC is of  $9 \mu\text{W}$  to convert a time interval of 10 ns at 500 k conversions per second, which is three times smaller than the one reported in [12]. Moreover we have achieved better time resolution for a smaller amount of power (see Table 1). The standard deviation of the output of the TDCs for uniform illumination across the array is about 19 codes (out of  $2^{11} = 2048$  codes). This figure is evaluated without applying any pixel-to-pixel calibration. The FWHM jitter of the TDC is 133 ps (or 0.92 LSB). The last two measurements have been performed at 90% of the full input range (or 270 ns).

The rest of the paper is organized as follows: the second section describes the functionality of the imager. The design of chip is thoroughly explained at architectural and transistor level. The third section is dedicated to experimental results. The fourth section concludes this work with the most representative achievements.

## 2. Architecture of the 3D image sensor

The proposed design occupies an area of  $5 \times 5 \text{ mm}^2$ , including the pad ring. It incorporates an array of  $64 \times 64$  2-D/3-D smart pixels, analog I/O buffers, fast signal distribution trees, row decoder, fast data serializer and a programmable Phase Locked-Loop (PLL). The block diagram of the chip is shown in Fig. 2.

The sensor array fits in less than  $4.1 \times 4.1 \text{ mm}^2$ . Analog buffers are needed to drive the voltage reference to each in-pixel ring oscillator. It is provided by the on-chip PLL. Thereby it overcomes the effects of uniform process, voltage supply and temperature variations [12]. Moreover analog input buffers are required to uniformly distribute the control signal for the dead time of the SPADs. Fast signal distribution

network is needed to share the same START and STOP signals for the array of TDCs. In addition to that, a rolling-shutter activation strategy is applied for the converters array to decrease the overall power consumption.

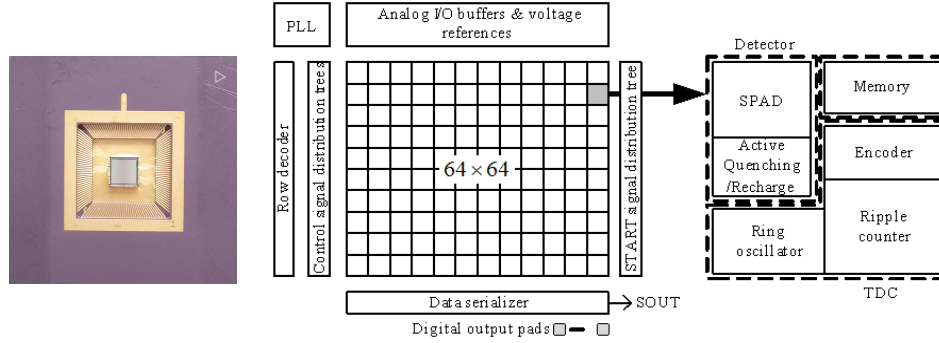


Fig. 2. Photo and block diagram of the chip.

A row decoder is implemented to read the imager line by line. Notice that for this kind of sensors the most appropriate scheme is a serial input parallel output shift register. This scheme is faster, more compact than the regular decoder based on logic gates and overcomes pulse overlapping. The programmable PLL enables adjustable time resolution. An extensive description of the architecture is provided in the subsection 2.2.

### 2.1. Imager functionality

The imager can be configured to work either in *i*) test, *ii*) 3-D or *iii*) 2-D mode.

*i*) In test mode, TDCs can be independently measured. Post-layout simulation of only three channels of the TDCs array is depicted in Fig. 3. In this scenario the imager works as a 64-channels TDC, as one single row of the array at a time is selected. Before any conversion sequence starts, all the pixels has to be reset by the global R signal (see subset a).

The subset b) represents the start (Ext.Start1-3) and stop (Ext.Stop) signals distributed to the first three rows/ channels. These external signals are provided by a time interval generator implemented on a VIRTEX5 FPGA [13]. The subset c) plots the first phase of the VCRO of cell (1, 64), (2, 64) and (3, 64) of the corresponding TDCs. The time intervals that fall between the rising edge of consecutive start and stop signals are simultaneously measured and the time stamps are stored in the local memory of each pixel. Afterwards the imager is readout offline. The last three subsets show how the bit streams of the pixels (1, 64) and (2, 64) are sequentially loaded in the output buffer and serially delivered off-chip.

The jitter of the TDC,  $\tau_{TDC}$ , is estimated by:

$$\tau_{TDC} = \sqrt{\tau_T^2 - \tau_{Start}^2 - \tau_{Stop}^2}, \quad (1)$$

where  $\tau_T$  is the total jitter,  $\tau_{Start}$  and  $\tau_{Stop}$  are the jitter of the start and stop signals. Special care needs to be put in the routing of these signals. They should be shielded and symmetrically loaded by the parasitic capacitances. Moreover they need to uniformly drive the different rows of the array, therefore a skew-less distribution scheme has been designed.

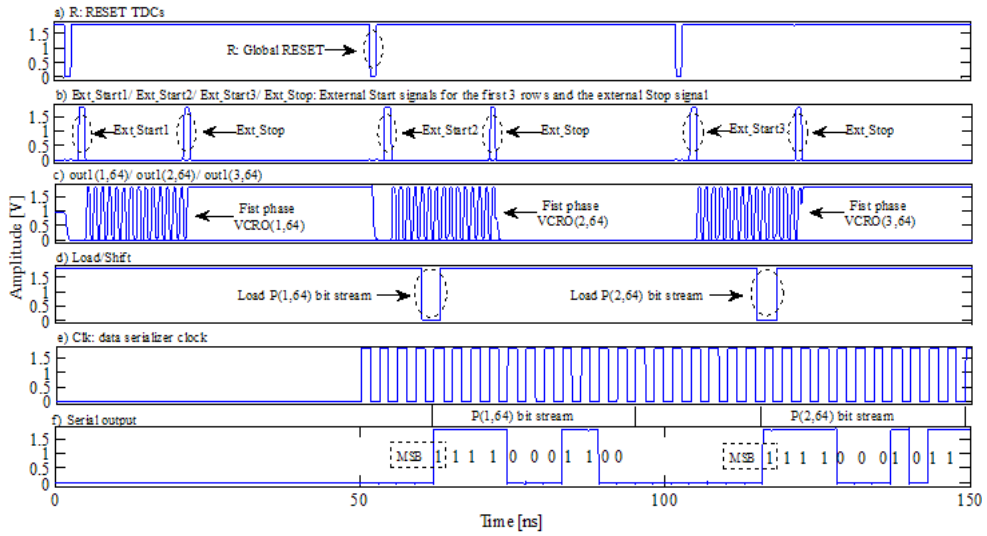


Fig. 3. Signals chronogram in test operation mode.

ii) In the 3D-mode each pixel measures the time elapsed from the actual detection to the next stop pulse of the synchronization signal. A time-gated measurement for the pixel (1, 64) is depicted in Fig. 4. Right after the SPAD is enabled, the pixel has to be reset (see the first two subsets). Subsets c) and d) show that the TDC is started by the first detected event,  $V_{out}$ , and stopped by the global Ext\_Stop signal. Moreover TDCs are not sensitive to the variation of SPADs dead-times. Subset e) plots the first phase of the VCRO. In the subsets g) and h) the first row is selected to be loaded in the data serializer and the time stamp is written in the local memory of the pixel. The last three subsets show how the first row bit stream is delivered off-chip starting with the digital code of the time interval resolved by the pixel (1, 64). Further, the depth map of the target can be inferred from the measured time intervals, considering that  $2T_{ToF} = T_{laser} - T_{measured}$  (Fig. 5).

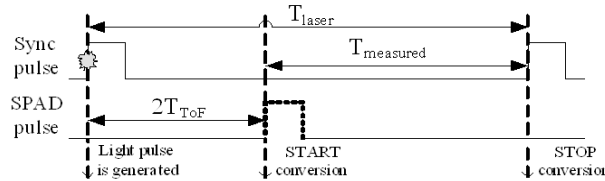


Fig. 5. Reverse start-stop scheme diagram.

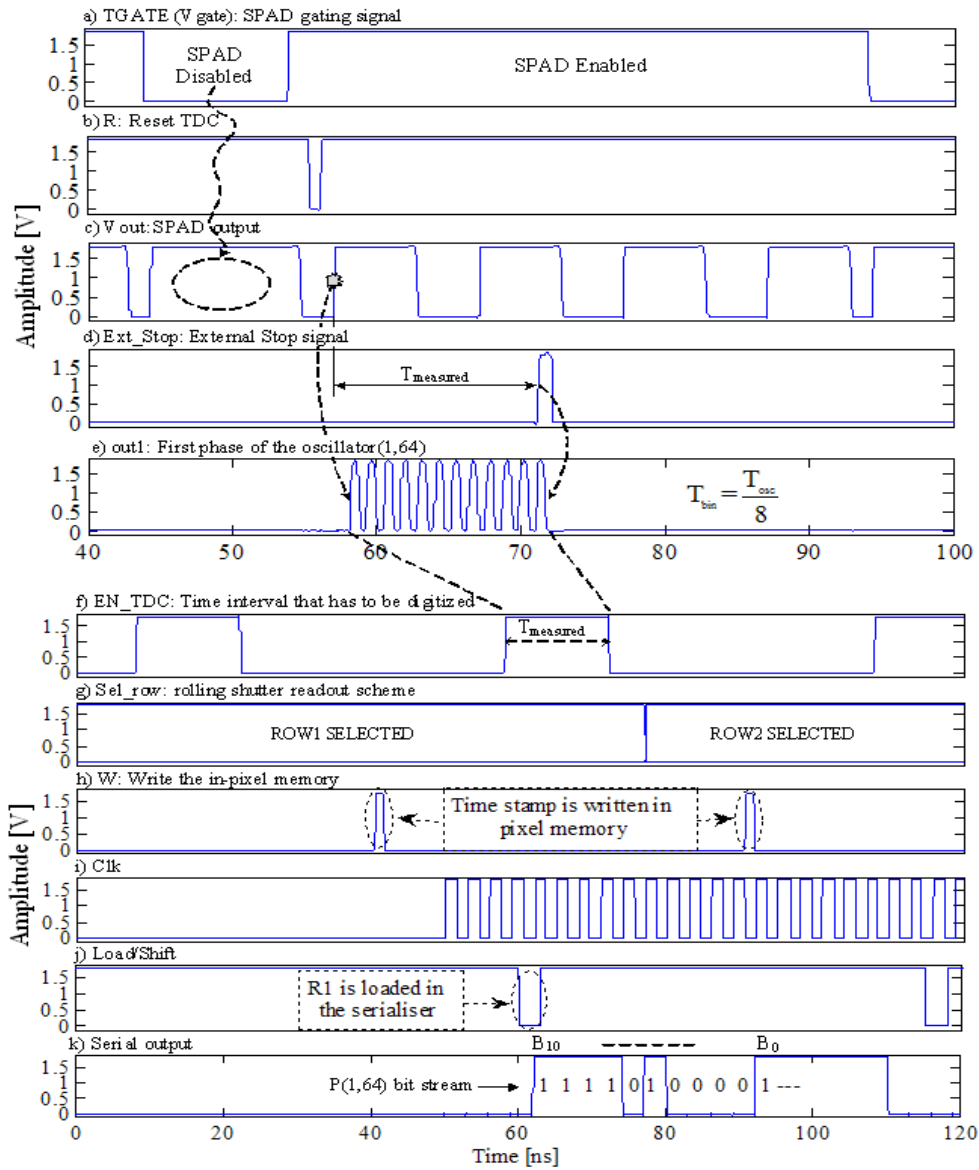


Fig. 4. Signals chronogram in 3D operation mode.

iii) The 2D-mode stands for the acquisition of the illumination map of a scene. It is done by connecting the output of the SPAD,  $V_{out}$ , to the ripple counter of the TDC (see Fig. 11). The amount of photons impinging on one single SPAD is estimated by merely counting pulses. At the end of the integration time the number of the pulses provided by each SPAD has to be proportional to the intensity of the light falling on

that particular photodiode, modified by the influence of spurious avalanches. At this point VCRO is disabled. The imager requires very little power.

### 2.2. Imager design

Each pixel of the array is composed by the single-photon detector, TDC, memory block and tri-state output buffers. The block diagram of the pixel is presented in Fig. 6. The signal MODE1 configures the imager in 2-D or 3-D acquisition mode while MODE2 is used to switch between an external start pulse and the output of the SPAD.

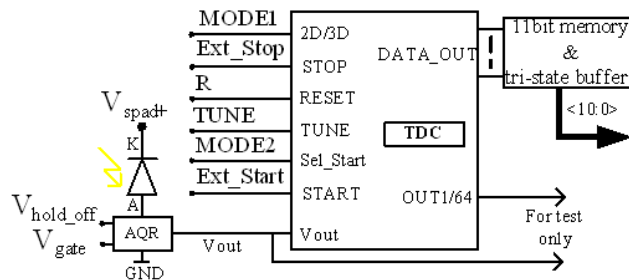


Fig. 6. Block diagram of 2-D/ 3-D pixel.

The signal OUT1/64 is the first phase of the VCRO divided by 64. The rest of the signals are explained in the next subsection. The first block is the SPAD sensor controlled by a time-gated active quenching/recharge circuit (AQR) with tunable dead-time down to 4 ns (see Fig. 10).

In order to build high-resolution single-photon image sensors, the area and power consumption per pixel are the most important constraints. The pixel pitch is 64  $\mu\text{m}$ . The fill factor is 2.7%. The main contribution to power consumption at the pixel level is the operation of the VCRO when running at maximum frequency. The average power consumption at full range and 5 kfps is 2.7  $\mu\text{W}$  per TDC. Pixel layout is depicted in Fig. 7.

The time-stamp digitized by the TDC is stored inside each pixel to allow offline readout at a lower speed. Tri-state buffers are controlled by a row decoder such that each row is successively connected to data serializer.

#### 2.2.1. Single photon detector ensemble

A single-photon avalanche-diode is a *pn* junction reversely biased beyond its breakdown voltage,  $V_{BD}$ . The overvoltage is called excess voltage,  $V_E$  [14]. The cross-section of the p+/n-well SPAD integrated in this chip is depicted in Fig. 8. It has been fabricated in a standard 0.18  $\mu\text{m}$  CMOS process. When a photon impinges on the active surface of the diode, the detection probability is a function of the impact ionization coefficient and depends on the absorption region [15]. Thus, the Photon Detection Probability (PDP) in the space charge region equals the photon absorption probability multiplied by the avalanche triggering probability. In the lower neutral

region, it depends on the collection efficiency. Any photon absorbed in the p-type substrate cannot be detected.

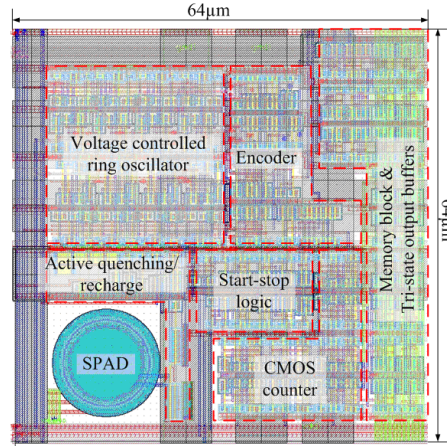


Fig. 7. Pixel layout.

The detected photon triggers an avalanche current,  $I_{SPAD}$ , which is almost instantaneously built up through the SPAD junction. It has to be quenched right away, otherwise the device can be irreversibly damaged. This can be done by a passive (Fig. 8) or an active (Fig. 10) scheme. The comparison between these two strategies is illustrated in Fig. 9. In the steady state region, no reverse current flows between cathode (K) and anode (A) ①. When the avalanche is triggered,  $I_{SPAD}$  increases, the voltage drop on the SPAD diode starts to decrease down to below  $V_{BD}$  ②. Further, if no other photons are absorbed the SPAD is passively recharged through the same resistor ③. Faster restoring of the SPAD is achieved by applying active recharge scheme (Fig. 10). Thus it turns back in the initial steady state ①.

Besides photons, avalanche currents can be also triggered by spurious factors representing the noise of a SPAD. Depending on its nature, these currents are called dark counts (DC's) or afterpulsing (AP) [16].

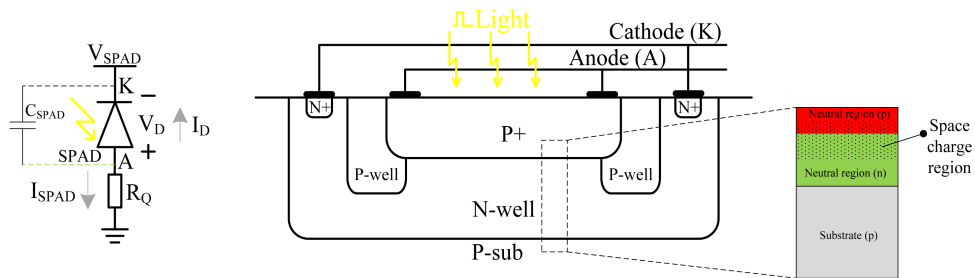


Fig. 8. Cross section of the integrated SPAD.



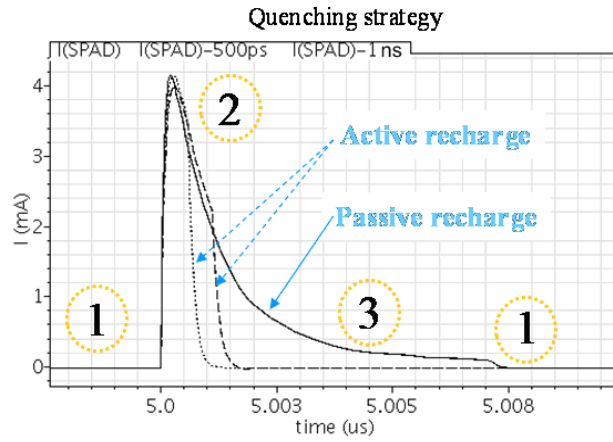


Fig. 9. Active/passive quenching strategy.

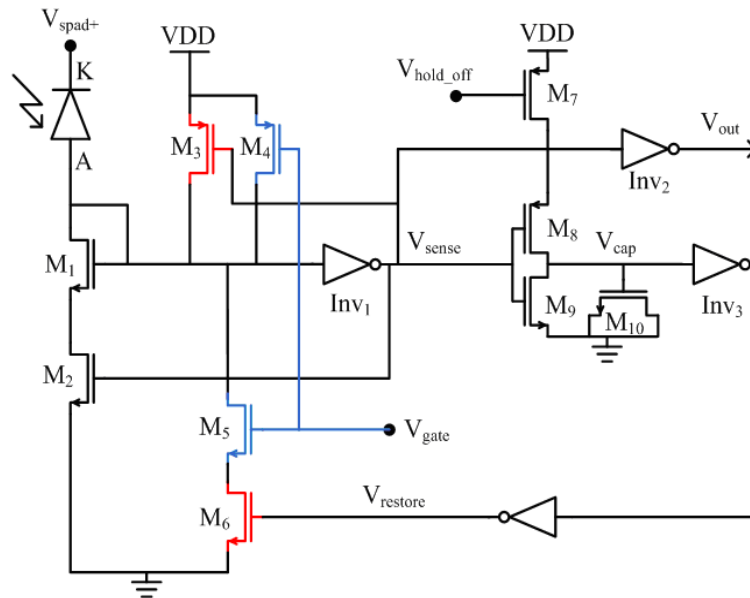


Fig. 10. Proposed time-gated active quenching/recharge circuitry.

The single photon detector ensemble is built by a SPAD and an Active Quenching/Recharge circuit (AQR). This scheme has been proposed for afterpulsing and power consumption reduction. The active area of the quasi-circular diode has a diameter of 12  $\mu\text{m}$ . This SPAD has been demonstrated in a previous work [17]. In addition to that, transistors  $M_4$  and  $M_5$  are added to perform time-gated operations. If  $V_{\text{gate}}$  is tied to VDD then the detector is enabled for proper operation: when an event is detected the avalanche current flows through  $M_{1,2}$  and the voltage of the anode A and  $V_{\text{out}}$  go up.  $V_{\text{sense}}$  goes down and switches on transistors  $M_{3,8}$ . The current

spike is quenched by pulling up the anode terminal. Notice that the quenching phase is speeded up by the positive feedback introduced by  $M_3$ . In the meantime, the MOS capacitor  $M_{10}$  is charged. When  $V_{cap}$  reaches the trip-point of  $Inv_3$  then  $M_6$  is turned on. The anode is pulled down through  $M_{5,6}$  and the SPAD junction is turned on again ready to detect new incoming photons.

If  $V_{gate}$  is tied to ground then the detector is disabled through the transistor  $M_4$ . Furthermore  $V_{out}$  and  $V_{restore}$  are at VDD, switching  $M_6$  on. When  $V_{gate}$  is set to VDD to enable the SPAD then  $M_5$  turns on which automatically restore the detector through the transistors  $M_{5,6}$ . It is worth to mention that the SPAD will not go through the restoring point if the time-gate is smaller than the dead-time. The latter parameter can be adjusted by the voltage  $V_{hold-off}$ .

The detector output  $V_{out}$  is either connected to the TDC for ToF measurements (3-D imaging) or to an 8b counter to evaluate light intensity (2-D imaging) by photon counting.

### 2.2.2. Pixel level TDC

The time interval delimited by the SPAD output pulse and the subsequent synchronization signal coming from the laser driver is locally quantized by a TDC. In order to efficiently save power, the pixel detector ensemble employs a reverse start-stop scheme. In this case the in-pixel TDC is triggered by a photon detection and stopped by the synchronization signal, Ext\_Stop. The actual ToF is directly computed by subtracting the measured time interval from the laser diode period. In order to achieve sub-nanosecond time accuracy, a wide range approach given by large-depth counters has to be combined with time interpolation techniques.

The proposed TDC (block diagram in Fig. 11) is composed by: *i*) a start/stop control unit (Fig. 12a); *ii*) a novel pseudo-differential VCRO [18] which has incorporated an additional control of the oscillation frequency (Fig. 13); *iii*) a coarse counter (Fig. 14a) and *iv*) an encoder for fine approximation (Fig. 14b). The TDC occupies  $29 \times 28 \mu\text{m}^2$ . The best time bin,  $T_{bin}$ , of 145 ps is achieved by interpolating eight phases.

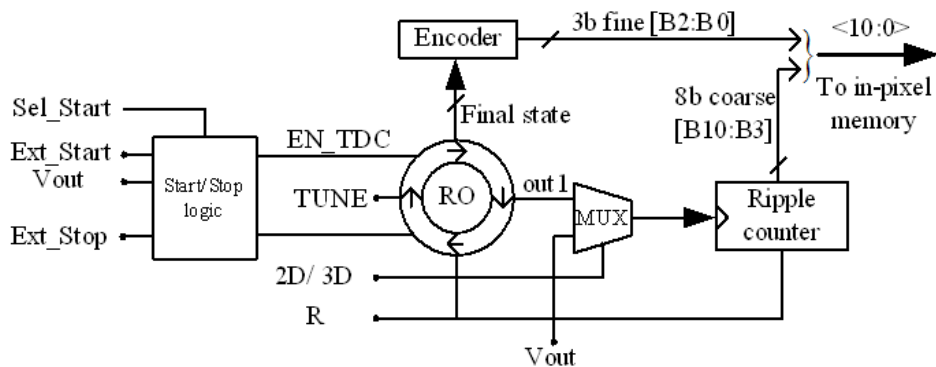
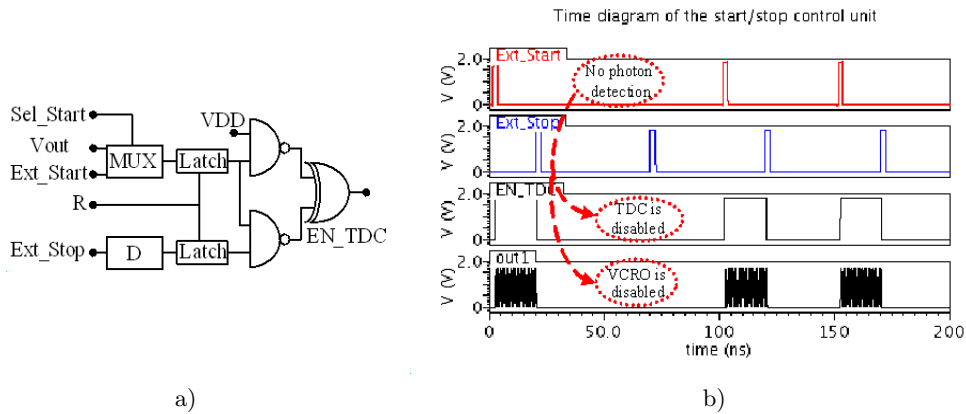


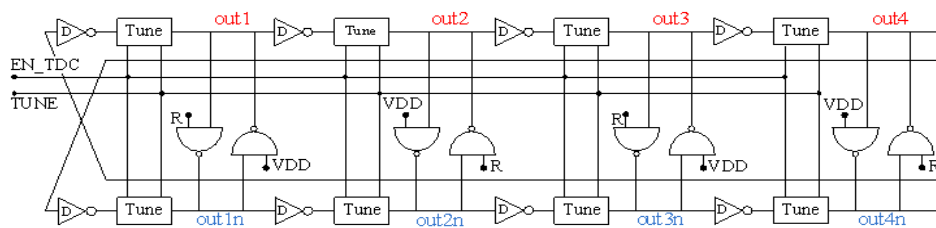
Fig. 11. TDC block diagram.

*i)* The first block has to ensure the proper functionality of the TDC as follows: the TDC is enabled by a start signal which could be either external or the output of the local SPAD. The core oscillator of the TDC is switched-on by the first positive edge of the selected input,  $V_{out}$  or Ext.Start, and is turned-off on the positive edge of the Ext.Stop synchronization signal. If the TDC is triggered by the SPAD then all the subsequent pulses that come after the first one are neglected. If no avalanche occurs then the TDC is not triggered saving significant amount of power considering that this approach applies for the entire array (Fig. 12b). Although the circuit is symmetric, the output EN\_TDC stays disabled every time the Ext.Stop is not preceded by a start signal.



**Fig. 12.** Schematic and time diagram of the start/stop control unit.

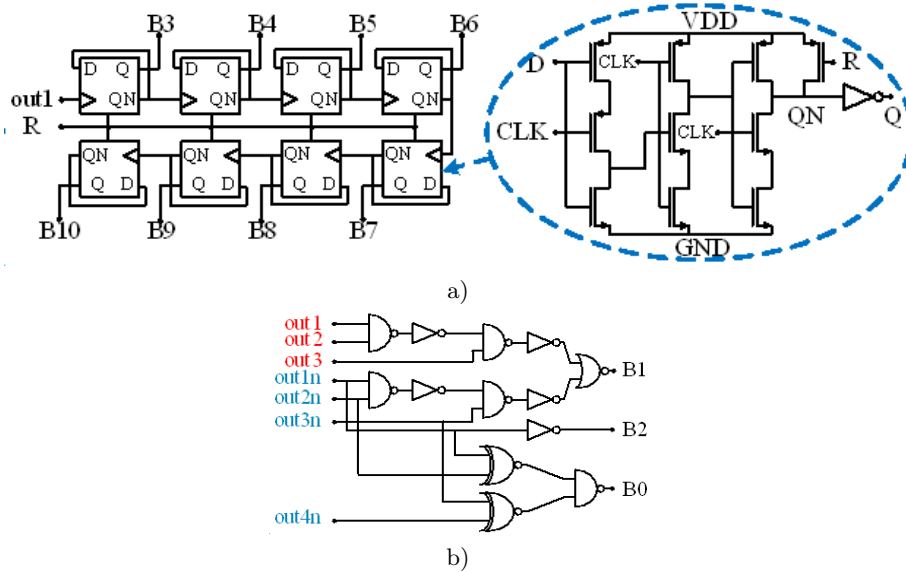
*ii)* The pseudo-differential VCRO is employed for fine conversion by applying phase interpolation. The block diagram is depicted in Fig. 13. As long as the signal EN\_TDC is active, the VCRO works at the frequency defined by the TUNE signal (Fig. 12b). This voltage reference is provided by the on-chip PLL. The finest time bin of the converter is given by the maximum oscillation frequency. Thus, the best time resolution of 145 ps that has been measured is achieved with an oscillation frequency of 862 MHz. In this case, the full-input range of the TDC is of 297 ns. Due to the reverse start-stop scheme, the maximum resolved distance is limited by the oscillator start-up which in this particular design is very fast, negligibly affecting the overall accuracy of the converter. The minimum measured distance is affected by the cumulative jitter of the oscillator which has been evaluated to 13 ps over 400 periods.



**Fig. 13.** Schematic of the pseudo-differential VCRO.

*iii)* The integer number of oscillation periods,  $T_{osc}$ , is counted by a coarse counter depicted in Fig. 14a. It can be connected either to the first phase of the VCRO for ToF estimation or to the output of the SPAD for photon counting. On the positive edge of the Ext\_Stop signal the oscillator is frozen (Fig. 12b). In the former case of 3-D imaging, the counter digits represent the most significant eight bits of the digitized time interval.

*iv)* The eight phases of the oscillator are passed through a thermometric-to-binary code converter (Fig. 14a) to provide the least significant three bits. In the case of 2-D imaging, the content of the counter is proportional with the number of photons while the output of the encoder is a fixed pattern with no meaning in this operation mode. Moreover the oscillator is turned-off.



**Fig. 14.** Schematic of the a) coarse counter based on CMOS DFF and b) encoder.

### 2.2.3. Sensor readout and control circuits

The central part of the imager is the  $64 \times 64$  array of SPAD cells. Each cell has the following I/O signals: *i)* R: the reset of the start/stop control unit, VCRO, 11b memory; *ii)* 2-D/3-D: switches between photon counting (or 2-D imaging – The coarse counter is connected to the SPAD output,  $V_{out}$ , to count the number of photons) and ToF estimation (or 3-D imaging – The coarse counter is connected to the first phase of the VCRO to count the integer number of oscillation periods); *iii)* Sel\_Start: switches between the test mode – the TDCs are triggered by an external start signal, Ext\_Start – and 3-D imaging – each TDC is triggered by local SPAD –; *iv)* Ext\_Start1-64: external start signals that are uniformly distributed to each row of TDCs; *v)* Ext\_Stop: external stop signal that works as a global shutter; *vi)* W: global signal used to write the digitized time interval in the in-pixel memory block; *vii)* Sel\_row1-64: the imager is readout by a rolling shutter scheme. The block diagram of the sensor is

depicted in Fig. 15. The sensor rows are loaded into the data serializer one at a time and delivered off-chip through a single output port. The shifting clock is set to 66 MHz. This limitation is due to the output digital buffers of the chip. The maximum frame rate is about 1.4 kfps at a throughput of 66 Mbps. It can be enhanced up to 22 kfps by parallelizing sixteen outputs, in which case the throughput is about 1 Gbps.

The row decoder is implemented by a shift register. This approach proved to be more suitable for image sensors from the area point of view. Moreover the pulse overlapping issues are easily avoided. The same scheme is employed to distribute the external start signal to certain rows of TDCs previously selected by loading the circular shift register with the appropriate pattern. The time-critical signals are skewless distributed across the array. The signals chronograms of the imager explain how the imager works both in test and 3-D operation mode (Figs. 3, 4).

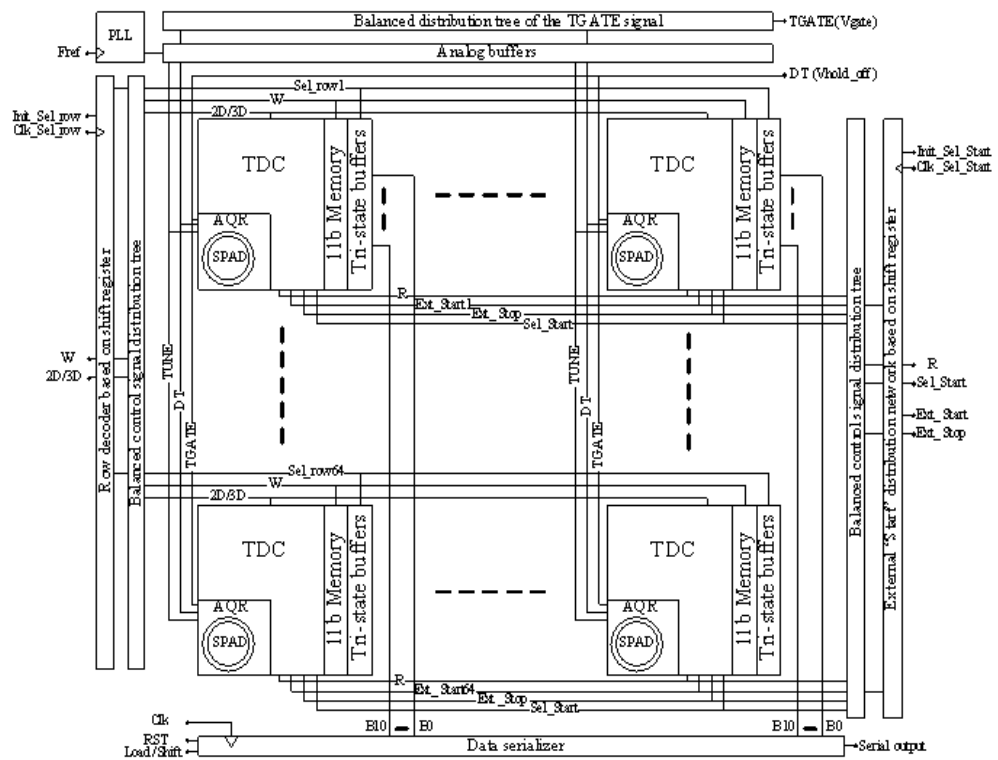


Fig. 15. Block diagram of the 3D imager.

2.2.4. Time resolution programmability

The oscillation frequency of the array of VCROs is controlled by the reference voltage taken from the loop filter of the on-chip integrated PLL (Fig. 16). This

scheme implements a double functionality: global calibration against process, power supply voltage and temperature variations and time resolution programmability. The measured time resolution of the TDCs array can be set between 357 ps and 145 ps. This is done by changing the loop division factor of the frequency divider. A post-layout simulation illustrating this scenario is depicted in Fig. 17.

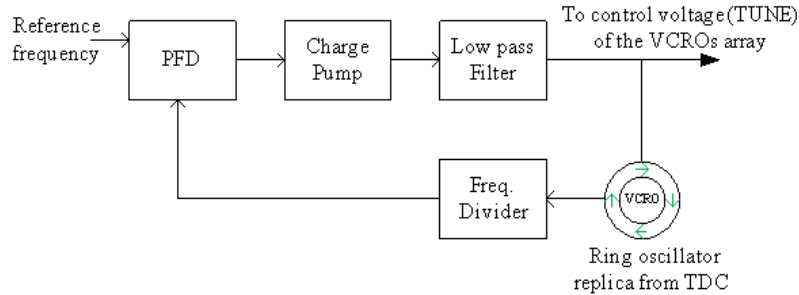


Fig. 16. Block diagram of the time resolution programmability.

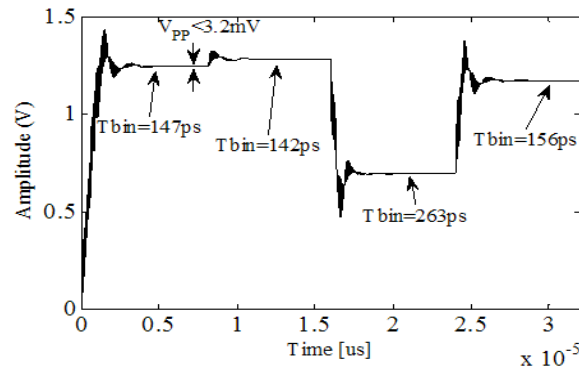


Fig. 17. Time resolution programmability.

### 3. Measurements results

This work reports measurements results on the TDC time accuracy (Fig. 18), jitter, code uniformity across the array (Fig. 22) and waveforms of the time-gated operation (Fig. 23). The accuracy of a single TDC is measured as less than  $\pm 1$ LSB DNL and  $\pm 1.7$  LSB INL. The imager is controlled by a VIRTEX5-FPGA.

The single row uniformity is measured at 90% of the full signal range at the maximum speed of the VCROs. The standard deviation is about 14.78 codes (Fig. 19). The average time bin across one row of 64 TDCs is of 145 ps. The maximum deviation of the time resolution is about 0.03 LSB. The static transfer characteristics of a single row of 64 TDCs are depicted in Fig. 20. The time intervals with an incremental 8 ps time resolution have been generated by a time interval generator [13]. Each time

interval has been measured in the same time by the TDCs array and a highly accurate instrument with 8 ps time resolution [19].

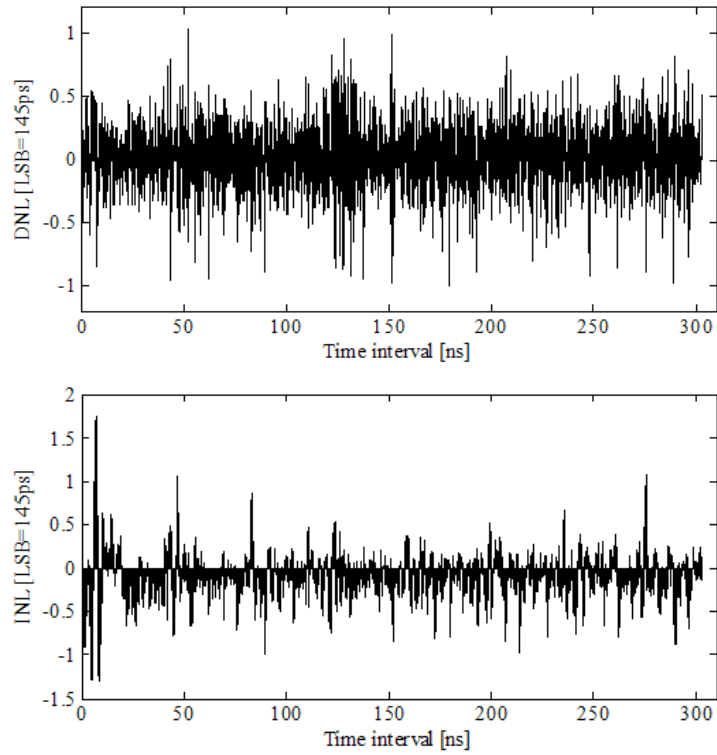


Fig. 18. TDC DNL and INL are below  $\pm 1$  LSB and  $\pm 1.7$  LSB, respectively.

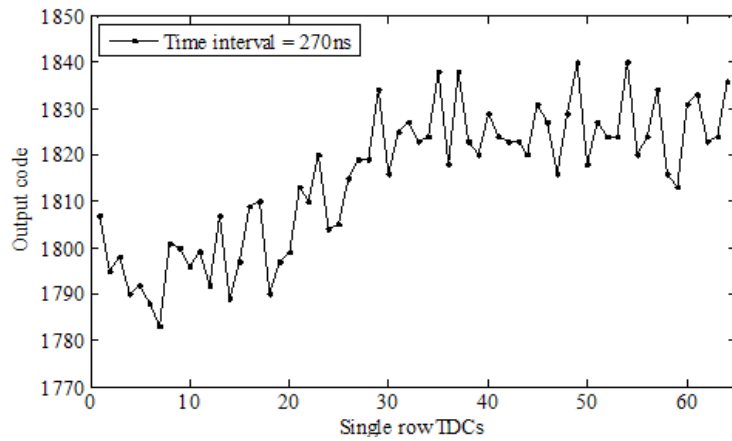


Fig. 19. Single row uniformity.

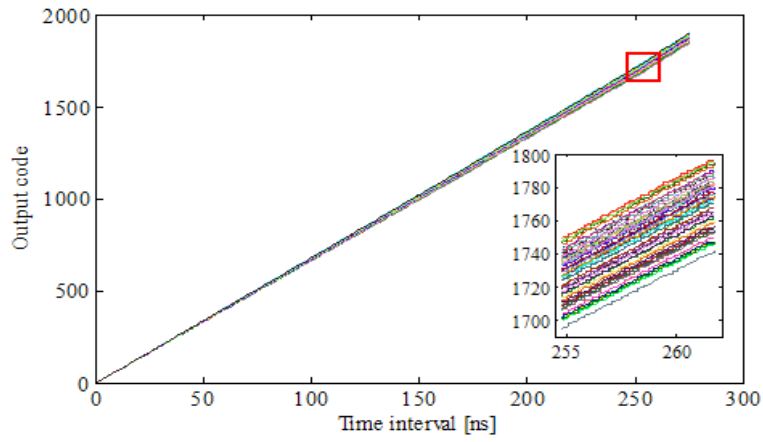


Fig. 20. Single row – 64 TDCs static transfer characteristic.

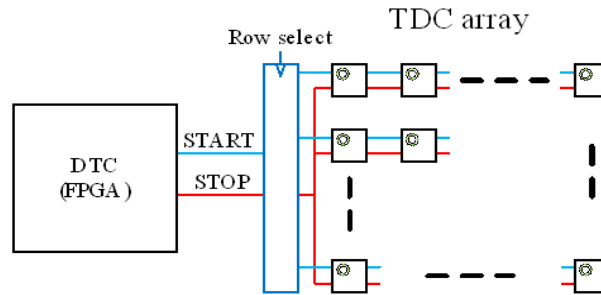


Fig. 21. Test scheme of the TDCs array.

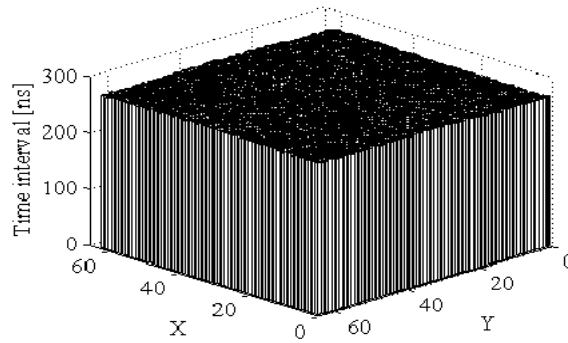


Fig. 22. TDC array code uniformity.

The TDCs array uniformity is evaluated converting a time interval of 270 ns. It represents 90% of the full signal range. The standard deviation across the array is about 19 codes.



The proper functionality of the time-gated setup is depicted in Fig. 23. The imager is enabled on the lower level of TGATE signal. In this case the START signal is provided by the SPAD detector of the pixel (64, 64). The local TDC is switched on by the first photon detection. The conversion stops on the negative edge of the synchronization signal, STOP. The time window that needs to be resolved is about 280ns (see signal TINT). The third analog channel depicts the output of the VCO divided by 64. At the end of the conversion time, the result is stored by the in-pixel memory. Each frame is readout through a single ended fast IO buffer (SOUT) for off-line data processing.

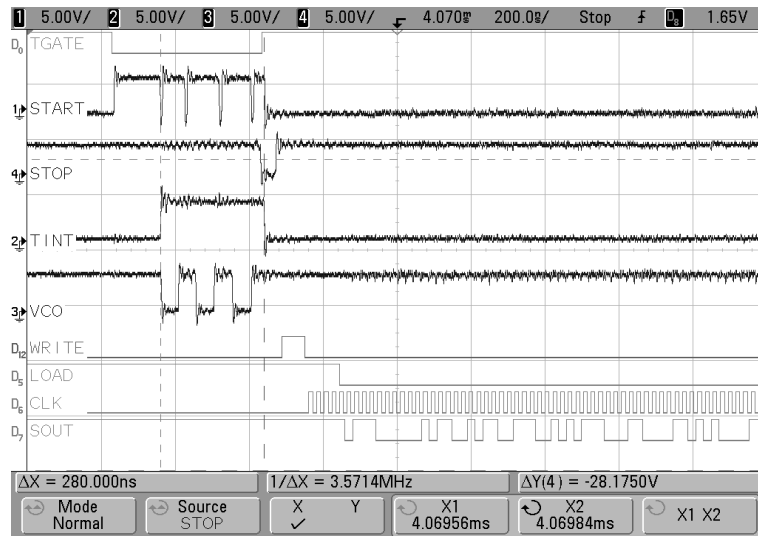


Fig. 23. Signal waveforms in 3D operation mode.

The test mode is implicitly proved by the 3-D mode while the only difference is that the START signal is globally generated externally, instead of each in-pixel SPAD detector.

The 2-D mode uses only a part of the 3-D mode architecture. Consequently the proper functionality of the 2-D mode is already present in the previous measurements.

Table 1. Comparison with state-of-the art 3D imagers

Performances	[1]	[4]	[12]	This work
Technology	HV 0.8 $\mu\text{m}$	0.13 $\mu\text{m}$	0.13 $\mu\text{m}$	0.18 $\mu\text{m}$
Format	32 $\times$ 32	32 $\times$ 32	32 $\times$ 32	<b>64<math>\times</math>64</b>
Pitch/ Fill factor	58 $\mu\text{m}$ /1.1%	50 $\mu\text{m}$ / -	50 $\mu\text{m}$ / -	<b>64 <math>\mu\text{m}</math> / 2.7%</b>
$T_{bin}$ $N_{bits}$	115 ps/ -	119 ps/10 bits	52,178 ps/10 bits	145 ps/11 bits
Dead time	< 40 ns	-	-	<b>4 ns - 500 ns</b>
TDC area			2200 $\mu\text{m}^2$	<b>1740 <math>\mu\text{m}^2</math></b>
TDC avg. power	-	-	38 $\mu\text{W}^1$	<b><math>\sim</math> 9 <math>\mu\text{W}^1</math></b>

<sup>1</sup>This power has been evaluated for 10 ns conversion time interval and 500 kfps.

## 4. Conclusion

A  $64 \times 64$  2-D/ 3-D imager based on SPADs was designed and fabricated in  $0.18 \mu\text{m}$  standard CMOS process. It incorporates double functionality: photon counting and ToF measurement. The pixel pitch is  $64 \mu\text{m}$  with a fill factor of 2.7%. It incorporates the SPAD detector, very fast AQR with adjustable dead-time down to 4 ns, low power TDC and 11 b memory with tri-state buffers. The finest time resolution is about 145 ps at  $9 \mu\text{W}$  normalized power consumption<sup>1</sup> per TDC.

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